

LATCH UP DETECTION

ABSTRACT

A device is presented. The device includes a first circuit coupled to first and second power rails of the device. The first circuit is subject to a latch up event in the presence of a latch up condition. The latch up event includes a low resistance path created between the first and second power rails. The device also includes a latch up sensing (LUS) circuit coupled to the first circuit. The LUS circuit is configured to receive a LUS input signal from the first circuit and generates a LUS output signal to the first circuit. When the input signal is an active latch up signal which indicates the presence of a latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

Fig. 1