**WHAT IS CLAIMED IS:**

1. A semiconductor device comprising:

an electrically insulating film (10) having a device hole (12);

a plurality of lead groups (30A-30D), each comprising a plurality of leads (30), arranged in a predetermined pattern that is formed in a corresponding plurality of lead formation regions (100-400) on the surface of said film, each lead formation region being located between said device hole and a respective outer edge (10a) of said film;

an integrated circuit chip (20) which is arranged within said device hole of said film and which has electrodes connected to ends of said leads;

a first group of aperture portions (14a-14d) which consists of at least one aperture portion and which is provided within a region (500-800) other than said lead formation regions;

a second group (16) of aperture portions (16a-16e) provided in each of said lead formation regions, each second group (16) consisting of a plurality of aperture portions with linking portions (18a-18d) defined between adjacent aperture portions; and

a resin sealing portion (50) that seals in at least said integrated circuit chip, said film, and said lead groups;

characterized in that each linking portion (18a-18d) is defined between a pair of parallel linear edges, one edge of each of two adjacent aperture portions, and a longitudinal direction of each

960124-8
2/3/99

linking portion, which is perpendicular to said pair of edges, intersects edges (10a) of said film (10) at an angle of approximately $45^0$.

2. A semiconductor device according to claim 1, wherein each of said leads (30) comprises an inner lead portion (32) protruding into said device hole (12) and an outer lead linkage portion (34) protruding outward beyond said respective outer edge (10a) of said film (10), said outer lead linkage portion being connected to an outer lead (40) of a mechanical strength greater than that of said outer lead linkage portion.

3. A semiconductor device according to claim 1 or claim 2, wherein said linking portions (18a-18d) are orientated such that said longitudinal directions of each linking portion is perpendicular to the leads (30) formed on that linking portion.

4. A semiconductor device according to any one of claim 1 to claim 3, wherein said plurality of aperture portions in each second group of aperture portions define a line of symmetry which is perpendicular to said respective outer edge (10a) of said film (10) and with respect to which the aperture portions are arranged in axial symmetry.

5. A semiconductor device according to any one of claim 2 to claim 4, wherein said leads (30) have straight portions and bend portion so as to allow the pitch of said inner lead portions (32) to be smaller than that of said outer lead linkage portions (34), and

said plurality of aperture portions (16a-16d) of each second group (16) are formed at positions separated from those where said bend portions of said leads are formed.

6. A semiconductor device according to any one of claim 1 to claim 5, wherein side leads (36) forming the two outermost leads of each lead groups (30A-30D) have a mechanical strength greater than that of the remaining leads (30) of the respective lead group.

7. A semiconductor device according to any one of claim 1 to claim 6, wherein said integrated circuit chip (20) is positioned at substantially the center of said resin sealing portion (50) in a direction perpendicular to the plane of said film (10).

8. A semiconductor device according to claim 7, wherein each of said leads (30) comprises an inner lead portion (32) protruding into said device hole (12), an outer lead linkage portion (34) protruding outward beyond said respective outer edge (10a) of said film (10) and an intermediate lead portion, each lead being bent such that said outer lead linkage portions, said inner lead portions and said intermediate lead portions are in a first, a second and a third one, respectively, of three parallel planes displaced with respect to each other in the direction perpendicular to the plane of said film (10), and the position of said integrated circuit chip (20) is set by the distance ($d_{OF}$) between said first and said third plane and the distance ($d_{IF}$) between said second and said third plane.

9. A semiconductor device according to claim 9, wherein each of said leads (30) comprises an inner lead portion (32) protruding into said device hole (12), an outer lead linkage portion (34) protruding outward beyond said respective outer edge (10a) of said film (10) and an intermediate lead portion, each lead being bent such that said inner lead portions and said intermediate lead portions are in a first and a second one, respectively, of two parallel planes displaced with respect to each other in the direction perpendicular to the plane of said film (10), and the position of said integrated circuit chip (20) is set by the distance between said first and said second plane and by outer leads (40) connected to said outer leads linkage portions.

10. A semiconductor device according to any one of claim 1 to claim 9, wherein, in a region encompassing inner lead portions of said leads (30) and said electrodes of said integrated circuit chip (20)connected to ends of said inner lead portions, a resin layer (52) consisting of a resin having good adhesive properties with respect to both said leads (30) and the resin forming said resin sealing portion (50) is formed between the former and the latter.

11. A semiconductor device according to any one of claim 1 to claim 10, wherein a radiator portion (60; 68) is connected to said integrated circuit chip (20).

12. A semiconductor device according to claim 11, wherein a plurality of aperture portions (62) are formed in said radiator portion (60).

13. A semiconductor device according to claim 11 or 12, wherein at least a part (68a) of said radiator portion (68) is exposed from said resin sealing portion (50).

14. A method of manufacturing a semiconductor device, comprising the steps of:

(A) forming, in an electrically insulating film (10), a device hole (12), a first group of aperture portions (14a-14d) consisting of at least one aperture portion within a region (500-800) outside of lead formation regions (100-400), and a second group (16) of aperture portions provided in each of said lead formation regions, each second group (16) consisting of a plurality of aperture portions (16a-16d) with linking portions (18a-18d) defined between adjacent aperture portions;

(B) attaching a conductive film to said film, using photolithography and etching to form leads (30) that each comprise an inner portion protruding into said device hole and an outer lead linkage portion, within said lead formation regions of said film, then placing an integrated circuit chip (50) within said device hole and connecting electrodes of said integrated circuit chip to said inner lead portions:

(C) superimposing on a predetermined position of said film a lead frame (80) having outer leads (40) arranged at the

same pitch as said outer lead linkage portions and having a mechanical strength greater than that of said outer lead linkage portions, and connecting said outer lead linkage portions to said outer leads; and

(D) using transfer molding to form a resin sealing portion (50) so as to seal said integrated circuit chip, said leads, and part of said outer leads therein;

characterized in that step (A) comprises forming said aperture portions (16a-16d) of said second group (16) such that each linking portion (18a-18d) is defined between a pair of parallel linear edges, one edge of each of two adjacent aperture portions, and a longitudinal direction of each linking portion, which is perpendicular to said pair of edges, intersects edges (10a) of said film (10) at an angle of approximately $45^0$.

15. A method of manufacturing a semiconductor device according to claim 16, wherein in said step (B), said integrated circuit chip (20) is arranged to be positioned such that it will be at substantially the center of said resin sealing portion (50) formed in step (D) in a direction perpendicular to the plane of said film (10).

16. A method of manufacturing a semiconductor device according to claim 14 or 15, further comprising a step of forming, before step (D), a resin layer (52) consisting of a resin having good adhesive properties with respect to both said leads (30) and the resin used

in step (D), in a region encompassing inner lead portions of said leads and electrodes of said integrated circuit chip (20).