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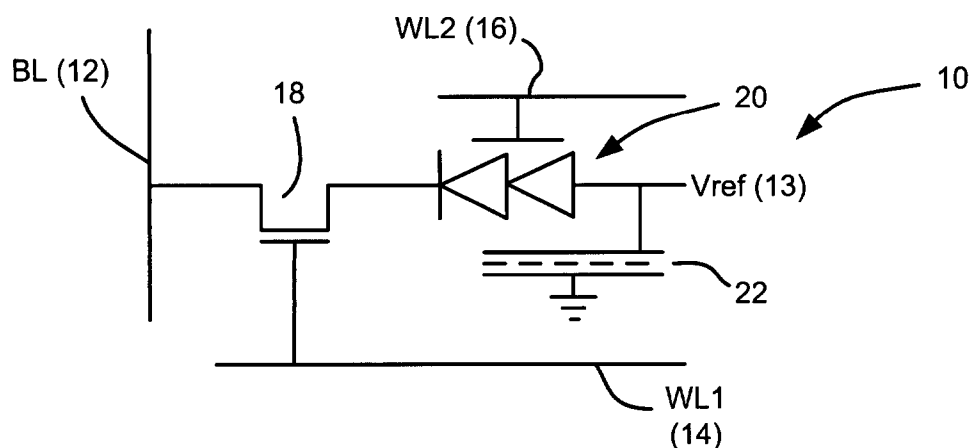
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(54) Title: SILICON ON INSULATOR READ-WRITE NON-VOLATILE MEMORY COMPRISING LATERAL THYRISTOR AND TRAPPING LAYER



(57) Abstract: Disclosed herein is an improved thyristor-based memory cell. In one embodiment, the cell (10) is formed in a floating substrate using Silicon-On-Insulator (SOI) technology. The cell preferably incorporates a lateral thyristor (20) formed entirely in the floating substrate, and which is gated by a second word line. The cathode of the thyristor also comprises a source of an access transistor (18), whose drain is connected to the bit line of the device, and which is gated by a first word line (14). A trapping layer is built into the floating substrate, and when writing to the cell, pulses are added to cause holes to be trapped on the trapping layer for a logic state '1' and to cause electrons to be trapped on the trapping layer for a logic state '0'. Trapping of charges on the trapping layer adds extra margin to the stored data states, prevents their degradation, and renders the cell non-volatile.

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