(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 February 2003 (27.02.2003)

PCT

(10) International Publication Number
WO 03/017648 A2

(51) International Patent Classification[7]: H04N 5/335

(21) International Application Number: PCT/US02/26061

(22) International Filing Date: 16 August 2002 (16.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/313,117 17 August 2001 (17.08.2001) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventors: HANSON, Eric; 354 Bramertown Road, Tuxedo, NY 10987 (US). KRYMSKI, Alexander; 2960 Mountain Pine, La Crescenta, CA 91214 (US). POSTINIKOV, Konstantin; 28600 Devil's Punchbowl Road, Pearblossom, CA 93553 (US).

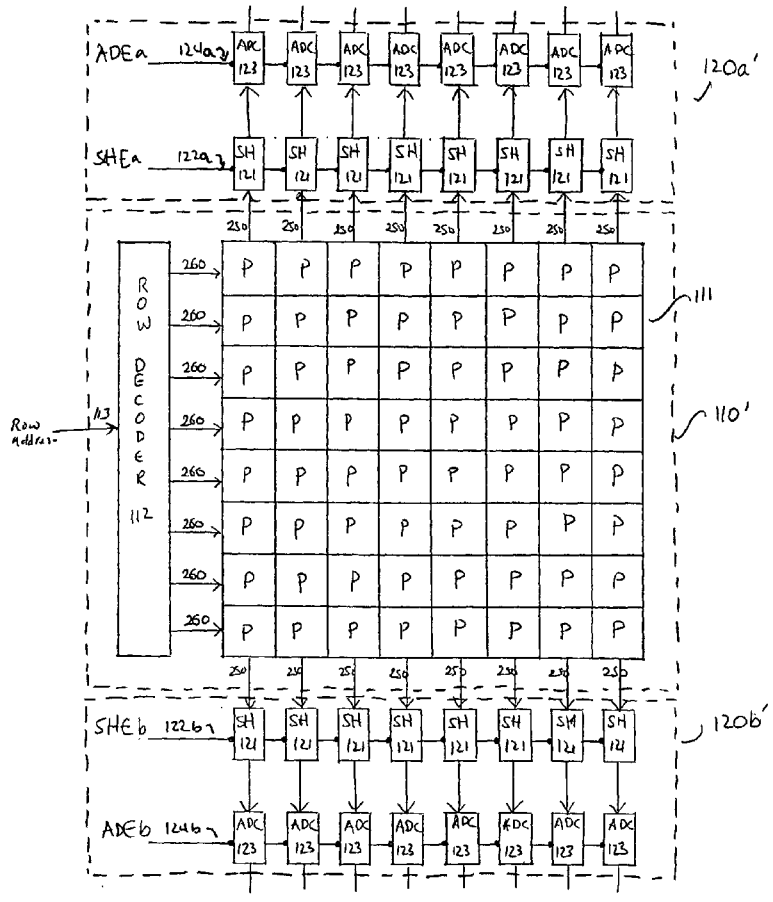
(74) Agent: D'AMICO, Thomas, J.; Dickstein Shapiro Morin & Oshinsky LLP, 2101 L Street, N.W., Washington, DC 20037-1526 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

*[Continued on next page]*

(54) Title: DOUBLING OF SPEED IN CMOS SENSOR WITH COLUMN-PARALLEL ADCS




(57) Abstract: An imaging system features high speed digitization of pixel signals by utilizing top and bottom digitization circuits which pipeline sample-and-hold operations with analog-to-digital conversion. In operation, while one digitization circuit is performing a sample-and-hold operation, the other digitization circuit is performing analog-to-digital conversion. The speed of the imaging system may be further increased by pipelining and interleaving operations within the top and bottom digitization circuits by using additional sets of sample-and-hold circuits and analog-to-digital converters.

WO 03/017648 A2

Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**

— *without international search report and to be republished upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*