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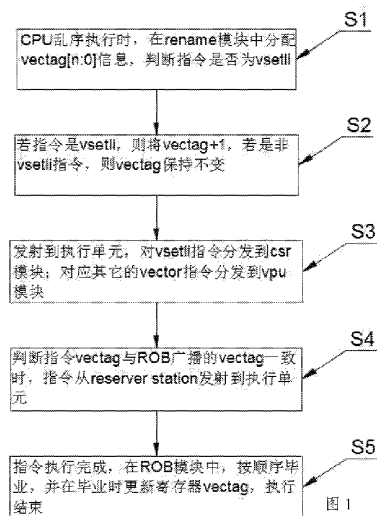
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(81) 指定国 (除另有指明, 要求每一种可提供的国家保护): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK,

(54) Title: METHOD AND SYSTEM FOR IMPLEMENTING VSETLI INSTRUCTION IN RISV_V VECTOR INSTRUCTION SET

(54) 发明名称: risv_v vector指令集vsetli指令的实现方法及系统



- S1 When a CPU executes out of order, allocate vectag[n:0] information in a rename module and determine whether an instruction is vsetli
S2 If the instruction is vsetli, add 1 to vectag, and if the instruction is not a vsetli instruction, keep the vectag unchanged
S3 Transmit to an execution unit, and distribute the vsetli instruction to a csr module; and distribute corresponding other vector instructions to a vpu module
S4 When it is determined that the vectag of the instruction is consistent with vectag broadcasted by ROB, transmit the instruction from a reserver station to the execution unit
S5 After execution of the instruction is completed, graduate in sequence in the ROB module, update vectag of a register at the time of graduation, and end the execution

(57) Abstract: The present invention relates to the technical field of CPUs, and in particular, to a method and system for implementing a vsetli instruction in a risv_v vector instruction set. The method comprises: when a CPU executes out of order, allocating vectag[n:0] information in a rename module and determine whether an instruction is vsetli; if the instruction is vsetli, adding 1 to vectag, and if the instruction is not a vsetli instruction, keeping the vectag unchanged; transmitting to an execution unit, and distributing the vsetli instruction to a csr module; distributing corresponding other vector instructions to a vpu module; when it is determined that the vectag

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of the instruction is consistent with vectag broadcasted by ROB, transmitting the instruction from a reserver station to the execution unit; and after execution of the instruction is completed, graduating in sequence in the ROB module, updating vectag of a register at the time of graduation, and ending the execution. In the present invention, the execution efficiency of a non-vsetl{i} Vector instruction is high. Data is selected using a mask mode, and thus, the power consumption is reduced; moreover, the execution period can be reduced, the latency is reduced, and the present invention has a wide market application prospect.

(57) 摘要: 本发明涉及CPU技术领域, 具体涉及一种risv_y vector指令集vsetli指令的实现方法及系统, CPU乱序执行时, 在rename模块中分配vectag[n:0]信息, 判断指令是否为vsetli; 若指令是vsetli, 则将vectag+1, 若是非vsetli指令, 则vectag保持不变; 发射到执行单元, 对vsetli指令分发到csr模块; 对应其它的vector指令分发到vpu模块; 判断指令vectag与ROB广播的vectag一致时, 指令从reserver station发射到执行单元; 指令执行完成, 在ROB模块中, 按顺序毕业, 并在毕业时更新寄存器vectag, 执行结束。本发明非vsetl{i}Vector指令执行效率高。通过mask的方式来对数据进行选择, 减少了功耗, 同时可以减少执行周期, 减少了latency, 具有很强的市场应用前景。