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"AM STEREO RECEIVER".

The present invention relates to an AM stereo receiver.

One known type of AM stereo receiver has been disclosed in Japanese Patent Publication No. 140901/78. This AM stereo system is also referred to as an "AM-PM system" in which an amplitude modulation (AM) sum signal L+R and a phase modulation (PM) difference signal L-R are transmitted from a transmitter. As is conventional, the reference letter L stands for the left channel stereo signal and R stands for the right channel stereo signal.

Accordingly, a known AM stereo receiver includes an antenna circuit, an RF amplifier stage and an intermediate frequency amplifier stage in the same way as a known AM radio receiver, and forms the sum signal (monaural signal) L+R by AM detecting a received signal obtained through the intermediate frequency amplifier stage. On the other hand, the difference signal L-R is formed by PM detecting the received signal. Both signals are composed (added or subtracted) in a matrix circuit to obtain a left channel stereo signal L and a right channel stereo signal R.

In the above referred to PM detection, an AM modulation component is removed by a limiter amplifier. Consequently, the difference signal L-R formed by the PM detection has a constant level which is irrelevant to an RF input field intensity RF_{1N} , as shown in the graph of Figure 1 of the accompanying drawings, whereas the sum signal L+R formed by the AM detection changes proportionally to the RM input field intensity RF_{1N} as shown in Figure 1. If both signals are directly composed by the matrix circuit, satisfactory stereo separation cannot be obtained. Hence, the difference signal L-R formed by the PM detection must be passed through a variable gain circuit which is subject to control by an AGC voltage varying in accordance with the level of the sum signal L+R, in order to realize level matching between both signals.

We have found that the following problem arises in this case.

As shown in the graph of Figure 2 of the accompanying drawings, the above referred to AGC voltage V_{AGC} contains an offset voltage V_{offset} due to the D.C. bias voltage in a detection element such as a transistor for the AM detecting operation. Moreover, the offset voltage V_{offset} in the AGC voltage frequently corresponds to a base bias voltage of the transistor which is level-shifted by the base-to-emitter voltage of the transistor. In other words, the AGC voltage has temperature dependency in accordance with the temperature characteristic of the base-to-emitter voltage of the transistor. This results in difficulty in level matching between the difference signal L-R and the sum signal L+R due to the temperature change and as a result deterioration of stereo separation

occurs.

The present invention is therefore directed to provide an AM stereo receiver which prevents deterioration of stereo separation due to the temperature change.

- 5 According to the present invention there is provided an AM stereo receiver for receiving stereo signals having an amplitude modulation sum signal component and a phase modulation difference signal component, the receiver including:
- 10 (a) a signal source circuit for receiving such AM stereo signals, the output of which circuit when it receives such signals in use still contains the said signal components;
- (b) an AM detector for generating a signal proportional to said amplitude modulation sum signal component;
- 15 (c) a PM detector for generating a signal proportional to said phase modulation difference signal component;
- (d) a variable gain circuit to which said phase modulation difference signal is applied;
- 20 (e) a matrix circuit for generating stereo reproduction signals by composing said sum signal component and said difference signal component passed through said variable gain circuit;
- (f) a detecting transistor formed in an integrated
- 25 circuit in the AM detector;
- (g) means for obtaining an AGC voltage by smoothing said sum signal component obtained from the output of the detecting transistor;
- (h) a level shift transistor formed in the integrated
- 30 circuit;
- (i) means for applying a voltage virtually equal to the base D.C. input voltage of said detecting transistor to the base electrode of the level shift transistor, in order to provide a level shift voltage from the emitter electrode

of said level shift transistor; and

(j) means for controlling the gain of the variable gain control circuit by the difference voltage between the AGC voltage and the level shift voltage.

5 Preferably the AGC voltage in the signal source circuit and the difference voltage for controlling the variable gain of the variable gain circuit are generated independently of each other, and influences of a strong interference electromagnetic wave can be reduced.

10 The present invention will now be described in greater detail by way of example with reference to the remaining figure of the accompanying drawing, wherein:-

Figure 3 is a circuit diagram of a preferred form of an AM stereo receiver.

15 Referring now to Figure 3, circuit elements (circuit blocks) formed in portions IC_1 , IC_2 encompassed by dash lines are formed respectively in one silicon chip by a known semiconductor manufacturing technique.

20 Numerals within circles represent terminal numbers of respective monolithic semiconductor integrated circuits, which are connected to external circuit networks constructed by external components via these terminals.

25 The circuit portion IC_1 forms a signal source circuit, which is a known monolithic semiconductor integrated circuit forming an AM radio receiver.

30 The radio frequency signal wave transmitted from a broadcasting station is received by an antenna ANT and is applied to a terminal No. 1 of the circuit portion IC_1 via an inter-stage frequency selector element 1. The received signal applied to the terminal No. 1 is amplified by an RF (radio frequency) amplifier stage 2 and is then

applied to a frequency convertor stage 4 via another inter-stage frequency selector element 3 that is interposed between terminals No. 2 and No. 3. A local oscillation signal is generated inside the frequency convertor stage 4, this local oscillation signal being higher than that of the RF stage by an intermediate frequency. This local oscillation signal and the RF signal are mixed to form an intermediate frequency signal is applied to a first intermediate frequency amplifier stage 6 via still another inter-stage frequency selector element 5 connected between terminals No. 4 and No. 5 where the intermediate signal is amplified. The amplification output signal is applied to a second intermediate frequency amplifier stage 8 via an interstage frequency selector element 7 connected between terminals No. 6 and No. 7 for amplification. The second intermediate frequency amplification output signal is applied to an AM detector 9. The AM detector 9 generates an AM detection output signal free from carrier components by means of a low pass filter 10 connected to a terminal No. 9 and produces the output from this terminal.

A resistor R_1 and a capacitor C_{101} connected to a terminal No. 8 together form an AGC filter, which smoothes the AM detection signal and generates an AGC voltage V_{AGC1} .

This AGC voltage V_{AGC1} is used for automatically controlling the gains of the RF amplifier stage 2 and of the first intermediate frequency amplifier stage 6.

To minimize influences of a strong interference electromagnetic wave, there are provided a reference voltage generated by a reference voltage source 11 and a voltage comparator 12. The voltage comparator 12 receives

on its non-inverting input the output voltage from the RF amplifier stage 2 and on its inverting input the reference voltage provided by the reference voltage source 11.

5 When the signal amplitude of the RF amplifier stage 2 exceeds the value of the reference voltage, the voltage comparator 12 charges up the capacitor C_{101} of the AGC filter by means of its detection output signal in order to increase the AGC voltage and thus to reduce the gain of the RF amplifier stage 2.

10 By the drop of the gain of this RF amplifier stage 2 in cooperation with the action of the inter-stage frequency selector element, the relative level difference of the interference electromagnetic wave with respect to the received signal can be greatly reduced on the output side
15 of the IF amplifier stage.

The detailed operation of the above referred to AM radio receiver is explained in United States Patent Specification No. 4,030,035. The monolithic semiconductor integrated circuit having the above referred to construction,
20 is manufactured by us under the tradename "HA1199".

The circuit portion IC_2 forms an AM stereo demodulator.

The signal at the terminal No. 7 of the circuit portion IC_1 , which is the input signal to the second
25 intermediate frequency amplifier stage 8 in IC_1 , is applied to a terminal No. 1 of the second circuit portion IC_2 via a coupling capacitor C_{102} . The intermediate frequency signal thus received at the terminal No. 1 is amplified by an amplifier 8' in the same way as in the second
30 intermediate frequency amplifier stage 8 in the first circuit portion IC_1 . This amplifier 8' consists of a common-

emitter amplifying transistor Q_1 and an emitter follower transistor Q_2 . The base electrode of the transistor Q_2 receives the collector output of the transistor Q_1 . The emitter output signal of the emitter follower transistor Q_2 is subjected to voltage division by resistors R_4 to R_6 and is negatively fed back to the base electrode of the amplifying transistor Q_1 , in order to set the voltage gain. A load resistor R_3 is provided in the collector circuit of the transistor Q_1 .

The output signal of the amplifier 8' is applied to the base electrode of a detection transistor Q_5 forming an AM detector 9'. A resistor R_8 and an emitter follower AM detection capacitor C_{107} are connected to the emitter electrode of the detection transistor Q_5 . A low pass filter 10' consisting of a resistor R_{101} and a capacitor C_{104} is connected to the emitter electrode of the detection transistor Q_5 via a terminal No. 3 in order to remove the carrier signal from the AM detection signal.

The AM detection signal (sum signal $L+R$) after removal of the carrier signal is applied to a terminal No. 4 via a coupling capacitor C_{105} and is delivered to one of input terminals of a matrix circuit 20.

On the other hand, the output signal of the amplifier 8' is also applied to a limiter amplifier 13. The first stage circuit of the limiter amplifier 13 comprises differential transistors Q_3 and Q_4 , an emitter constant current source I_0 and collector resistors R_6 and R_7 . A similar differential amplifier 13a has its two inputs connected to the collector electrodes of the transistors Q_3 and Q_4 . The D.C. output signal is fed back by a buffer amplifier 13b and a capacitor C_{103} connected to a

terminal No. 2.

After the AM modulation component is removed by the limiter amplifier 13, the intermediate frequency amplification signal is applied to a PM detector 14 to enable PM detection to be carried out.. The PM detection signal (difference signal L-R) is level-adjusted in accordance with the sum signal L+R by a variable gain circuit 15.

After the level adjustment, the difference signal (L-R) is fed to the other input terminal of the matrix circuit 20 via a mute circuit 16 provided for stereo/monaural selection.

In the AM-PM system described above, when carrier disappearance is caused by a large negative peak due to over saturation exceeding 100% AM modulation index or noise, an undesirable burst noise occurs in the PM detection output and causes offensive noises. The intermediate frequency amplification signal from the limiter amplifier 13 is also applied to a carrier disappearance detector 17, which consists of a peak detector for detecting the presence and absence of the carrier and a delay circuit for delaying only the recovery time of the peak detection output signal. This delay circuit is used for compensating for the delay of the burst noise to the carrier disappearance timing due to the presence of a low pass filter (not shown) in the PM detecting operation.

When the FM detection is effected by an FM detection circuit using a known balanced differential multiplier and the FM detection output is converted into a PM detection signal by the low pass filter, the recovery time of the burst noise integrated by the low pass filter is retarded.

The low pass filter 19, to which the PM detection output is applied, detects the presence and absence of a stereo pilot signal of 5Hz, inserted by the PM modulation and controls the mute circuit 16, in order to change over between stereo and monaural operation and actuate a lamp connected to a terminal No. 6 for display. However, even in the case of stereo broadcasting in which the stereo pilot signal is detected, an AGC voltage V'_{AGC2} is applied to change to monaural reproduction if the intensity of the RF input field is weak and thus unsuitable for stereo reproduction.

The gain control voltage of the variable gain circuit 15 is generated in the following manner.

The AM detection signal at the emitter electrode of the AM detecting transistor Q_5 is converted into the AGC voltage V_{AGC2} by the AGC filter consisting of the resistor R_9 and the capacitor C_{106} connected to a terminal No. 5.

On the basis of the concept that the feedback D.C. voltage V_{NFB} in the first stage circuit of the limiter amplifier 13 is equal to the D.C. input voltage V_{DC} (the D.C. base voltage of the detecting transistor Q_5) of the AM detector 9', the D.C. feedback voltage is used for compensating for the offset voltage of the AGC voltage V_{AGC2} .

The D.C. feedback voltage V_{NFB} is level-shifted by an emitter follower level shift circuit consisting of a transistor Q_6 and a resistor R_{10} , in order to provide a level shift voltage V_{LS} from the emitter electrode of the transistor Q_6 . These voltages V_{AGC2} and V_{LS} are applied to a voltage comparator 18 to form a difference voltage

$V'_{AGC2} (= V_{AGC2} - V_{LS})$, which is used as a control voltage for the gain control circuit 15.

Accordingly, it is possible to change the difference voltage V'_{AGC2} to a control voltage proportional to the AM detection signal level not having the offset voltage, as indicated by dash line in Figure 2. Since the AM detecting transistor Q_5 and the emitter follower level shift transistor Q_6 are formed in the same monolithic semiconductor integrated circuit IC_2 , variance in the base-emitter voltage and temperature characteristic of both transistors Q_5 and Q_6 are equal to each other and are cancelled by the voltage comparator 18.

Hence, the offset voltage of the variable gain control voltage can be compensated for under non-adjustment, and deterioration of stereo separation due to temperature change and element variance can be prevented.

The AGC voltage V_{AGC1} of the signal source circuit IC_1 and the AGC voltage V_{AGC2} of the variable gain circuit for stereo demodulation are formed by the peculiar circuit, the interference electromagnetic wave in the signal source circuit can be suppressed. If the AGC voltage V_{AGC1} is increased by the signal amplitude of the RF amplifying stage in order to suppress the interference electromagnetic wave and if the variable gain circuit 15 is to be controlled by this AGC voltage V_{AGC1} , level matching becomes impossible between the sum signal and the difference signal so that stereo separation noticeably deteriorates.

By contrast, the variable gain circuit 15 is controlled by the AGC voltage V_{AGC2} , generated only by the AM detection output signal level formed by the detecting circuit 9'. Hence, the above problem does not occur.

A number of modifications to the above described circuits are possible. In a circuit in which a bias voltage is applied, via a bias resistor, to the base electrode of an AM detecting transistor for generating the sum signal, the above referred to bias voltage may be level-shifted by use of the similar emitter follower circuit as a D.C. voltage for compensating for the offset voltage at its detection output.

In an AM stereo receiver which consists of two chips of monolithic semiconductor integrated circuits, a variable gain control voltage generation circuit formed by the AM detector, the level shift circuit and the voltage comparator may be located in the signal source circuit.

If the AM detector 9 of the first circuit portion IC₁ is used as an AM detector for generating the sum signal, it is necessary to prepare two sets of AGC filters and to use one for the gain control of the RF stage and the other, for the variable gain control voltage. In this case, however, if the interference voltage preventing function is not added, only one AGC filter may be used.

Incidentally, since the monolithic semiconductor integrated circuit of the existing AM radio receiver can be used in the above described circuits, the cost of production can be reduced.



CLAIMS.

1. An AM stereo receiver for receiving stereo signals having an amplitude modulation sum signal component and a phase modulation difference signal component, the receiver including:
 - 5 (a) a signal source circuit for receiving such AM stereo signals, the output of which circuit when it receives such signals in use still contains the said signal components;
 - (b) an AM detector for generating a signal pro-
10 portional to said amplitude modulation sum signal component;
 - (c) a PM detector for generating a signal proportional to said phase modulation difference signal component;
 - (d) a variable gain circuit to which said phase modulation difference signal is applied;
 - 15 (e) a matrix circuit for generating stereo reproduction signals by composing said sum signal component and said difference signal component passed through said variable gain circuit;
 - (f) a detecting transistor formed in an integrated
20 circuit in the AM detector;
 - (g) means for obtaining an AGC voltage by smoothing said sum signal component obtained from the output of the detecting transistor;
 - (h) a level shift transistor formed in the integrated
25 circuit;
 - (i) means for applying a voltage virtually equal to the base D.C. input voltage of said detecting transistor to the base electrode of the level shift transistor, in order to provide a level shift voltage from the emitter electrode



of said level shift transistor; and

(j) means for controlling the gain of the variable gain control circuit by the difference voltage between the AGC voltage and the level shift voltage.

2. An AM stereo receiver according to Claim 1, further including:

(k) a limiter amplifier having its signal input terminal connected to the base electrode of the detecting transistor, its negative feedback input terminal connected to the base electrode of the level shift transistor and its output terminal connected to the input terminal of the PM detector.

3. An AM stereo receiver according to Claim 2, further including:

(1) a D.C. negative feedback circuit interposed between the output terminal and the negative feedback input terminal of said limiter amplifier in such a manner as to determine the voltage at the negative feedback input terminal of the limiter amplifier to be virtually equal to the D.C. base input voltage of the detecting transistor.

4. An AM stereo receiver according to any one of the preceding claims, wherein said signal source circuit includes an RF amplifier stage, a frequency convertor stage, an IF amplifier stage, a second AM detector, an AGC filter for controlling the gains of said RF amplifier stage and said IF amplifier stage by smoothing the detection output signal of the second AM detector and a voltage comparator for comparing and detecting a signal amplitude value of said RF amplifier stage with a reference value, so that when the signal amplitude value of said RF amplifier stage exceeds the reference voltage, its detection output signal is applied to the AGC filter to lower the gain of the RF



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amplifier stage.

5. An AM stereo receiver according to any one of the preceding claims, wherein the voltage applying means comprises a first differential amplifier comprising a pair of transistors, a constant current source connected to the commoned emitter electrodes, a second differential amplifier whose inputs are connected to respective collector electrodes of the transistors of the first differential amplifier; and a buffer amplifier which feeds back the output from the second differential amplifier to the base electrode of the level shift transistor and to the base electrode of one of the transistors of the first differential amplifier.

6. An AM stereo receiver according to any one of the preceding claims, wherein the variable gain circuit controlling means comprises a voltage comparator which receives on one input, the level shifted voltage from the level shift transistor, and on the other input an output from the detecting transistor, the comparison between these two voltages being used as a control voltage for controlling the variable gain circuit.

7. An AM stereo receiver constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 3 of the accompanying drawings.
