CLAIMS

1. A semiconductor device comprising:

M (M represents an integer of 3 or larger) semiconductor chips that are stacked; and

N through electrodes (N represents an integer of 2 or larger) for channels that are embedded in the semiconductor chips to connect electrically the semiconductor chips in a direction of stacking, wherein

connection destinations of the through electrodes are exchanged between one or more upper and lower layers of the semiconductor chips,

the M semiconductor chips include a first semiconductor chip, a second semiconductor chip, and a third semiconductor chip,

the first semiconductor chip includes:

a first through electrode; and

a second through electrode,

the second semiconductor chip includes:

a third through electrode disposed on a location not corresponding to the second through electrode, the third through electrode being electrically connected to the second through electrode; and

a fourth through electrode disposed on a location not corresponding to the first through electrode, the fourth through electrode being electrically connected to the first through electrode,

the third semiconductor chip includes:

a fifth through electrode disposed on a location not corresponding to the fourth through electrode, the fifth through electrode being electrically connected to the fourth through electrode; and

a sixth through electrode disposed on a location

not corresponding to the third through electrode, the sixth through electrode being electrically connected to the third through electrode,

the second semiconductor chip is stacked on the first semiconductor chip,

the third semiconductor chip is stacked on the second semiconductor chip,

the first semiconductor chip further includes:

a first wiring layer that electrically connects the first through electrode to the fourth through electrode; and

a second wiring layer that electrically connects the second through electrode to the third through electrode,

the second semiconductor chip further includes:

a third wiring layer that electrically connects the third through electrode to the sixth through electrode; and

a fourth wiring layer that electrically connects the fourth through electrode to the fifth through electrode.

2. The semiconductor device according to claim 1, wherein

the first semiconductor chip further includes:

a first internal circuit and

a first interface unit that electrically connects the second through electrode to the first internal circuit.

3. The semiconductor device according to claim 2, wherein

the N channels include a first channel and a second channel,

the first through electrode, the fourth through electrode, and the fifth through electrode correspond to the first channel,

the second through electrode, the third through

electrode, and the sixth through electrode correspond to the second channel,

in the first semiconductor chip, the first interface unit forms the second channel for the first semiconductor chip.

4. The semiconductor device according to claim 3, wherein

the first interface unit includes a first AND circuit that takes in a first signal for the second channel according to a first internal enable signal.

5. The semiconductor device according to claim 4, wherein

the first semiconductor chip further includes a first logic circuit that generates the first internal enable signal based on a chip address and chip identification information.

6. The semiconductor device according to claim 1, further comprising a controller that controls the semiconductor chips, wherein

the controller includes a channel control unit that controls the number of channels achieved by the N through electrodes.

7. The semiconductor device according to claim 6, wherein

the channel control unit controls the number of the channels by inputting a same signal into two or more of the N through electrodes or by inputting different signals into the N through electrodes.

8. The semiconductor device according to claim 7, wherein,

in order to operate the M semiconductor chips with K (K represents an integer of equal to or smaller than M)

channels, the channel control unit divides the N through electrodes into K groups, inputs a same signal into a same group, and inputs different signals into different groups.

9. The semiconductor device according to claim 6, wherein the controller controls the number of assignments of chip enable signals for the N through electrodes.

10. The semiconductor device according to claim 6, wherein the controller is disposed on the top semiconductor chip or under the bottom semiconductor chip.

11. The semiconductor device according to claim 1, wherein the semiconductor chips are NAND memories.

12. The semiconductor device according to claim 1, wherein

the first semiconductor chip further includes:

a seventh through electrode; and

an eighth through electrode,

the second semiconductor chip further includes:

a ninth through electrode disposed on a location not corresponding to the eighth through electrode, the ninth through electrode being electrically connected to the eighth through electrode; and

a tenth through electrode disposed on a location not corresponding to the seventh through electrode, the tenth through electrode being electrically connected to the seventh through electrode,

the third semiconductor chip further includes:

an eleventh through electrode disposed on a location not corresponding to the tenth through electrode, the eleventh through electrode being electrically connected to the tenth through electrode; and

a twelfth through electrode disposed on a location not corresponding to the ninth through electrode, the twelfth through electrode being electrically connected to the ninth through electrode.

13. The semiconductor device according to claim 12, wherein

the first semiconductor chip further includes:

a first internal circuit and

a first interface unit that electrically connects the second through electrode to the first internal circuit, and

the second semiconductor chip further includes:

a second internal circuit and

a second interface unit that electrically connects the ninth through electrode to the second internal circuit,

the third semiconductor chip further includes:

a third internal circuit and

a third interface unit that electrically connects the eleventh through electrode to the third internal circuit.

14. The semiconductor device according to claim 13, wherein

the channels include a first channel, a second channel, a third channel, and a fourth channel,

the first through electrode, the fourth through electrode, and the fifth through electrode correspond to the first channel,

the second through electrode, the third through electrode, and the sixth through electrode correspond to the second channel,

the seventh through electrode, the tenth through electrode, and the eleventh through electrode correspond to the third channel, and

the eighth through electrode, the ninth through electrode, and the twelfth through electrode correspond to the fourth channel.

15. The semiconductor device according to claim 14, wherein

the first interface unit includes a first AND circuit that takes in a first signal for the second channel according to a first internal enable signal,

the second interface unit includes a second AND circuit that takes in a second signal for the fourth channel according to a second internal enable signal,

the third interface unit includes a third AND circuit that takes in a third signal for the third channel according to a third internal enable signal.

16. The semiconductor device according to claim 15, wherein

the first semiconductor chip further includes a first logic circuit that generates the first internal enable signal based on a chip address and chip identification information, and

the second semiconductor chip further includes a second logic circuit that generates the second internal enable signal based on a chip address and chip identification information,

the third semiconductor chip further includes a third logic circuit that generates the third internal enable signal based on a chip address and chip identification information.

17. The semiconductor device according to claim 12, further comprising a controller that controls the semiconductor chips, wherein

the controller includes a channel control unit that controls the number of channels achieved by the N through electrodes.

18. The semiconductor device according to claim 12, wherein

the first through electrode, the second through electrode, the seventh through electrode, and the eighth through electrode are disposed in square form, and

the third through electrode, the fourth through electrode, the ninth through electrode, and the tenth through electrode are disposed in square form,

the fifth through electrode, the sixth through electrode, the eleventh through electrode, and the twelfth through electrode are disposed in square form.

19. The semiconductor device according to claim 1, wherein

the first through electrode, the second through electrode, the first wiring layer, and the second wiring layer form square layout shape when seen through in a direction perpendicular to a surface of the first semiconductor chip,

the third through electrode, the fourth through electrode, the third wiring layer, and the fourth wiring layer form square layout shape when seen through in the direction.