

## ABSTRACT

A vertical memory device includes gate electrode structures, channels, first to third division patterns, and a first support layer. The gate electrode structure includes gate electrodes stacked in a first direction, and extends in a second direction. The gate electrode structures are spaced apart from one another in a third direction. The first division pattern extends in the second direction between the gate electrode structures. The second and third division patterns are alternately disposed in the second direction between the gate electrode structures. The first support layer is on the gate electrode structures at substantially the same height as upper portions of the first and second division patterns, and contacts the upper portions of the first and second division patterns. The upper portions of the first and second division patterns are arranged in a zigzag pattern in the second direction in a plan view.

FIG. 1