

SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Korean Patent Application No. 10-2017-0119813,
5 filed on September 18, 2017 in the Korean Intellectual Property Office (KIPO), the contents
of which are herein incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] Example embodiments relate to semiconductor devices. More particularly,
10 example embodiments relate to semiconductor devices having vertically stacked channels.

BACKGROUND

[0003] As the distance between channels in a multi-bridge-channel MOSFET (MBCFET)
decreases, it may be difficult to control the thickness of a barrier layer to obtain a target
15 threshold voltage of the MBCFET. It is desired to have a barrier layer having a relatively
thicker thickness in an MBCFET having a relatively high threshold voltage, and thus, there
may not be sufficient space for forming a workfunction metal layer, and a target threshold
voltage may not be obtained.

SUMMARY

20 **[0004]** Example embodiments provide a semiconductor device having good characteristics
to improve performance. More particularly, example embodiments provide a semiconductor
device having good aluminum diffusion prevention characteristics.

[0005] According to example embodiments, there is provided a semiconductor device.

The semiconductor device may include a first transistor and a second transistor. The first transistor may have a first threshold voltage, and include first channels on a substrate, first source/drain layers on the substrate, and a first gate structure surrounding the first channels. The first channels may be spaced apart from each other in a vertical direction on an upper surface of the substrate. The first source/drain layers may be connected to respective opposite sidewalls of the first channels. The first gate structure may include a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels. The second transistor may have a second threshold voltage greater than the first threshold voltage, and include second channels on the substrate, second source/drain layers on the substrate, and a second gate structure surrounding the second channels. The second channels may be spaced apart from each other in the vertical direction on the upper surface of the substrate. The second source/drain layers may be connected to respective opposite sidewalls of the second channels. The second gate structure may include a second gate insulation pattern, a second threshold voltage control pattern, and a second workfunction metal pattern sequentially stacked from a surface of each of the second channels. A thickness of the second threshold voltage control pattern in a direction perpendicular to the upper surface of the substrate may be equal to or less than a thickness of the first threshold voltage control pattern in the direction perpendicular to the upper surface of the substrate.

[0006] According to example embodiments, there is provided a semiconductor device. The semiconductor device may include a first transistor, a second transistor, and a third transistor. The first transistor may have a positive first threshold voltage, and include first channels on a first region of a substrate including the first region and a second region, first source/drain layers on the first region of the substrate, and a first gate structure surrounding

the first channels. The first channels may be spaced apart from each other in a vertical direction on an upper surface of the substrate. The first source/drain layers may be connected to respective opposite sidewalls of the first channels. The first gate structure may include a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels. The second transistor may have a positive second threshold voltage greater than the positive first threshold voltage, and include second channels on the first region of the substrate, second source/drain layers on the first region of the substrate, and a second gate structure surrounding the second channels. The second channels may be spaced apart from each other in the vertical direction on the upper surface of the substrate. The second source/drain layers may be connected to respective opposite sidewalls of the second channels. The second gate structure may include a second gate insulation pattern, a second threshold voltage control pattern, and a second workfunction metal pattern sequentially stacked from a surface of each of the second channels. The third transistor may have a negative third threshold voltage, and include third channels on the second region of the substrate, third source/drain layers on the substrate, and a third gate structure surrounding the third channels. The third channels may be spaced apart from each other in the vertical direction on the upper surface of the substrate. The third source/drain layers may be connected to respective opposite sidewalls of the third channels. The third gate structure may include a third gate insulation pattern and a third threshold voltage control pattern sequentially stacked from a surface of each of the third channels. The first threshold voltage control pattern may have a first pattern having a first material composition, the second threshold voltage control pattern may have a second pattern having a second material composition different from the first material composition, and the third threshold

voltage control pattern may have the first and second patterns.

[0007] According to example embodiments, there is provided a semiconductor device.

The semiconductor device may include first channels on a substrate, a first gate structure surrounding the first channels, second channels on the substrate, and a second gate structure

5 surrounding the second channels. The first channels may be spaced apart from each other in a vertical direction on an upper surface of the substrate. The first gate structure may include a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels.

The second channels may be spaced apart from each other in the vertical direction on the

10 upper surface of the substrate and may be spaced apart from the first channels in a horizontal direction parallel to the upper surface of the substrate. The second gate structure may include a second gate insulation pattern, a second threshold voltage control

pattern, and a second workfunction metal pattern sequentially stacked from a surface of each of the second channels. A second workfunction of the second gate structure may be

15 greater than a first workfunction of the first gate structure, and a thickness of the second threshold voltage control pattern may be equal to or less than a thickness of the first threshold voltage control pattern.

[0008] According to example embodiments, there is provided a semiconductor device.

The semiconductor device may include first channels on a substrate, a first gate structure

20 surrounding the first channels, second channels on the substrate, and a second gate structure surrounding the second channels. The first channels may be spaced apart from each other

in a vertical direction on an upper surface of the substrate. The first gate structure may include a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels.

The second channels may be spaced apart from each other in the vertical direction on the upper surface of the substrate and may be spaced apart from the first channels in a horizontal direction parallel to the upper surface of the substrate. The second gate structure may include a second gate insulation pattern, a second threshold voltage control pattern, and a second workfunction metal pattern sequentially stacked from a surface of each of the second channels. A second workfunction of the second gate structure may be greater than a first workfunction of the first gate structure, and a thickness in the vertical direction of a portion of the first work metal pattern between the first channels may be equal to or less than a thickness in the vertical direction of a portion of the second workfunction metal pattern between the second channels.

[0009] According to example embodiments, there is provided a semiconductor device. The semiconductor device may include first channels on a substrate, first source/drain layers on the substrate, and a first gate structure surrounding the first channels. The first channels may be spaced apart from each other in a vertical direction on an upper surface of the substrate. The first source/drain layers may be connected to respective opposite sidewalls of the first channels. The first gate structure may include a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels. A thickness in the vertical direction of a portion of the first work metal pattern between the first channels may be less than a thickness in a horizontal direction parallel to the upper surface of the substrate of a portion of the first workfunction metal pattern stacked from a sidewall of the first threshold voltage control pattern.

[0010] In the semiconductor device in accordance with example embodiments, even if the vertical distances between channels of the MBCFET decrease, the MBCFET may have a

target threshold voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

[0012] FIGS. 1, 2A, 2B, 3A and 3B are a plan view and cross-sectional views illustrating a first semiconductor device in accordance with example embodiments;

[0013] FIGS. 4 to 17 are plan views and cross-sectional views illustrating stages of a method of manufacturing a semiconductor device in accordance with example embodiments;

[0014] FIGS. 18 to 20 are cross-sectional views illustrating second to fourth semiconductor devices, respectively, in accordance with example embodiments;

[0015] FIGS. 21, 22, 23A and 23B are a plan view and cross-sectional views illustrating a fifth semiconductor device in accordance with example embodiments;

[0016] FIG. 24 is a cross-sectional view illustrating a sixth semiconductor device in accordance with example embodiments; and

[0017] FIGS. 25, 26, 27A and 27B are a plan view and cross-sectional views illustrating an eighth semiconductor device in accordance with example embodiments.

DETAILED DESCRIPTION

[0018] FIGS. 1, 2A, 2B, 3A and 3B are a plan view and cross-sectional views illustrating a first semiconductor device in accordance with example embodiments. Particularly, FIG. 1 is a plan view, FIGS. 2A and 2B are cross-sectional views taken along a line A-A' of FIG. 1, FIG. 3A is a cross-sectional view taken along lines B-B' and C-C' of FIG. 1, and FIG. 3B is

an enlarged cross-sectional view of regions X and Y of FIG. 3A.

[0019] Hereinafter, two directions substantially parallel to an upper surface of a substrate 100 and crossing each other may be referred to as first and second directions, respectively, and a direction substantially perpendicular to the upper surface of the substrate 100 may be referred to as a third direction.

[0020] Referring to FIGS. 1, 2A, 2B, 3A and 3B, the first semiconductor device may include first and second semiconductor patterns 126 and 128, first and second epitaxial layers 212 and 214, and first and second gate structures 282 and 284 on the substrate 100. The first semiconductor device may further include first and second active fins 102 and 104, an isolation pattern 130, first and second gate spacers 182 and 184, an inner spacer 200, and an insulation layer 220.

[0021] As used herein, the first semiconductor device may be in the form of, for example, a semiconductor chip or die, formed from a semiconductor wafer. The term “semiconductor device” as used herein may also refer to a semiconductor package, including a package substrate, one or more semiconductor chips, and an encapsulant.

[0022] The substrate 100 may include a semiconductor material, e.g., silicon, germanium, silicon-germanium, etc., or III-V semiconductor compounds, e.g., GaP, GaAs, GaSb, etc. In some embodiments, the substrate 100 may be a silicon-on-insulator (SOI) substrate, or a germanium-on-insulator (GOI) substrate.

[0023] The substrate 100 may include first and second regions I and II. The first region I may be a low voltage region to which a relatively low voltage may be applied, and the second region II may be a high voltage region to which a relatively high voltage may be applied.

[0024] The first and second active fins 102 and 104 may protrude from the first and second

regions I and II of the substrate 100, respectively, in the third direction, and each of the first and second active fins 102 and 104 may extend in the first direction. In the figures, according to exemplary embodiments, one first active fin 102 and one second active fin 104 are shown on the first and second regions I and II, respectively, however, the inventive
5 concepts are not limited thereto. Thus, a plurality of first active fins 102 may be spaced apart from each other in the second direction on the first region I, and a plurality of second active fins 104 may be spaced apart from each other in the second direction on the second region II.

[0025] Opposing sidewalls of the first and second active fins 102 and 104 may be covered
10 by the isolation pattern 130. The first and second active fins 102 and 104 may include substantially the same material as that of the substrate 100, and the isolation pattern 130 may include an oxide, e.g., silicon oxide.

[0026] Unless the context indicates otherwise, the terms first, second, third, etc., are used as labels to distinguish one element, component, region, layer or section from another
15 element, component, region, layer or section (that may or may not be similar). Thus, a first element, component, region, layer or section discussed below in one section of the specification (or claim) may be referred to as a second element, component, region, layer or section in another section of the specification (or another claim).

[0027] A plurality of first semiconductor patterns 126 may be formed at a plurality of
20 levels, respectively, to be spaced apart from each other in the third direction from an upper surface of the first active fin 102, and a plurality of second semiconductor patterns 128 may be formed at a plurality of levels, respectively, to be spaced apart from each other in the third direction from an upper surface of the second active fin 104. The levels at which the first and second semiconductor patterns 126 and 128 are formed may be positioned at the

same heights. In the figures, according to exemplary embodiments, each of the first and second semiconductor patterns 126 and 128 is shown at three levels, however, the inventive concepts may not be limited thereto. As illustrated in the exemplary figures, according to example embodiments, the lowermost first semiconductor pattern of the plurality of first semiconductor patterns 126 may be positioned in the third direction (vertical direction) from an upper surface of the first active fin 102 at the same height as the corresponding lowermost second semiconductor pattern of the plurality of second semiconductor patterns 128 in the third direction (vertical direction) from an upper surface of the second active fin 104. As illustrated in the exemplary figures, according to example embodiments, the uppermost first semiconductor pattern of the plurality of first semiconductor patterns 126 may be positioned in the third direction (vertical direction) from an upper surface of the first active fin 102 at the same height as the corresponding uppermost second semiconductor pattern of the plurality of second semiconductor patterns 128 in the third direction (vertical direction) from an upper surface of the second active fin 104. As illustrated in the exemplary figures, according to example embodiments, the middle first semiconductor pattern of the plurality of first semiconductor patterns 126 may be positioned in the third direction (vertical direction) from an upper surface of the first active fin 102 at the same height as the corresponding middle second semiconductor pattern of the plurality of second semiconductor patterns 128 in the third direction (vertical direction) from an upper surface of the second active fin 104.

[0028] In the figures, according to exemplary embodiments, only one first semiconductor pattern 126 is shown at each level on the first active fin 102 and only one second semiconductor pattern 128 is shown at each level on the second active fin 104, however, the inventive concepts may not be limited thereto. Thus, a plurality of first semiconductor

patterns 126 may be formed to be spaced apart from each other in the first direction at each level on the first active fin 102, and a plurality of second semiconductor patterns 128 may be formed to be spaced apart from each other in the first direction at each level on the second active fin 104.

5 **[0029]** In example embodiments, the first and second semiconductor patterns 126 and 128 may be nanosheets including a semiconductor material, e.g., silicon, germanium, etc. Alternatively, the first and second semiconductor patterns 126 and 128 may be nanowires including a semiconductor material.

[0030] In example embodiments, the first and second semiconductor patterns 126 and 128
10 may serve as channels of first and second transistors, respectively, which may be referred to as first and second channels, respectively.

[0031] The first epitaxial layer 212 may extend in the third direction from the upper surface of the first active fin 102, and may commonly contact respective sidewalls of the first semiconductor patterns 126 at the plurality of levels to be connected thereto. An
15 upper portion of the first epitaxial layer 212 may contact a lower sidewall of the first gate spacer 182. The second epitaxial layer 214 may extend in the third direction from the upper surface of the second active fin 104, and may commonly contact respective sidewalls of the second semiconductor patterns 128 at the plurality of levels to be connected thereto. An upper portion of the second epitaxial layer 214 may contact a lower sidewall of the
20 second gate spacer 184.

[0032] In example embodiments, each of the first and second epitaxial layers 212 and 214 may include single crystalline silicon carbide doped with n-type impurities or single crystalline silicon doped with n-type impurities, and thus may serve as a source/drain layer of an NMOS transistor. Alternatively, each of the first and second epitaxial layers 212 and

214 may include single crystalline silicon-germanium doped with p-type impurities, and thus may serve as a source/drain layer of a PMOS transistor. The first and second epitaxial layers 212 and 214 may serve as first and second source/drain layers, respectively.

[0033] The first and second gate structures 282 and 284 may be formed on the first and second regions I and II, respectively, of the substrate 100, and may surround the first and second semiconductor patterns 126 and 128, respectively. In the figures, according to exemplary embodiments, the first gate structure 282 is shown to cover the first semiconductor pattern 126 on one first active fin 102, and the second gate structure 284 is shown to cover the second semiconductor pattern 128 on one second active fin 104, however, the inventive concepts may not be limited thereto. For example, each of the first and second gate structures 282 and 284 may extend in the second direction, and the first gate structure 282 may cover the first semiconductor patterns 126 on a plurality of first active fins 102, and the second gate structure 284 may cover the second semiconductor patterns 128 on a plurality of second active fins 104.

[0034] In the figure, according to exemplary embodiments, one first gate structure 282 is shown on the first region I of the substrate 100, and one second gate structure 284 is shown on the second region II of the substrate 100, however, the inventive concepts may not be limited thereto. Thus, a plurality of first gate structures 282 may be formed on the first region I of the substrate 100, and a plurality of second gate structures 284 may be formed on the second region II of the substrate 100.

[0035] The first and second gate spacers 182 and 184 may cover upper sidewalls in the first direction and sidewalls in the second direction of the first and second gate structures 282 and 284, respectively, and the inner spacer 200 may be formed between lower sidewalls in the first direction of the first and second gate structures 282 and 284, respectively, and the

first and second epitaxial layers 212 and 214, respectively.

[0036] The first and second gate spacers 182 and 184 may include a nitride, e.g., silicon nitride, the inner spacer 200 may include an oxide, e.g., silicon oxide. In an example embodiment, a thickness of the inner spacer 200 in the first direction may be equal to that of each of the first and second gate spacers 182 and 184 in the first direction.

[0037] The first gate structure 282 may include a first gate insulation pattern, a first threshold voltage control pattern 262, and a first workfunction metal pattern 272 sequentially stacked from a surface of each of the first semiconductor patterns 126, and the first gate insulation pattern may include a first interface pattern 242 and a first high-k dielectric pattern 252 sequentially stacked.

[0038] The first interface pattern 242 may be formed on the upper surface of the first active fin 102 and the surfaces of the first semiconductor patterns 126, and the first high-k dielectric pattern 252 may be formed on a surface of the first interface pattern 242, an inner sidewall of the inner spacer 200, and an inner sidewall of the first gate spacer 182. The first threshold voltage control pattern 262 may be formed on the first high-k dielectric pattern 252, and the first workfunction metal pattern 272 may fill a space between the first semiconductor patterns 126 spaced apart from each other in the third direction and a space defined by an inside of the first gate spacer 182 on an uppermost one of the first semiconductor patterns 126.

[0039] The first interface pattern 242 may include an oxide, e.g., silicon oxide, and the first high-k dielectric pattern 252 may include, e.g., hafnium oxide, tantalum oxide, zirconium oxide, etc.

[0040] The first threshold voltage control pattern 262 may include, e.g., titanium nitride, titanium oxynitride, titanium oxycarbonitride, titanium silicon nitride, titanium silicon

oxynitride, titanium aluminum oxynitride, tantalum nitride, tantalum oxynitride, tantalum aluminum nitride, tantalum aluminum oxynitride, tungsten nitride, tungsten carbonitride, aluminum oxide, etc. The first workfunction metal pattern 272 may include, e.g., titanium aluminum, titanium aluminum oxide, titanium aluminum carbide, titanium aluminum nitride, titanium aluminum oxynitride, titanium aluminum carbonitride, titanium aluminum oxycarbonitride, etc.

[0041] The first gate structure 282 together with the first epitaxial layer 212 serving as a source/drain layer and the first semiconductor pattern 126 serving as a channel may form a first transistor. The first transistor may be an NMOS transistor or a PMOS transistor according to the conductivity type of the impurities doped in the first epitaxial layer 212. The first transistor may include the plurality of first semiconductor patterns 126 sequentially stacked in the third direction, and thus may be an MBCFET.

[0042] The first transistor may have a first threshold voltage, which may be obtained by the first workfunction metal pattern 272 and the first threshold voltage control pattern 262.

For example, when the first workfunction metal pattern 272 includes titanium aluminum carbide and the first threshold voltage control pattern 262 includes titanium nitride, the first threshold voltage control pattern 262 may prevent or reduce the diffusion of aluminum in the first workfunction metal pattern 272, and the degree of diffusion of aluminum may be controlled by the thickness of the first threshold voltage control pattern 262 so that the first threshold voltage may be obtained.

[0043] The second gate structure 284 may include a second gate insulation pattern, a second threshold voltage control pattern 264, and a second workfunction metal pattern 274 sequentially stacked from a surface of each of the second semiconductor patterns 128, and the second gate insulation pattern may include a second interface pattern 244 and a second

high-k dielectric pattern 254 sequentially stacked.

[0044] The second interface pattern 244, the second high-k dielectric pattern 254, and the second workfunction metal pattern 274 may include substantially the same material compositions as those of the first interface pattern 242, the first high-k dielectric pattern 252, and the first workfunction control pattern 264, respectively. The second threshold voltage control pattern 264 may include the above-mentioned materials of the first threshold voltage control pattern 262.

[0045] Terms such as “same,” “equal,” “planar,” or “coplanar,” as used herein when referring to orientation, layout, location, shapes, sizes, amounts, or other measures do not necessarily mean an exactly identical orientation, layout, location, shape, size, amount, or other measure, but are intended to encompass nearly identical orientation, layout, location, shapes, sizes, amounts, or other measures within acceptable variations that may occur, for example, due to manufacturing processes. The term “substantially” may be used herein to emphasize this meaning, unless the context or other statements indicate otherwise. For example, items described as “substantially the same,” “substantially equal,” or “substantially planar,” may be exactly the same, equal, or planar, or may be the same, equal, or planar within acceptable variations that may occur, for example, due to manufacturing processes.

[0046] The second gate structure 284 together with the second epitaxial layer 214 serving as a source/drain layer and the second semiconductor pattern 128 serving as a channel may form a second transistor. The second transistor may be an NMOS transistor or a PMOS transistor according to the conductivity type of the impurities doped in the second epitaxial layer 214. The second transistor may include the plurality of second semiconductor patterns 128 sequentially stacked in the third direction, and thus may be an MBCFET.

[0047] The second transistor may have a second threshold voltage, which may be obtained by the second workfunction metal pattern 274 and the second threshold voltage control pattern 264.

[0048] In example embodiments, each of the first and second channels may be a nanosheet, and each of a distance between the first channels and a distance between the second channels is equal to or less than about 10nm.

[0049] In example embodiments, each of the first and second transistors may be an NMOS transistor. The second threshold voltage of the second transistor may be higher than the first threshold voltage of the first transistor. A second workfunction of the second gate structure 284 including the second workfunction metal pattern 274 and the second threshold voltage control pattern 264 may be higher than that of the first gate structure 282 including the first workfunction metal pattern 272 and the first threshold voltage control pattern 262. Thus, when the first and second workfunction metal patterns 272 and 274 include the same material compositions and the first and second threshold voltage control patterns 262 and 264 include the same material compositions, generally, a thickness of the second threshold voltage control pattern 264 is more than that of the first threshold voltage control pattern 262.

[0050] As illustrated in FIG. 3B, in example embodiments, the first and second threshold voltage control patterns 262 and 264 may include different material compositions, and a fifth thickness T5 of the second threshold voltage control pattern 264 may be equal to or less than a fourth thickness T4 of the first threshold voltage control pattern 262. As illustrated in FIG. 3B, the fourth thickness T4 of the first threshold voltage control pattern 262 may be uniform in a direction perpendicular to an upper surface of the substrate 100 and in a direction parallel to the upper surface of the substrate 100. Likewise, the fifth

thickness T5 of the second threshold voltage control pattern 264 may be uniform in a direction perpendicular to an upper surface of the substrate 100 and in a direction parallel to the upper surface of the substrate 100. In an example embodiment, the first and second threshold voltage control patterns 262 and 264 may include titanium nitride and titanium silicon nitride, respectively, and the characteristics of the second threshold voltage control pattern 264 including titanium silicon nitride for preventing the diffusion of aluminum may be greater than those of the first threshold voltage control pattern 262 including titanium nitride for preventing the diffusion of aluminum. Accordingly, even if the second threshold voltage control pattern 264 of the second transistor has a relatively thinner thickness compared to that of the first threshold voltage control pattern 262, the relatively high threshold voltage may be obtained by the second threshold voltage control pattern 264.

[0051] In example embodiments, a distance between neighboring ones of the first semiconductor patterns 126 sequentially stacked in the third direction or a distance between neighboring ones of the second semiconductor patterns 128 sequentially stacked in the third direction may be less than about 10nm. As the distance between channels sequentially stacked in the third direction decreases, the threshold voltage control pattern and the workfunction metal pattern may not have sufficiently thick thicknesses between the channels. For example, in order to obtain the second threshold voltage having a relatively high value, conventionally, the second threshold voltage control pattern 264 may need a relatively thicker thickness, and thus there may not be sufficient spaces for forming the second workfunction metal pattern 274.

[0052] However, in example embodiments, the second threshold voltage control pattern 264 may include a material having relatively high diffusion prevention characteristics when compared to those of the first threshold voltage control pattern 262, and thus a relatively

high threshold voltage may be obtained even with a relatively thinner thickness compared to that of the first threshold voltage control pattern 262, and the second workfunction metal pattern 274 may have a sufficiently thicker thickness compared to that of the first workfunction metal pattern 272.

- 5 **[0053]** In FIG. 2A, a third thickness T3 in a vertical direction of a portion of the second workfunction metal pattern 274 between the second semiconductor patterns 128 in the second transistor is greater than a second thickness T2 in the vertical direction of a portion of the first workfunction metal pattern 272 between the first semiconductor patterns 126 in the first transistor.
- 10 **[0054]** As the distance between the channels decreases, the second thickness T2 in the vertical direction of the portion of the first workfunction metal pattern 272 between the first semiconductor patterns 126 in the first transistor is less than twice the first thickness T1 in a horizontal direction of a portion of the first workfunction metal pattern 272 stacked in the second direction from the sidewall of the first threshold voltage control pattern 262 in FIG.
- 15 2A. FIG. 2B shows the second thickness T2 in the vertical direction of the portion of the first workfunction metal pattern 272 between the first semiconductor patterns 126 in the first transistor is less than the first thickness T1 in the horizontal direction of the portion of the first workfunction metal pattern 272 stacked in the second direction from the sidewall of the first threshold voltage control pattern 262.
- 20 **[0055]** The third thickness T3 in the vertical direction of the portion of the second workfunction metal pattern 274 between the second semiconductor patterns 128 in the second transistor is equal to or more than twice the first thickness T1 in the horizontal direction of a portion of the second workfunction metal pattern 274 stacked in the second direction from the sidewall of the second threshold voltage control pattern 264 in FIG. 2A.

[0056] The insulation layer 220 may surround the sidewalls of the first and second gate spacers 182 and 184 and cover the first and second epitaxial layers 212 and 214. The insulation layer 220 may include an oxide, e.g., silicon oxide.

[0057] The first semiconductor device may further include contact plugs (not shown), wirings (not shown) or wiring patterns, etc., electrically connected to the first and second epitaxial layers 212 and 214. Contact plugs may be, for example, conductive plugs formed of a conductive material such as a metal. The wiring patterns described above may also be formed of a conductive material, for example, a metal, and each may be formed horizontally within the die.

[0058] FIGS. 4 to 17 are plan views and cross-sectional views illustrating stages of a method of manufacturing a semiconductor device in accordance with example embodiments. Particularly, FIGS. 4, 6, 8, 11, 14, and 16 are plan views, and FIGS. 5, 7, 9-10, 12-13, 15, and 17 are cross-sectional views.

[0059] FIGS. 5, 7, and 9 are cross-sectional views taken along lines A-A' of corresponding plan views, respectively, FIGS. 10, 12, 13, 15, and 17 are cross-sectional views taken along lines B-B' of corresponding plan views, respectively.

[0060] Referring to FIGS. 4 and 5, a sacrificial layer 110 and a semiconductor layer 120 may be alternately stacked on a substrate 100 including first and second regions I and II.

[0061] In the figures, according to exemplary embodiments, three sacrificial layers 110 and three semiconductor layers 120 are shown to be formed on the substrate 100, however, the inventive concepts may not be limited thereto.

[0062] The sacrificial layer 110 may include a material having an etching selectivity with respect to the substrate 100 and the semiconductor layer 120, which may include, e.g., silicon-germanium.

[0063] Referring to FIGS. 6 and 7, a photoresist pattern may be formed on an uppermost one of the semiconductor layers 120 to extend in the first direction, and the semiconductor layers 120, the sacrificial layers 110, and an upper portion of the substrate 100 may be etched using the photoresist pattern as an etching mask.

5 **[0064]** Thus, a first active fin 102, a first sacrificial line 112, and a first semiconductor line 122 each of which may extend in the first direction may be formed on the first region I of the substrate 100, and a second active fin 104, a second sacrificial line 114, and a second semiconductor line 124 each of which may extend in the first direction may be formed on the second region II of the substrate 100.

10 **[0065]** After removing the photoresist pattern, an isolation pattern 130 may be formed on the first and second regions I and II of the substrate 100 to cover sidewalls of the first and second active fins 102 and 104.

[0066] Hereinafter, the first sacrificial lines 112 and the first semiconductor lines 122, each of which may extend in the first direction, sequentially stacked on an upper surface of the first active fin 102 may be referred to as a first structure, and the second sacrificial lines 114 and the second semiconductor lines 124, each of which may extend in the first direction, sequentially stacked on an upper surface of the second active fin 104 may be referred to as a second structure.

20 **[0067]** In example embodiments, a plurality of first structures may be formed to be spaced apart from each other in the second direction on the first region I of the substrate 100, and a plurality of second structures may be formed to be spaced apart from each other in the second direction on the second region II of the substrate 100.

[0068] Referring to FIGS. 8 to 10, a first dummy gate structure 172 may be formed on the first region I of the substrate 100 to partially cover the first structure and the isolation

pattern 130, and a second dummy gate structure 174 may be formed on the second region II of the substrate 100 to partially cover the second structure and the isolation pattern 130.

[0069] Particularly, a dummy gate insulation layer, a dummy gate electrode layer, and a dummy gate mask layer may be sequentially formed on the substrate 100 having the first and second structures and the isolation pattern 130 thereon, a photoresist pattern may be formed on the dummy gate mask layer, and the dummy gate mask layer may be etched using the photoresist pattern as an etching mask to form first and second dummy gate masks 162 and 164 on the first and second regions I and II, respectively, of the substrate 100. The dummy gate insulation layer may include an oxide, e.g., silicon oxide, the dummy gate electrode layer may include, e.g., polysilicon, and the dummy gate mask layer may include a nitride, e.g., silicon nitride.

[0070] The dummy gate electrode layer and the dummy gate insulation layer may be etched using the first and second dummy gate masks 162 and 164 as an etching mask to form a first dummy gate electrode 152 and a first dummy gate insulation pattern 142, respectively, on the first region I of the substrate 100 and to form a second dummy gate electrode 154 and a second dummy gate insulation pattern 144, respectively, on the second region II of the substrate 100.

[0071] The first dummy gate insulation pattern 142, the first dummy gate electrode 152, and the first dummy gate mask 162 sequentially stacked on the first active fin 102 and a portion of the isolation pattern 130 adjacent thereto may form the first dummy gate structure 172, and the second dummy gate insulation pattern 144, the second dummy gate electrode 154, and the second dummy gate mask 164 sequentially stacked on the second active fin 104 and a portion of the isolation pattern 130 adjacent thereto may form the second dummy gate structure 174.

[0072] In example embodiments, the first and second dummy gate structures 172 and 174 may extend in the second direction to cover sidewalls in the second direction of the first and second structures, respectively.

[0073] First and second gate spacers 182 and 184 may be formed on sidewalls of the first and second dummy gate structures 172 and 174, respectively.

[0074] Particularly, a gate spacer layer may be formed on the substrate 100 having the first and second structures, the isolation pattern 130, and the first and second dummy gate structures 172 and 174 thereon, and may be anisotropically etched to form the first and second gate spacers 182 and 184, respectively.

[0075] Referring to FIGS. 11 and 12, the first and second structures may be etched using the first and second dummy gate structures 172 and 174, and the first and second gate spacers 182 and 184 as an etching mask to form third and fourth structures, respectively.

[0076] The third structure may include first sacrificial patterns 116 and first semiconductor patterns 126 alternately stacked on the upper surface of the first active fin 102 on the first region I of the substrate 100, and a plurality of third structures may be formed to be spaced apart from each other in each of the first and second directions. Likewise, the fourth structure may include second sacrificial patterns (not shown) and second semiconductor patterns 128 (refer to FIGS. 2A and 3A) alternately stacked on the upper surface of the second active fin 104 on the second region II of the substrate 100, and a plurality of fourth structures may be formed to be spaced apart from each other in each of the first and second directions.

[0077] Hereinafter, the first dummy gate structure 172, the first gate spacer 182 on the sidewall of the first dummy gate structure 172, and the third structure may be referred to as a fifth structure, and the second dummy gate structure 174, the second gate spacer 184 on

the sidewall of the second dummy gate structure 174, and the fourth structure may be referred to as a sixth structure. In example embodiments, a plurality of fifth structures may be formed to be spaced apart from each other in each of the first and second directions, and a plurality of sixth structures may be formed to be spaced apart from each other in each of the first and second directions. A first opening 190 may be formed between neighboring ones of the fifth and sixth structures.

[0078] Referring to FIG. 13, opposite sidewalls in the first direction of the first sacrificial patterns 116 and the second sacrificial patterns exposed by the first opening 190 may be etched to form recesses, and an inner spacer 200 may be formed to fill each of the recesses.

[0079] In example embodiments, the recesses may be formed by a wet etching process on the first sacrificial patterns 116 and the second sacrificial patterns. The inner spacer 200 may be formed by a deposition process, e.g., a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, etc.

[0080] In an example embodiment, the inner spacer 200 may have a thickness in the first direction substantially equal to a thickness in the first direction of each of the first and second gate spacers 182 and 184.

[0081] Referring to FIGS. 14 and 15, first and second epitaxial layers 212 and 214 may be formed on upper surfaces of the first and second active fins 102 and 104, respectively, of the substrate 100 exposed by the first opening 190.

[0082] In example embodiments, the first and second epitaxial layers 212 and 214 may be formed by a selective epitaxial growth (SEG) process using the exposed upper surfaces of the first and second active fins 102 and 104 by the first opening 190 as a seed.

[0083] In example embodiments, the SEG process may be performed using a silicon source gas such as disilane (Si_2H_6) and a carbon source gas such as SiH_3CH_3 , to form a

single crystalline silicon carbide (SiC) layer. In an example embodiment, the SEG process may be performed using only the silicon source gas such as disilane (Si_2H_6), to form a single crystalline silicon layer.

[0084] Alternatively, the SEG process may be performed, using a silicon source gas such as dichlorosilane (SiH_2Cl_2) and a germanium source gas such as germane (GeH_4), to form a single crystalline silicon germanium (SiGe) layer.

[0085] In example embodiments, the first and second epitaxial layers 212 and 214 may be formed on sidewalls in the first direction of the fifth and sixth structures, respectively. In example embodiments, the first and second epitaxial layers 212 and 214 may contact sidewalls of the third and fourth structures, respectively, and further grow to contact sidewalls of the first and second gate spacers 182 and 184, respectively, on the third and fourth structures, respectively.

[0086] In some embodiments, the first and second epitaxial layers 212 and 214 may be formed by a laser epitaxial growth (LEG) process or a solid phase epitaxy (SPE) process.

[0087] The first and second epitaxial layers 212 and 214 may serve as source/drain layers of the first and second transistors, respectively. An impurity doping process and a heat treatment process may be further performed on the first and second epitaxial layers 212 and 214. For example, when the first and second epitaxial layers 212 and 214 include silicon carbide or silicon, n-type impurities may be doped therein and a heat treatment may be performed to form a source/drain layer of an NMOS transistor. When the first and second epitaxial layers 212 and 214 include silicon-germanium, p-type impurities may be doped therein and a heat treatment may be performed to form a source/drain layer of a PMOS transistor.

[0088] Referring to FIGS. 16 and 17, an insulation layer 220 may be formed on the

substrate 100 to cover the fifth and sixth structures and the first and second epitaxial layers 212 and 214, and may be planarized until upper surfaces of the first and second dummy gate electrodes 152 and 154 of the fifth and sixth structures, respectively, may be exposed. During the planarization process, the first and second dummy gate masks 162 and 164 may
5 be also removed, and upper portions of the first and second gate spacers 182 and 184 may be removed.

[0089] The planarization process may be performed by a chemical mechanical polishing (CMP) process and/or an etch back process.

[0090] The exposed first and second dummy gate electrodes 152 and 154 and the first and
10 second dummy gate insulation patterns 142 and 144 may be removed to form a second opening 232 exposing an inner sidewall of the first gate spacer 182, an inner sidewall of the inner spacer 200, surfaces of the first semiconductor patterns 126, and the upper surface of the first active fin 102, and to form a third opening 234 exposing an inner sidewall of the second gate spacer 184, the inner sidewall of the inner spacer 200, surfaces of the second
15 semiconductor patterns 128, and the upper surface of the second active fin 104.

[0091] Referring to FIGS. 1 to 3 again, first and second gate structures 282 and 284 may be formed on the first and second regions I and II, respectively, of the substrate 100 to fill the second and third openings 232 and 234, respectively.

[0092] Particularly, a thermal oxidation process may be performed on the upper surfaces of
20 the first and second active fins 102 and 104 and the surfaces of the first and second semiconductor patterns 126 and 128 exposed by the second and third openings 232 and 234, respectively, to form first and second interface patterns 242 and 244, respectively, and a high-k dielectric layer and a first threshold voltage control layer may be sequentially formed on surfaces of the first and second interface patterns 242 and 244, the inner sidewall of the

inner spacer 200, the inner sidewalls of the first and second gate spacers 182 and 184, and an upper surface of the insulation layer 220.

[0093] A first mask may be formed to cover the first region I of the substrate 100, and a portion of the first threshold voltage control layer on the second region II of the substrate 100 may be etched using the first mask as an etching mask to expose a portion of the high-k dielectric layer on the second region II of the substrate 100. Thus, the first threshold voltage control layer may remain on the first region I of the substrate 100.

[0094] A second threshold voltage control layer may be formed on the first threshold voltage control layer remaining on the first region I of the substrate 100 and the exposed portion of the high-k dielectric layer on the second region II of the substrate 100. A second mask may be formed to cover the second region II of the substrate 100, and a portion of the second threshold voltage control layer on the first region I of the substrate 100 may be etched using the second mask as an etching mask to expose the first threshold voltage control layer on the first region I of the substrate 100. Thus, the second threshold voltage control layer may remain on the second region II of the substrate 100.

[0095] A workfunction metal layer may be formed on the first and second threshold voltage control layers to fill the second and third openings 232 and 234.

[0096] The high-k dielectric layer, the first and second threshold voltage control layers, and the workfunction metal layer may be formed by, e.g., a CVD process, an ALD process, a physical vapor deposition (PVD) process, etc. The first and second interface patterns 242 and 244 may be also formed by a CVD process, an ALD process, etc., instead of the thermal oxidation process. In this case, the first and second interface patterns 242 and 244 may be also formed on the inner sidewall of the inner spacer 200 and the inner sidewalls of the first and second gate spacers 182 and 184.

[0097] In example embodiments, the first and second threshold voltage control layers may include different material compositions. The second threshold voltage control layer may have a thickness equal to or less than that of the first threshold voltage control layer.

[0098] The workfunction metal layer, the first and second threshold voltage control layers, and the high-k dielectric layer may be planarized until the upper surface of the insulation layer 20 may be exposed to form first and second workfunction metal patterns 272 and 274, first and second threshold voltage control patterns 262 and 264, and first and second high-k dielectric patterns 252 and 254, respectively.

[0099] The first interface pattern 242, the first high-k dielectric pattern 252, the first threshold voltage control pattern 262, and the first workfunction metal pattern 272 may form the first gate structure 282, and the second interface pattern 244, the second high-k dielectric pattern 254, the second threshold voltage control pattern 264, and the second workfunction metal pattern 274 may form the second gate structure 284.

[00100] FIGS. 18 to 20 are cross-sectional views illustrating second to fourth semiconductor devices, respectively, in accordance with example embodiments. Each of FIGS. 18 to 20 is an enlarged cross-sectional view of regions X and Y of FIG. 3A. The second to fourth semiconductor devices may be substantially the same as or similar to the first semiconductor device. Thus, like reference numerals refer to like elements, and detailed descriptions thereon are omitted herein.

[00101] Referring to FIG. 18, the second gate structure 284 may include a threshold voltage control pattern structure 304 having third and second threshold voltage control patterns 294 and 264 sequentially stacked such that the third threshold voltage control pattern 294 is conformally provided between the second high-k dielectric pattern 254 and the second threshold voltage control pattern 264.

[00102] In example embodiments, the third threshold voltage control pattern 294 may include the substantially the same material composition as that of the first threshold voltage control pattern 262, e.g., titanium nitride, and thus may have a double-layered structure including a titanium nitride layer and a titanium silicon nitride layer sequentially stacked.

5 **[00103]** In example embodiments, a sixth thickness T6 of the threshold voltage control pattern structure 304 may be equal to or less than the fourth thickness T4 of the first threshold voltage control pattern 262. However, the second threshold voltage control pattern 264 of the threshold voltage control pattern structure 304 may have improved diffusion prevention characteristics for a workfunction metal, and thus the second threshold
10 voltage higher than the first threshold voltage may be obtained. As illustrated in FIGS. 18, 19, and 20, the fourth thickness T4 of the first threshold voltage control pattern 262 may be uniform in a direction perpendicular to an upper surface of the substrate 100 and in a direction parallel to the upper surface of the substrate 100; the fifth thickness T5 of the second threshold voltage control pattern 264 may be uniform in a direction perpendicular to
15 an upper surface of the substrate 100 and in a direction parallel to the upper surface of the substrate 100; and the sixth thickness T6 of the threshold voltage control pattern structure 304 may be uniform in a direction perpendicular to an upper surface of the substrate 100 and in a direction parallel to the upper surface of the substrate 100.

[00104] In some embodiments, although not illustrated in the figures, the threshold
20 voltage control pattern structure 304 may include second and third threshold voltage control patterns 264 and 294 sequentially stacked such that the second threshold voltage control pattern 264 is conformally provided between the second high-k dielectric pattern 254 and the third threshold voltage control pattern 294.

[00105] Referring to FIG. 19, the second gate structure 284 may further include a second

dipole layer 314 having dipoles at an interface between the second interface pattern 244 and the second high-k dielectric pattern 254 such that an upper surface of the second dipole layer 314 is in contact with a lower surface of the second high-k dielectric pattern 254 and a lower surface of the second dipole layer 314 is in contact with an upper surface of the second interface pattern 244.

[00106] In example embodiments, the second dipole layer 314 may include aluminum oxide dipoles, and the second threshold voltage of the second transistor may move in a positive direction. Thus, in an NMOS transistor, even if the second threshold voltage control pattern 264 includes the substantially the same material composition as that of the first threshold voltage control pattern 262, e.g., titanium nitride, the second threshold voltage control pattern 264 may have the fifth thickness T5 less than the fourth thickness T4 of the first threshold voltage control pattern 262, and the relatively high second threshold voltage may be obtained.

[00107] For example, the second dipole layer 314 may be formed by forming and thermally treating a layer including aluminum oxide on the second high-k dielectric pattern 254, so that dipoles of aluminum oxide in the layer may move into the interface between the second interface pattern 244 and the second high-k dielectric pattern 254.

[00108] Referring to FIG. 20, the first gate structure 282 may further include a first dipole layer 312 having dipoles at an interface between the first interface pattern 242 and the first high-k dielectric pattern 252 such that an upper surface of the first dipole layer 312 is in contact with a lower surface of the first high-k dielectric pattern 252 and a lower surface of the first dipole layer 312 is in contact with an upper surface of the first interface pattern 242.

[00109] When an element is referred to as “contacting” or “in contact with” another element, there are no intervening elements present.

[00110] In example embodiments, the first dipole layer 312 may include lanthanum oxide dipoles, and the first threshold voltage of the first transistor may move in a negative direction. Thus, the fourth thickness T4 of the first threshold voltage control pattern 262 in FIG. 20 may be more than the fourth thickness T4 of the first threshold voltage control pattern 262 in FIG. 3B.

[00111] FIGS. 21, 22, 23A and 23B are a plan view and cross-sectional views illustrating a fifth semiconductor device in accordance with example embodiments. Particularly, FIG. 21 is a plan view, FIG. 22 is a cross-sectional view taken along a line D-D' of FIG. 21, FIG. 23A is a cross-sectional view taken along lines E-E', F-F' and G-G' of FIG. 21, and FIG. 23B is an enlarged cross-sectional view of regions U, V and W of FIG. 23A.

[00112] Referring to FIGS. 21, 22, 23A and 23B, the fifth semiconductor device may include third to fifth semiconductor patterns 422, 424 and 426, third to fifth epitaxial layers 512, 514 and 516, and third to fifth gate structures 582, 584 and 586 on a substrate 400. The fifth semiconductor device may further include third to fifth active fins 402, 404 and 406, an isolation pattern 430, third to fifth gate spacers 482, 484 and 486, an inner spacer 500, and an insulation layer 520.

[00113] The substrate 400 may include third to fifth regions III, IV and V. A relatively low voltage, a middle voltage, and a relatively high voltage may be applied to the third to fifth regions III, IV and V, respectively.

[00114] In example embodiments, the third to fifth semiconductor patterns 422, 424 and 426 may serve as channels of third to fifth transistors, respectively. Each of the third to fifth epitaxial layers 512, 514 and 516 may serve as a source/drain layer of an NMOS transistor or a PMOS transistor.

[00115] The third to fifth gate structures 582, 584 and 586 may be formed on the third to

fifth regions III, IV and V, respectively, of the substrate 400, and may surround the third to fifth semiconductor patterns 422, 424 and 426, respectively.

[00116] The third gate structure 582 may include a third gate insulation pattern, a fourth threshold voltage control pattern 562, and a third workfunction metal pattern 572 sequentially stacked from a surface of each of the third semiconductor patterns 422, and the third gate insulation pattern may include a third interface pattern 542 and a third high-k dielectric pattern 552 sequentially stacked. The third gate structure 582 together with the third epitaxial layer 512 and the third semiconductor pattern 422 may form the third transistor.

[00117] The fourth gate structure 584 may include a fourth gate insulation pattern, a fifth threshold voltage control pattern 564, and a fourth workfunction metal pattern 574 sequentially stacked from a surface of each of the fourth semiconductor patterns 424, and the fourth gate insulation pattern may include a fourth interface pattern 544 and a fourth high-k dielectric pattern 554 sequentially stacked. The fourth gate structure 584 together with the fourth epitaxial layer 514 and the fourth semiconductor pattern 424 may form the fourth transistor.

[00118] The fifth gate structure 586 may include a fifth gate insulation pattern, a sixth threshold voltage control pattern 566, and a fifth workfunction metal pattern 576 sequentially stacked from a surface of each of the fifth semiconductor patterns 426, and the fifth gate insulation pattern may include a fifth interface pattern 546 and a fifth high-k dielectric pattern 556 sequentially stacked. The fifth gate structure 586 together with the fifth epitaxial layer 516 and the fifth semiconductor pattern 426 may form the fifth transistor.

[00119] In example embodiments, each of the third to fifth transistors may be an NMOS

transistor, and third to fifth threshold voltages of the respective third to fifth transistors on the respective third to fifth regions III, IV and V may increase in this order. For example, the fifth threshold voltage may be greater than the fourth threshold voltage, and the fourth threshold voltage may be greater than the third threshold voltage. Additionally, third to fifth workfunctions of the respective third to fifth gate structures 582, 584 and 586 may increase in this order. For example, the fifth workfunction of the fifth gate structure 586 may be greater than the fourth workfunction of fourth gate structure 584, and the fourth workfunction of fourth gate structure 584 may be greater than the third workfunction of third gate structure 582.

[00120] In example embodiments, the fourth and fifth threshold voltage control patterns 562 and 564 may include substantially the same material composition, e.g., titanium nitride, and as the fourth threshold voltage is greater than the third threshold voltage, a twelfth thickness T12 of the fifth threshold voltage control pattern 564 may be greater than an eleventh thickness T11 of the fourth threshold voltage control pattern 562. The sixth threshold voltage control pattern 566 may include a different material composition from that of the fourth and fifth threshold voltage control patterns 562 and 564, e.g., titanium silicon nitride, and thus the fifth threshold voltage may be greater than the fourth threshold voltage, however, a thirteenth thickness T13 of the sixth threshold voltage control pattern 566 may be equal to or less than the twelfth thickness T12 of the fifth threshold voltage control pattern 564.

[00121] A ninth thickness T9 in the vertical direction of a portion of the fourth workfunction metal pattern 574 of the fourth transistor between the fourth semiconductor patterns 424 may be equal to or less than an eighth thickness T8 in the vertical direction of a portion of third workfunction metal pattern 572 of the third transistor between the third

semiconductor patterns 422. Also, the ninth thickness T9 in the vertical direction of a portion of the fourth workfunction metal pattern 574 of the fourth transistor between the fourth semiconductor patterns 424 may be equal to or less than a tenth thickness T10 in the vertical direction of a portion of fifth workfunction metal pattern 576 of the fifth transistor
5 between the fifth semiconductor patterns 426.

[00122] Additionally, the ninth thickness T9 in the vertical direction of the portion of the fourth workfunction metal pattern 574 of the fourth transistor between the fourth semiconductor patterns 424 may be less than twice a seventh thickness T7 in the horizontal direction of a portion of the fourth workfunction metal pattern 574 stacked from a sidewall
10 of the fifth threshold voltage control pattern 564 in the second direction.

[00123] FIG. 24 is a cross-sectional view illustrating a sixth semiconductor device in accordance with example embodiments. Particularly, FIG. 24 is an enlarged cross-sectional view of regions U, V and W of FIG. 24. The sixth semiconductor device may be substantially the same as or similar to the fifth semiconductor device, except for the
15 gate structure.

[00124] Referring to FIG. 24, the fifth gate structure 586 of the fifth transistor may further include a third dipole layer 616 having dipoles at an interface between the fifth interface pattern 546 and the fifth high-k dielectric pattern 556 such that an upper surface of the third dipole layer 616 is in contact with a lower surface of the fifth high-k dielectric pattern 556
20 and a lower surface of the third dipole layer 616 is in contact with an upper surface of the fifth interface pattern 546.

[00125] In example embodiments, the third dipole layer 616 may include aluminum oxide dipoles, and the fifth threshold voltage of the fifth transistor may move in a positive direction. Thus, in an NMOS transistor, even if the sixth threshold voltage control pattern

566 includes substantially the same material composition as that of the fifth threshold voltage control pattern 564, e.g., titanium nitride, the sixth threshold voltage control pattern 566 may have a thirteenth thickness T13 less than the twelfth thickness T12 of the fifth threshold voltage control pattern 564, and the relatively higher fifth threshold voltage may be obtained compared to the fourth threshold voltage.

[00126] FIGS. 25, 26, 27A and 27B are a plan view and cross-sectional views illustrating an eighth semiconductor device in accordance with example embodiments. Particularly, FIG. 25 is a plan view, FIG. 26 is a cross-sectional view taken along lines D-D' and H-H' of FIG. 25, FIG. 27A is a cross-sectional view taken along lines I-I', J-J' and K-K' of FIG. 25, and FIG. 27B is an enlarged cross-sectional view of regions U, V, W, R, S and T of FIG. 27A.

[00127] The eighth semiconductor device may further include a seventh semiconductor device on sixth to eighth regions VI, VII and VIII of the substrate 400 in addition to the sixth semiconductor on the third to fifth regions III, IV and V of the substrate 400. Thus, only the seventh semiconductor device will be described.

[00128] In example embodiments, the third to fifth regions III, IV and V of the substrate 400 may be NMOS regions, and the sixth to eighth regions VI, VII and VIII of the substrate 400 may be PMOS regions. For example, the sixth and seventh semiconductor devices may include NMOS transistors and PMOS transistors, respectively.

[00129] Referring to FIGS. 25, 26, 27A and 27B, the seventh semiconductor device may include sixth to eighth semiconductor patterns 722, 724 and 726, sixth to eighth epitaxial layers 812, 814 and 816, and sixth to eighth gate structures 882, 884 and 886 on the substrate 400. The seventh semiconductor device may further include sixth to eighth active fins 403, 405 and 407, the isolation pattern 430, sixth to eighth gate spacers 782, 784

and 786, an inner spacer 800, and the insulation layer 520.

[00130] The sixth to eighth gate structures 882, 884 and 886 may be formed on the sixth to eighth regions VI, VII and VIII, respectively, of the substrate 400, and may surround sixth to eighth semiconductor patterns 722, 724 and 726, respectively.

5 **[00131]** The sixth gate structure 882 may include a sixth gate insulation pattern, a seventh threshold voltage control pattern 862, and an eighth threshold voltage control pattern 872 sequentially stacked from a surface of each of the sixth semiconductor patterns 722, and the sixth gate insulation pattern may include a sixth interface pattern 842 and a sixth high-k dielectric pattern 852 sequentially stacked. The sixth gate structure 882 together with the
10 sixth epitaxial layer 812 and the sixth semiconductor pattern 722 may form a sixth transistor.

[00132] The seventh gate structure 884 may include a seventh gate insulation pattern and a ninth threshold voltage control pattern 864 sequentially stacked from a surface of each of the seventh semiconductor patterns 724, and the seventh gate insulation pattern may include
15 a seventh interface pattern 844 and a seventh high-k dielectric pattern 854 sequentially stacked, and a fourth dipole layer 914 at an interface therebetween. The seventh gate structure 884 together with the seventh epitaxial layer 814 and the seventh semiconductor pattern 724 may form a seventh transistor.

[00133] The eighth gate structure 886 may include an eighth gate insulation pattern and a
20 tenth threshold voltage control pattern 866, and the eighth gate insulation pattern may include an eighth interface pattern 846 and an eighth high-k dielectric pattern 856 sequentially stacked. The eighth gate structure 886 together with the eighth epitaxial layer 816 and the eighth semiconductor pattern 726 may form an eighth transistor.

[00134] In example embodiments, all of sixth to eighth threshold voltages of the

respective sixth to eighth transistors on the respective sixth to eighth regions VI, VII and VIII may have negative values, and absolute values of the sixth to eighth threshold voltages may decrease in this order. For example, the absolute value of the sixth threshold voltage may be greater than the absolute value of the seventh threshold voltage, and the absolute value of the seventh threshold voltage may be greater than the absolute value of the eighth threshold voltage.

[00135] In example embodiments, the ninth and tenth threshold voltage control patterns 864 and 866 may include substantially the same material, e.g., titanium nitride, and may have substantially the same thickness. However, as the fourth dipole layer 914 includes, e.g., lanthanum oxide dipoles, the seventh threshold voltage of the seventh transistor may move in a negative direction, and thus the absolute value of the seventh threshold voltage of the seventh transistor may be greater than the absolute value of the eighth threshold voltage of the eighth transistor.

[00136] The sixth transistor may include the seventh and eighth threshold voltage control patterns 862 and 872 sequentially stacked, and the seventh and eighth threshold voltage control patterns 862 and 872 may include, e.g., titanium silicon nitride and titanium nitride, respectively. As the sixth transistor has the seventh threshold voltage control pattern 862 including titanium silicon nitride having good diffusion prevention characteristics for a workfunction metal, the sixth threshold voltage of which an absolute value is high may be obtained.

[00137] In the figures, according to exemplary embodiments, the sixth to eighth transistors are shown to include no workfunction metal patterns, however, the inventive concepts may not be limited thereto. Thus, in some embodiments, the sixth to eighth transistors may include workfunction metal patterns, respectively, according to the distances

between channels.

[00138] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example
5 embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. Therefore, it is
10 to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A semiconductor device, comprising:

a first transistor having a first threshold voltage, the first transistor including:

5 first channels on a substrate, the first channels being spaced apart from each other in a vertical direction on an upper surface of the substrate;

first source/drain layers on the substrate, the first source/drain layers being connected to respective opposite sidewalls of the first channels; and

a first gate structure surrounding the first channels and including a first gate
10 insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels; and

a second transistor having a second threshold voltage greater than the first threshold voltage, the second transistor including:

15 second channels on the substrate, the second channels being spaced apart from each other in the vertical direction on the upper surface of the substrate;

second source/drain layers on the substrate, the second source/drain layers being connected to respective opposite sidewalls of the second channels; and

a second gate structure surrounding the second channels and including a second gate insulation pattern, a second threshold voltage control pattern, and a second
20 workfunction metal pattern sequentially stacked from a surface of each of the second channels,

wherein a thickness of the second threshold voltage control pattern in a direction perpendicular to the upper surface of the substrate is less than a thickness of the first threshold voltage control pattern in the direction perpendicular to the upper surface of the

substrate.

2. The semiconductor device of claim 1, wherein the first threshold voltage control pattern has a material composition different from a material composition of the second threshold voltage control pattern.

3. The semiconductor device of claim 1 or claim 2, wherein each of the first and second threshold voltage control patterns includes at least one of titanium nitride, titanium oxynitride, titanium oxycarbonitride, titanium silicon nitride, titanium oxynitride, titanium aluminum oxynitride, tantalum nitride, tantalum oxynitride, tantalum aluminum nitride, tantalum aluminum oxynitride, tungsten nitride, tungsten carbonitride, and aluminum oxide.

4. The semiconductor device of claim 3, wherein the first threshold voltage control pattern includes titanium nitride, and the second threshold voltage control pattern includes titanium silicon nitride.

5. The semiconductor device of claim 3 or claim 4, wherein the first threshold voltage control pattern has a single layer, and the second threshold voltage control pattern includes a double-layered structure.

6. The semiconductor device of any one of claims 1 to 5, wherein the first threshold voltage control pattern includes a titanium nitride layer, and the second threshold voltage control pattern includes a titanium nitride layer and a titanium silicon nitride layer

sequentially stacked.

7. The semiconductor device of claim 1, wherein the first gate insulation pattern includes a first interface pattern and a first high-k dielectric pattern sequentially stacked, and the second gate insulation pattern includes a second interface pattern and a second high-k dielectric pattern sequentially stacked.

8. The semiconductor device of claim 7, wherein the second gate insulation pattern further includes a dipole layer at an interface between the second interface pattern and the second high-k dielectric pattern, the dipole layer including aluminum oxide dipoles.

9. The semiconductor device of claim 8, wherein the first and second threshold voltage control patterns have the same material composition.

10. The semiconductor device of claim 9, wherein each of the first and second threshold voltage control patterns includes a titanium nitride layer.

11. The semiconductor device of any one of claims 8 to 10, wherein the second interface pattern includes silicon oxide, and the second high-k dielectric pattern includes at least one of hafnium oxide, tantalum oxide, and zirconium oxide.

12. The semiconductor device of any one of claims 7 to 11, further comprising a first dipole layer at an interface between the first interface pattern and the first high-k dielectric pattern, the first dipole layer including lanthanum oxide dipoles.

13. The semiconductor device of claim 12, wherein the first interface pattern includes silicon oxide, and the first high-k dielectric pattern includes at least one of hafnium oxide, tantalum oxide, and zirconium oxide.

5

14. The semiconductor device of any one of claims 1 to 13, wherein a thickness in the vertical direction of a portion of the first workfunction metal pattern between the first channels is equal to or less than a thickness in the vertical direction of a portion of the second workfunction metal pattern between the second channels.

10

15. The semiconductor device of any one of claims 1 to 13, wherein a thickness in the vertical direction of a portion of the first workfunction metal pattern between the first channels is less than a thickness in a horizontal direction of a portion of the first workfunction metal pattern stacked from a sidewall of the first threshold voltage control pattern, the horizontal direction being parallel to the upper surface of the substrate.

15

16. The semiconductor device of any one of claims 1 to 15, wherein the first and second workfunction metal patterns have the same material composition.

17. The semiconductor device of any one of claims 1 to 16, wherein each of the first and second source/drain layers includes single crystalline silicon doped with n-type impurities or single crystalline silicon carbide doped with n-type impurities.

20

18. The semiconductor device of any one of claims 1 to 17, wherein each of

the first and second channels is a nanosheet, and wherein each of a distance between the first channels and a distance between the second channels is equal to or less than about 10nm.

5 19. A semiconductor device of any one of claims 1 to 18, further comprising:
a third transistor having a third threshold voltage greater than the second threshold voltage, the third transistor including:

third channels on the substrate, the third channels being spaced apart from each other in the vertical direction on the upper surface of the substrate;

10 third source/drain layers on the substrate, the third source/drain layers being connected to respective opposite sidewalls of the third channels; and

a third gate structure surrounding the third channels and including a third gate insulation pattern, a third threshold voltage control pattern, and a third workfunction metal pattern sequentially stacked from a surface of each of the third channels,

15 wherein the thickness of the third threshold voltage control patterns in a direction perpendicular to the upper surface of the substrate is equal to or less than a thickness of the second threshold voltage control pattern in the direction perpendicular to the upper surface of the substrate.

20 20. A semiconductor device, comprising:
a first transistor having a positive first threshold voltage, the first transistor including:

first channels on a first region of a substrate including the first region and a second region, the first channels being spaced apart from each other in a vertical direction

on an upper surface of the substrate;

first source/drain layers on the first region of the substrate, the first source/drain layers being connected to respective opposite sidewalls of the first channels; and

5 a first gate structure surrounding the first channels and including a first gate insulation pattern, a first threshold voltage control pattern, and a first workfunction metal pattern sequentially stacked from a surface of each of the first channels;

a second transistor having a positive second threshold voltage greater than the positive first threshold voltage, the second transistor including:

10 second channels on the first region of the substrate, the second channels being spaced apart from each other in the vertical direction on the upper surface of the substrate;

second source/drain layers on the first region of the substrate, the second source/drain layers being connected to respective opposite sidewalls of the second channels;

15 and

a second gate structure surrounding the second channels and including a second gate insulation pattern, a second threshold voltage control pattern, and a second workfunction metal pattern sequentially stacked from a surface of each of the second channels; and

20 a third transistor having a negative third threshold voltage, the third transistor including:

third channels on the second region of the substrate, the third channels being spaced apart from each other in the vertical direction on the upper surface of the substrate;

third source/drain layers on the substrate, the third source/drain layers being connected to respective opposite sidewalls of the third channels; and

a third gate structure surrounding the third channels and including a third gate insulation pattern and a third threshold voltage control pattern sequentially stacked
5 from a surface of each of the third channels,

wherein the first threshold voltage control pattern has a first pattern having a first material composition, the second threshold voltage control pattern has a second pattern having a second material composition different from the first material composition, and the third threshold voltage control pattern has the first and second patterns,

10 wherein a thickness of the second threshold voltage control pattern in a direction perpendicular to the upper surface of the substrate is less than a thickness of the first threshold voltage control pattern in the direction perpendicular to the upper surface of the substrate.

15