SEMICONDUCTOR DEVICE ~~AND METHOD OF FORMING~~HAVING A VERTICAL INTERCONNECT STRUCTURE USING STUD BUMPS

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming a vertical interconnect structure using stud bumps and integrated passive devices (IPD) for fan-out wafer level chip scale packages (FO-WSCSP).

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor

A plurality of semiconductor die or components 124 is mounted to interface layer 121 in a flipchip arrangement with contact pads 126 oriented downward over carrier 120. Semiconductor die 124 each include an active surface 128 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 128 to implement baseband analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die 124 may also contain IPD, such as inductors, capacitors, and resistors, for RF signal processing. In another embodiment, a discrete semiconductor component can be mounted to interface layer 121.

In FIG. 3b, a plurality of stud bumps or posts 130 are formed over the wettable contact pads of conductive layer 122. In one embodiment, a wire-bonding machine can form stud bumps 130. Stud bumps 130 have a height ranging from 2-120 micrometers (μm).

FIG. 3b shows stud bumps 130 implemented as stud bumps, including bump portion 132 and stud portion 134. In another embodiment, stud bumps 130 can be formed with stacked bumps 136, as shown in FIG. 3c. Stud bumps 130 can also be formed without conductive layer 122, as shown in FIG. 3d. In any case, the formation of stud bumps 130 use a simple, low-cost manufacturing process.

FIG. 3e shows an encapsulant or molding compound 138 deposited over semiconductor die 124 and stud bumps 130 using a paste printing, compressive molding, transfer molding, liquid

Claims

What is claimed:

~~1. A method of making a semiconductor device, comprising:~~

~~providing a semiconductor die;~~

~~forming a conductive layer outside a footprint of the semiconductor die;~~

~~forming a first stud bump over the conductive layer;~~

~~depositing an encapsulant over the semiconductor die and around the first stud bump;~~

~~forming a first interconnect structure over a first surface of the encapsulant, the first interconnect structure including a first integrated passive device (IPD) electrically connected to the first stud bump; and~~

~~forming a second interconnect structure over a second surface of encapsulant opposite the first interconnect structure.~~

~~2. The method of claim 1, wherein the second interconnect structure includes a second IPD.~~

~~3. The method of claim 1, wherein the first stud bump includes a plurality of stacked bumps.~~

~~4. The method of claim 1, wherein the first stud bump includes a bump portion and a stud portion.~~

~~5. The method of claim 1, further including forming a second stud bump over the semiconductor die electrically connected to the first interconnect structure.~~

6. The method of claim 1, further including forming a bond wire between the semiconductor die and conductive layer.

7. A method of making a semiconductor device, comprising:
providing a semiconductor die or component;
forming a vertical interconnect structure around the semiconductor die or component;
depositing an encapsulant over the semiconductor die or component and around the vertical interconnect structure;
forming a first interconnect structure over a first surface of the encapsulant; and
forming a second interconnect structure over a second surface of encapsulant opposite the first interconnect structure.

8. The method of claim 7, wherein the first interconnect structure includes an integrated passive device.

9. The method of claim 7, wherein the second interconnect structure includes an integrated passive device.

10. The method of claim 7, wherein the vertical interconnect structure includes a plurality of stacked bumps.

11. The method of claim 7, wherein the vertical interconnect structure includes a bump portion and a stud portion.

12. The method of claim 7, further including:

stacking a plurality of semiconductor devices; and

electrically connecting the stacked semiconductor devices through the first interconnect structure, second interconnect structure, and vertical interconnect structure.

13. The semiconductor device of claim 7, further including forming a third interconnect structure over the semiconductor die or component and electrically connected to the first interconnect structure.

14. A method of making a semiconductor device, comprising:

providing a semiconductor die or component;

forming a vertical interconnect structure around the semiconductor die or component;

depositing an encapsulant over the semiconductor die or component and around the vertical interconnect structure; and

forming a first interconnect structure over a first surface of the encapsulant, the first interconnect structure including a first integrated passive device (IPD).

15. The method of claim 14, further including forming a second interconnect structure over a second surface of encapsulant opposite the first interconnect structure.

16. The method of claim 15, wherein the second interconnect structure includes a second IPD.

17. The method of claim 14, wherein the vertical interconnect structure includes a bump portion and stud portion or a plurality of stacked bumps.

~~18. The method of claim 14, further including forming a conductive layer outside a footprint of the semiconductor die or component prior to forming the vertical interconnect structure.~~

~~19. The method of claim 14, further including:~~

~~stacking a plurality of semiconductor devices; and~~

~~electrically connecting the stacked semiconductor devices through the first interconnect structure and vertical interconnect structure.~~

~~20. The method of claim 14, further including forming a third interconnect structure over the semiconductor die or component and electrically connected to the first interconnect structure.~~

~~2~~1. A semiconductor device, comprising:

a semiconductor die or component;

a vertical interconnect structure formed ~~around~~adjacent to the semiconductor die or component, the vertical interconnect structure including a bump portion and a stud portion extending from the bump portion;

an encapsulant deposited over the semiconductor die or component and around the vertical interconnect structure; and

a first interconnect structure formed over a first surface of the encapsulant, the first interconnect structure including a plurality of conductive layers and an insulating layer which form a first integrated passive device (IPD).

~~2~~2. The semiconductor device of claim ~~2~~1, further including a second interconnect structure formed over a second surface of the encapsulant opposite the first interconnect structure.

~~2~~3. The semiconductor device of claim ~~22~~1, wherein the ~~second~~first interconnect structure includes a second IPD.

~~24. The semiconductor device of claim 21, wherein the vertical interconnect structure includes a bump portion and a stud portion or a plurality of stacked bumps.~~

~~25~~4. The semiconductor device of claim ~~2~~1, further including a plurality of stacked semiconductor devices electrically connected through the vertical interconnect structure.

5. A semiconductor device, comprising:

a semiconductor die or component;

a stud bump disposed adjacent to the semiconductor die or component, the stud bump including a bump portion and a stud portion extending from the bump portion;

an encapsulant disposed over the semiconductor die or component and stud bump with the stud portion of the stud bump extending through the encapsulant;

a first interconnect structure formed over a first surface of the encapsulant and contacting the stud portion of the stud bump; and

a second interconnect structure formed over a second surface of the encapsulant opposite the first surface of the encapsulant and coupled to the first interconnect structure through the stud bump.

6. The semiconductor device of claim 5, wherein the first interconnect structure includes a first integrated passive device (IPD) and the second interconnect structure includes a second IPD.

7. The semiconductor device of claim 5, further including a contact pad disposed over the stud bump.

8. The semiconductor device of claim 5, further including a plurality of stacked semiconductor devices electrically connected through the first interconnect structure, second interconnect structure, and stud bump.

9. The semiconductor device of claim 5, further including a third interconnect structure formed over the semiconductor die or component and electrically connected to the first interconnect structure.

10. A semiconductor device, comprising:

a semiconductor die or component;

a stud bump formed adjacent to the semiconductor die or component;

a first interconnect structure formed over a first surface of the semiconductor die or component and coupled to the stud bump; and

a second interconnect structure formed over a second surface of the semiconductor die or component opposite the first surface of the semiconductor die and coupled to the first interconnect structure through the stud bump.

11. The semiconductor device of claim 10, wherein the first interconnect structure includes a first integrated passive device (IPD) and the second interconnect structure includes a second IPD.

12. The semiconductor device of claim 10, wherein the stud bump includes a plurality of stacked bumps.

13. A semiconductor device, comprising:

a first interconnect structure including a first integrated passive device (IPD);

a stud bump formed over the first interconnect structure;

a semiconductor die or component disposed over the first interconnect structure;

an encapsulant formed over the semiconductor die or component and around the stud bump; and

a second interconnect structure formed over the encapsulant opposite the first interconnect structure.

14. The semiconductor device of claim 13, further including a plurality of stacked semiconductor devices electrically connected through the stud bump.

15. The semiconductor device of claim 13, wherein the semiconductor die or component includes a flipchip semiconductor die including an active surface oriented toward the first interconnect structure.