WHAT IS CLAIMED IS:

1. A circuit comprising:

a first power clamp coupled to a first power rail and a first ground rail;

a first NMOS transistor having a first source, a first drain, and a first gate, wherein the first source is coupled to a second ground rail; and

a first PMOS transistor having a second source, a second drain, and a second gate, wherein the second source is coupled to the first power rail, and the first power clamp provides a signal to turn on the first NMOS transistor during an ESD event that occurs at the first power rail.

2. The circuit according to claim 1, wherein the first gate is coupled to the first power clamp, the second drain is coupled to the first drain, and an ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the ESD event.

3. The circuit according to claim 1, further comprising:

a second power clamp coupled to a second power rail and the second ground rail, wherein an ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the ESD event.

4. The circuit according to claim 1, further comprising:

a second NMOS transistor having a third source, a third drain, a third gate, and a body, wherein the body is coupled to the second ground rail, and the second NMOS transistor is turned on during the ESD event.

5. The circuit according to claim 4, wherein the third source is coupled to the second drain, and the third drain is coupled to a second power rail, the circuit further comprising:

a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate, wherein the fourth source is coupled to the first ground rail, the fourth drain is coupled to the third gate, and the fourth gate is coupled to the second ground rail.

6. The circuit according to claim 5, wherein an ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the ESD event.

7. The circuit according to claim 1, further comprising:

a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate, wherein the fifth source is coupled to the first source; and

a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate, wherein the sixth source is coupled to the second power rail, the sixth drain is coupled to the fifth drain, and the sixth gate is coupled to the second drain and the fifth gate.

8. The circuit according to claim 1, wherein the first power clamp includes:

a resistor coupled to the first power rail;

a capacitor coupled to the resistor and the first ground rail; and

an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.

9. A method comprising:

coupling a first power clamp to a first power rail and a first ground rail;

providing a first NMOS transistor having a first source, a first drain, and a first gate;

coupling the first source to a second ground rail;

providing a first PMOS transistor having a second source, a second drain, and a second gate;

coupling the second source to the first power rail; and

providing, via the first power clamp, a signal to turn on the first NMOS transistor during an ESD event that occurs at the first power rail.

10. The method according to claim 9, further comprising:

coupling the first gate to the first power clamp; and

coupling the second drain to the first drain, wherein an ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the ESD event.

11. The method according to claim 9, further comprising:

coupling a second power clamp to a second power rail and the second ground rail, wherein an ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the ESD event.

12. The method according to claim 9, further comprising:

providing a second NMOS transistor having a third source, a third drain, a third gate, and a body; and

coupling the body to the second ground rail, wherein the second NMOS transistor is turned on during the ESD event.

13. The method according to claim 12, further comprising:

coupling the third source to the second drain;

coupling the third drain to a second power rail;

providing a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate;

coupling the fourth source to the first ground rail;

coupling the fourth drain to the third gate; and

coupling the fourth gate to the second ground rail.

14. The method according to claim 13, wherein an ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the ESD event.

15. The method according to claim 9, further comprising:

providing a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate;

coupling the fifth source to the first source;

providing a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate;

coupling the sixth source to the second power rail;

coupling the sixth drain to the fifth drain; and

coupling the sixth gate to the second drain and the fifth gate.

16. The method according to claim 9, wherein the first power clamp is provided by:

providing a resistor coupled to the first power rail;

providing a capacitor coupled to the resistor and the first ground rail; and

providing an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.

17. A circuit comprising:

a first power clamp coupled to a first power rail and a first ground rail;

a first NMOS transistor having a first source, a first drain, and a first gate; and

a first PMOS transistor having a second source, a second drain, and a second gate,

wherein the first source is coupled to a second ground rail, and the first gate is coupled to the first power clamp, the second source is coupled to the first power rail, and the second drain is coupled to the first drain, and

wherein the first power clamp provides a signal to turn on the first NMOS transistor during a cross-domain ESD event that occurs at the first power rail, and a first ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the cross-domain ESD event.

18. The circuit according to claim 17, further comprising:

a second power clamp coupled to a second power rail and the second ground rail, wherein a second ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the cross-domain ESD event.

19. The circuit according to claim 17, further comprising:

a second NMOS transistor having a third source, a third drain, a third gate, and a body, wherein the body is coupled to the second ground rail, the third source is coupled to the second drain, the third drain is coupled to a second power rail, and the second NMOS transistor is turned on during the cross-domain ESD event; and

a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate, wherein the fourth source is coupled to the first ground rail, the fourth drain is coupled to the third gate, the fourth gate is coupled to the second ground rail, and a third ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the cross-domain ESD event.

20. The circuit according to claim 17, further comprising:

a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate, wherein the fifth source is coupled to the first source; and

a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate, wherein the sixth source is coupled to the second power rail, the sixth drain is coupled to the fifth drain, and the sixth gate is coupled to the second drain and the fifth gate, and

wherein the first power clamp includes: a resistor coupled to the first power rail; a capacitor coupled to the resistor and the first ground rail; and an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a first power clamp coupled to a first power rail and a first ground rail;

a first NMOS transistor having a first source, a first drain, and a first gate, wherein the first source is coupled to a second ground rail;

a first PMOS transistor having a second source, a second drain, and a second gate, wherein the second source is coupled to the first power rail, and the first power clamp provides a signal to turn on the first NMOS transistor during an ESD event that occurs at the first power rail;

a second NMOS transistor having a third source, a third drain, a third gate, and a body, wherein the body is coupled to the second ground rail, and the second NMOS transistor is turned on during the ESD event; and

a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate,

wherein the third source is coupled to the second drain, and the third drain is coupled to a second power rail, and the fourth source is coupled to the first ground rail, the fourth drain is coupled to the third gate, and the fourth gate is coupled to the second ground rail.

2. The circuit according to claim 1, wherein the first gate is coupled to the first power clamp, the second drain is coupled to the first drain, and an ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the ESD event.

3. The circuit according to claim 1, further comprising:

a second power clamp coupled to a second power rail and the second ground rail, wherein an ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the ESD event.

4. The circuit according to claim 1, wherein an ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the ESD event.

5. The circuit according to claim 1, further comprising:

a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate, wherein the fifth source is coupled to the first source; and

a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate, wherein the sixth source is coupled to the second power rail, the sixth drain is coupled to the fifth drain, and the sixth gate is coupled to the second drain and the fifth gate.

6. The circuit according to claim 1, wherein the first power clamp includes:

a resistor coupled to the first power rail;

a capacitor coupled to the resistor and the first ground rail; and

an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.

7. A method comprising:

coupling a first power clamp to a first power rail and a first ground rail;

providing a first NMOS transistor having a first source, a first drain, and a first gate;

coupling the first source to a second ground rail;

providing a first PMOS transistor having a second source, a second drain, and a second gate;

coupling the second source to the first power rail;

providing, via the first power clamp, a signal to turn on the first NMOS transistor during an ESD event that occurs at the first power rail;

providing a second NMOS transistor having a third source, a third drain, a third gate, and a body;

coupling the body to the second ground rail, wherein the second NMOS transistor is turned on during the ESD event;

coupling the third source to the second drain;

coupling the third drain to a second power rail;

providing a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate;

coupling the fourth source to the first ground rail;

coupling the fourth drain to the third gate; and

coupling the fourth gate to the second ground rail.

8. The method according to claim 7, further comprising:

coupling the first gate to the first power clamp; and

coupling the second drain to the first drain, wherein an ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the ESD event.

9. The method according to claim 7, further comprising:

coupling a second power clamp to a second power rail and the second ground rail, wherein an ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the ESD event.

10. The method according to claim 7, wherein an ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the ESD event.

11. The method according to claim 7, further comprising:

providing a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate;

coupling the fifth source to the first source;

providing a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate;

coupling the sixth source to the second power rail;

coupling the sixth drain to the fifth drain; and

coupling the sixth gate to the second drain and the fifth gate.

12. The method according to claim 7, wherein the first power clamp is provided by:

providing a resistor coupled to the first power rail;

providing a capacitor coupled to the resistor and the first ground rail; and

providing an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.

13. A circuit comprising:

a first power clamp coupled to a first power rail and a first ground rail;

a first NMOS transistor having a first source, a first drain, and a first gate;

a first PMOS transistor having a second source, a second drain, and a second gate;

a second NMOS transistor having a third source, a third drain, a third gate, and a body; and

a second PMOS transistor having a fourth source, a fourth drain, and a fourth gate,

wherein the first source is coupled to a second ground rail, and the first gate is coupled to the first power clamp, the second source is coupled to the first power rail, and the second drain is coupled to the first drain,

wherein the first power clamp provides a signal to turn on the first NMOS transistor during a cross-domain ESD event that occurs at the first power rail, and a first ESD path from the first PMOS transistor to the second ground rail through the first NMOS transistor is provided during the cross-domain ESD event,

wherein the body is coupled to the second ground rail, the third source is coupled to the second drain, the third drain is coupled to a second power rail, and the second NMOS transistor is turned on during the cross-domain ESD event, and

wherein the fourth source is coupled to the first ground rail, the fourth drain is coupled to the third gate, the fourth gate is coupled to the second ground rail, and a third ESD path from the first PMOS transistor to the second power rail through the second NMOS transistor is provided during the cross-domain ESD event.

14. The circuit according to claim 13, further comprising:

a second power clamp coupled to a second power rail and the second ground rail, wherein a second ESD path from the first PMOS transistor to the second power rail through the first NMOS transistor and the second power clamp is provided during the cross-domain ESD event.

15. The circuit according to claim 13, further comprising:

a third NMOS transistor having a fifth source, a fifth drain, and a fifth gate, wherein the fifth source is coupled to the first source; and

a third PMOS transistor having a sixth source, a sixth drain, and a sixth gate, wherein the sixth source is coupled to the second power rail, the sixth drain is coupled to the fifth drain, and the sixth gate is coupled to the second drain and the fifth gate, and

wherein the first power clamp includes: a resistor coupled to the first power rail; a capacitor coupled to the resistor and the first ground rail; and an inverter having an input terminal coupled to the resistor and the capacitor, and an output terminal coupled to the first gate.