

A Quantizer Device

TECHNICAL FIELD

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The present disclosure relates broadly to a quantizer device and to a method of quantizing a signal.

BACKGROUND

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In the field of analog-to-digital converters (ADCs), quantizers are a part of ADCs, where analog signals are quantized in time and voltage to generate finite output bits at finite intervals of time. Quantizers can be single bit or multi-bit. Even though single bit quantizers are relatively simple to design and are inherently linear, use of a single bit output reduces the linearity of a first integrator in a loop (sigma delta modulator loop). On the other hand, multi-bit quantizers need additional design requirements such as linearity of the multi-bit quantizers/DAC (digital-to-analog conversion) at the output and a need for wider voltage output swing for the last integrator in a high-order sigma delta loop.

20 In relation to the above limitations, it is recognised that sigma delta ADCs typically use three types of multi-bit quantizers, namely Flash, successive approximation register (SAR) and Voltage-Controlled Oscillator-based (VCO-based) quantizer types. For these types of typical quantizers, it is known that such quantizers require a large input swing for a higher dynamic range, which in turn increases the voltage output swing requirement of the last integrator in a sigma delta loop. Further, it is recognised that a majority of the above-named quantizers typically require additional dynamic element matching (DEM) at the output for DAC linearity or to minimise distortion. Such DEM processes increase loop delay and hence, can reduce the stability of the sigma delta loop.

30 In view of the above limitations and different types of quantizers, the inventor recognises that delta modulation may be explored instead. Delta modulation is a relatively simple technique used in communication fields to transmit high bandwidth, low resolution data where the output bit is reduced to a one-bit stream. In delta modulation, an analog signal input is approximated with a series of segments. Each segment of the approximated signal is compared to the preceding bits and the successive bits are determined by this comparison. Thus, past information is used in delta modulation. In delta modulation, only the change in information is sent/output. That is, only

an increase or decrease of the error amplitude from the previous sample is sent whereas a no-change condition results in the modulated signal remaining at the same 0 or 1 state of the previous sample.

5 However, it is recognised that when using delta modulation as quantizer, the limitations of stability, large output swing and output rotation pattern, i.e. DEM to minimise DAC nonlinearity, are still challenges that are present.

10 In view of the above, there exists a need for a quantizer device and a method for quantising a signal that seeks to address at least one of the above problems.

SUMMARY

15 In accordance with an aspect of the present disclosure, there is provided a quantizer device, the quantizer device comprising, a plurality of comparators for coupling to an integrator output of an integrator stage of a signal modulator, the plurality of comparators to perform multi-bit quantization of the integrator output; a feedback loop connection coupled to outputs of the plurality of comparators and coupled to an input of the integrator stage, the feedback loop connection for transmitting quantized outputs of the plurality of comparators as a
20 comparator feedback signal to the input of the integrator stage; a digital-to-analog converter disposed within the feedback loop connection to perform digital-to-analog conversion of the quantized outputs of the plurality of comparators to generate the comparator feedback signal; and a gain stage disposed within the feedback loop connection to provide a gain to the comparator feedback signal.

25 The quantizer device may further comprise a digital logic component coupled to the plurality of comparators, the digital logic component to receive the quantized outputs of the plurality of comparators and the digital logic component disposed to provide a final output of the quantizer device.

30 The digital logic component may comprise one or more state-machine based digital logic gates and the digital logic component may be capable of utilising the quantized outputs of the plurality of comparators to change a state of the one or more state-machine based digital logic gates to perform digital integration and dynamic element matching (DEM) within
35 the digital logic component.

The DEM may be based on CLA (Clocked Level Averaging), and the digital logic component may comprise a plurality of cyclic shift registers each clocked by a gated clock, the gated clock based on the quantized outputs of the plurality of comparators.

5 The digital logic component may further comprise a digital member to process a state difference of the plurality of cyclic shift registers to produce a final N-bit output of the quantizer device.

10 The digital member may be a XOR gate.

15 The DEM may be based on DWA (Data Weighted Averaging), and the digital logic component may comprise a plurality of unit cells, each unit cell coupled to the quantized outputs of the plurality of comparators and each unit cell clocked based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.

20 The unit cells may be coupled to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.

25 The digital logic component may further comprise a DWA-DEM generation element that is disposed to generate a DEM pattern based on a current/present state of the each unit cell output.

 The DWA-DEM generation element may comprise a plurality of multiplexer units connected in series.

30 The plurality of comparators may each have an input coupled to a single voltage reference and the multi-bit quantization of the integrator output is performed based on the single voltage reference.

35 In accordance with another aspect of the present disclosure, there is provided a method of quantizing a signal, the method comprising, inputting a signal into a sigma delta modulator; coupling a plurality of comparators to an integrator output of an integrator stage of the modulator; performing multi-bit quantization of the integrator output using the plurality of comparators; providing a feedback of quantized outputs of the plurality of comparators to an

input of the integrator stage, the quantized outputs of the plurality of comparators being a comparator feedback signal to the input of the integrator stage; performing digital-to-analog conversion of the quantized outputs of the plurality of comparators to generate the comparator feedback signal; and providing a gain to the comparator feedback signal.

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The method may further comprise coupling a digital logic component to the plurality of comparators, receiving the quantized outputs of the plurality of comparators into the digital logic component and using the digital logic component to provide a final output of the quantizer device.

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The method may further comprise utilising the quantized outputs of the plurality of comparators to change a state of one or more state-machine based digital logic gates of the digital logic component to perform digital integration and dynamic element matching (DEM) within the digital logic component.

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The DEM may be based on CLA (Clocked Level Averaging), and the method may further comprise clocking a plurality of cyclic shift registers of the digital logic component, with each clocked by a gated clock, the gated clock based on the quantized outputs of the plurality of comparators.

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The method may further comprise processing a state difference of the plurality of cyclic shift registers to produce a final N-bit output of the quantizer device using a digital member of the digital logic component.

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The DEM may be based on DWA (Data Weighted Averaging), and the method may further comprise coupling a plurality of unit cells of the digital logic component, each coupled to the quantized outputs of the plurality of comparators; clocking each unit cell based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.

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The method may further comprise coupling the unit cells to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.

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The method may further comprise using a DWA-DEM generation element of the digital logic component to generate a DEM pattern based on a current/present state of the each unit cell output.

- 5 The method may further comprise coupling an input of each of the plurality of comparators to a single voltage reference and performing the multi-bit quantization of the integrator output based on the single voltage reference.

BRIEF DESCRIPTION OF THE DRAWINGS

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Exemplary embodiments of the present disclosure will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

- 15 FIG. 1A is a schematic diagram of an analog-to-digital converter (ADC) using delta modulation.

FIG. 1B is a fast Fourier transform of the output of the ADC of FIG. 1A.

- 20 FIG. 1C shows output waveforms of the ADC of FIG. 1A.

FIG. 2 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in an exemplary embodiment.

- 25 FIG. 3 is an exemplary illustration of switching capacitor circuits used for digital-to-analog conversion in the exemplary embodiment.

FIG. 4 is a diagram illustrating waveforms obtained from the ADC of FIG. 2 in the exemplary embodiment.

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FIG. 5 is a fast Fourier transform of the output of the ADC of FIG. 2.

FIG. 6 shows output waveforms from the ADC of FIG. 2.

- 35 FIG. 7 is a schematic diagram for illustrating a digital logic component in an exemplary embodiment for implementing digital integration and Clocked Level Averaging Dynamic Element Matching (CLA-DEM).

FIG. 8 shows a set of waveforms obtained from the digital logic component of FIG. 7.

FIG. 9A is a schematic diagram for illustrating a digital logic component in an exemplary embodiment for implementing digital integration and Data Weighted Averaging Dynamic Element Matching (DWA-DEM).

FIG. 9B is a flow sheet providing an algorithm for data generation for digital integration in the exemplary embodiment.

FIG. 9C is a schematic diagram illustrating a DWA-DEM generation block in the exemplary embodiment.

FIG. 10 is an output spectrum obtained from a second order sigma delta modulator using a quantizer device of an exemplary embodiment.

FIG. 11 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in another exemplary embodiment.

FIG. 12 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in another exemplary embodiment.

FIG. 13 is a schematic flowchart for illustrating a method of quantizing a signal in an exemplary embodiment.

DETAILED DESCRIPTION

In exemplary embodiments described herein, there may be provided a multi-bit quantizer/quantizer device for delta modulation in a sigma delta loop.

The inventor recognises that delta modulation can be explored as a quantizer in a sigma delta loop.

FIG. 1A is a schematic diagram of an analog-to-digital converter (ADC) using delta modulation. The number of integrators n in the sigma delta loop indicates the n^{th} -order of the sigma delta loop. In the ADC 102, there is shown a second order delta modulator 104 with a delta modulator 106 as a quantizer device 106.

The quantizer device 106 comprises a comparator 108 coupled to a digital integrator 110. The delta modulator 104 has an integrator stage that comprises a last integrator 112. The output of the last integrator 112 is coupled to the comparator 108.

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In the ADC 102, the previous digital output (output at the digital integrator 110) is subtracted from the output of the integrator 112 (see numeral 114) and the comparator 108 determines whether there is a delta change in output (defined by V_{REF}) and produces a 1 or -1 as the comparator output. The digital integrator 110 accumulates the comparator output to produce an N-bit output 116. The N-bit output 116 is transmitted to the output of the last integrator 112 (see numeral 114) and to an input of the delta modulator 104 (see numeral 130).

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The inventor recognises that the structure shown in ADC 102 may have a number of limitations. The inventor recognises that the multi-bit digital output 116 is oscillating due to usage of the single bit comparator 108 which produces 1, -1 as output. Therefore, signal-to-noise ratio (SNR) is degraded. Further, the last integrator 112 needs a large output swing (at node B of FIG. 1) for achieving full-scale dynamic range. Reference may be made to FIG. 1B.

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FIG. 1B is a fast Fourier transform of the output of the ADC 102 of FIG. 1A. The fast Fourier transform (FFT) results 118 show the waveform as a function of frequency. As seen in the FFT results 118, the single bit comparator 108 produces oscillations e.g. 120 as $fs/2$ as shown in FIG. 1B, and increases the noise floor limiting SNR. The FFT results 118 also shows the harmonics 122 caused by the integrator 112 when the swing requirements are high. From the FFT results 118, the inventor recognises that a lower swing for the op-amp integrators should be taken into account.

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From the ADC of FIG. 1A, the inventor recognises that the delta modulation implicitly assumes that the change in input is limited to $2 \cdot V_{REF}$. However, the changes in the integrator output at node B in FIG. 1A can exceed $2 \cdot V_{REF}$ in a higher order loop causing loop stability issues. Reference may be made to FIG. 1C.

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FIG. 1C shows output waveforms of the ADC of FIG. 1A. The output waveforms are for signal amplitude as a function of time. The waveforms 124, 126 are from the differential output at node B of FIG. 1A. The waveform 128 shows the output of the quantizer 106. The waveforms 124, 126 shows instability in the delta modulator 104 when the output exceeds $2 \cdot V_{REF}$. The waveforms 124, 126 show the voltage at node B of FIG. 1A oscillates between supply and ground rails (voltage). As a result, the output of the quantizer 106 shown at the waveform 128 saturates.

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In addition to the above limitations, the inventor recognises that a multi-bit DAC, i.e. at the output 116, needs additional dynamic element matching (DEM), e.g. an additional DEM block coupled to the output 116 to receive the N-bit output, to address DAC non-linearity. With the additional DEM block, loop delay for the ADC 102 increases. DEM is a technique that may be used to mitigate DAC element mismatch while using multi-bit feedback. In order to incorporate DEM for the delta modulator quantizer 106, additional digital logic is needed which can take up or incur at least half a cycle or one full cycle to rotate the output pattern obtained at the output 116. Such a delay is undesirable in a feedback path (see numeral 130 of FIG. 1A), which in turn leads to a need for additional loop delay compensation which further complicates the loop of the modulator 104. Thus, the inventor recognises that a quantizer device with inherent DEM is desirable.

FIG. 2 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in an exemplary embodiment. The ADC 202 comprises a second order delta sigma modulator with a second order loop filter, hereinafter termed modulator 204, the modulator having an integrator stage (e.g. a last integrator stage) comprising a last integrator 206. The ADC 202 further comprises a quantizer device 208.

The modulator 204 comprises an input node 205 for receiving an analog signal input (e.g. a sinusoidal input). In the exemplary embodiment, an N-bit output 216 of the ADC 202 is coupled to the input node 205, e.g. such that past/previous information is used for processing of the current analog signal input, and that change in input may be tracked by the quantizer device 208. In the exemplary embodiment, the modulator 204 comprises a first integrator 226 that provides its output at point A.

In the exemplary embodiment, the quantizer device 208 is provided to perform multi-bit quantization, e.g. two-bit quantization, on an output of the integrator 206 (e.g. of a last integrator stage). In the exemplary embodiment, instead of single bit comparison of conventional delta modulation, the quantizer device 208 employs two-bit quantization. In the exemplary embodiment, the two-bit quantization is performed on a differential output of the integrator 206 (e.g. of a last integrator stage). For two-bit quantization, in the exemplary embodiment, the quantizer device 208 comprises two comparators, i.e. a first comparator 212 and a second comparator 214. The comparators 212, 214 are coupled to the integrator 206 output. Any suitable voltage comparators may be used, including comparator circuits, op-amp comparators etc.

In the exemplary embodiment, the first comparator 212 and the second comparator 214 each compare against a single voltage reference V_{REF} . That is, the first comparator 212 and the second comparator 214 each have an input coupled to a single voltage reference V_{REF} (compare numeral 215) and the multi-bit quantization of the integrator output is performed
5 based on the single voltage reference V_{REF} .

The output of the first comparator 212 is C+ and the output of the second comparator 214 is C-. The two-bit output C+, C- represents three logic states 10, 00 and 01 (or ternary values) of the outputs of the first comparator 212 and the second comparator 214 and the states correspond
10 to integer values 1, 0 and -1 respectively. The two-bit output can usefully overcome abrupt oscillation between 1 and -1 when using the delta modulation technique as shown in the ADC 102 of FIG. 1A. Therefore, SNR for the quantizer device 208 can be improved.

In the exemplary embodiment, the quantizer device 208 further comprises a digital logic
15 component 224. The outputs of the two comparators 212, 214, are coupled to the digital logic component 224. The digital logic component 224 is disposed prior to providing the final N-bit output 216 of the ADC 202. The final N-bit output 216 is the digital output signal of the ADC 202. In the exemplary embodiment, the digital logic component 224 is provided to perform at least integration of the outputs of the two comparators 212, 214. The digital logic component 224 is
20 also provided to perform DEM (dynamic element matching) within the digital logic component 224.

In the exemplary embodiment, the N-bit output 216 of the ADC 202 can be determined by a setting of the voltage reference V_{REF} . For example, for a 7-bit output at the output 216, the V_{REF}
25 is chosen as $4/7 * V_{DD}$ (where V_{DD} is the full scale input voltage, e.g. applied to the drain of transistors).

In the exemplary embodiment, the outputs of the first comparator 212 and the second comparator 214 (e.g. the two-bit output C+, C-) are coupled via a feedback path/loop connection
30 218 to an input 220 of the last integrator stage of the modulator 204, e.g. comprising the last integrator 206. The feedback loop connection 218 can facilitate transmission of quantized outputs of the first comparator 212 and the second comparator 214 as a comparator feedback signal to the input 220 of the integrator stage.

35 In the exemplary embodiment, there are two observable differences with the feedback loop connection 218 as compared to FIG. 1A. That is, the internal feedback in the device 208 is now the 2-bit comparator output instead of the integrated N-bit feedback (e.g. the N-bit output

216). Further, the position of feedback is provided to the input 220 of the integrator stage (e.g. of an analog integrator) rather than at an output as shown in FIG. 1A. In the exemplary embodiment, the comparator output signal is thus provided to the input 220 of the integrator 206. The inventor recognises that the feedback loop connection 218 not only reduces the output swing required of the integrator 206 (i.e. output at node B 221 of FIG. 2) but also improves the stability of the sigma delta loop 202.

Therefore, with the above arrangement, it may be observed that an analog integrator (e.g. the integrator 206) is embedded in a delta modulation architecture (at the input stage of the quantizer device 208).

In addition, the feedback loop connection 218 comprises a gain stage 222 inserted within the loop connection 218 prior to the outputs of the first comparator 212 and the second comparator 214 being provided to the input 220. Thus, a gain can be provided to the comparator feedback signal. In the exemplary embodiment, the gain stage 222 can improve stability of the sigma delta loop of the modulator 204 as the integrator swing at node B 221 cannot exceed $2 \cdot V_{REF}$. In the exemplary embodiment, at the input 220, the first integrator 226 outputs at point A are summed and a subtraction of the gain stage 222 output (i.e. of the comparator feedback signal) is performed.

In the exemplary embodiment, the internal feedback of the outputs of the first comparator 212 and the second comparator 214 (e.g. the two-bit output C+, C-) via the feedback loop connection 218 to the input 220 may be implemented using any type of N-bit (digital-to-analog converters) DACs such as resistive DAC, capacitive DAC and/or current DAC types. For example, if switched capacitors are used, the feedback DACs is capacitive. An example implementation is provided in FIG. 3 which illustrates an implementation of the functions of components 220, 222, and the integrator 206.

FIG. 3 is an exemplary illustration of switching capacitor circuits used for DAC in the exemplary embodiment. Such DAC may be termed a multiplying DAC (MDAC). Switching capacitor circuits 302, 304 are provided as a parallel capacitor network for processing the two-bit output C+, C-. For the switching capacitor circuit 302, individual capacitors C_1 322, C_2 324 are connected or disconnected with switches e.g. 306 based on the inputs 308, e.g. of C+, C-. The switching capacitor circuit 304 comprises a substantially identical arrangement to the switching capacitor circuit 302, the switching capacitor circuit 304 hidden from view in FIG. 3. The last integrator 206 in FIG. 2 is comprised of an amplifier 310, the switching capacitor circuits 302 and 304 and a pair of capacitors 318 and 320. The amplifier 310 has a first input 312, a second input

314, and outputs e.g. 316. The outputs e.g. 316 are coupled to the quantizer device 208, i.e. coupled to the inputs of the comparators 212, 214 of FIG. 2. The amplifier 310 includes the capacitor 318, i.e. a feedback capacitor 318, with a first end coupled to the first input 312 of the amplifier 310, and a second end coupled to the outputs e.g. 316. The amplifier 310 includes the
5 capacitor 320, i.e. a second feedback capacitor 320, with a first end coupled to the second input 314 and a second end coupled to the outputs e.g. 316. In the exemplary embodiment, the gain stage 222 may be based on a difference in DAC values for input and feedback i.e., the ratio between capacitors C1 322 and C2 324. The ratio is the gain (compare gain stage 222 of FIG. 2). In the exemplary implementation, C2 324 is the DAC (or the analog-to-digital converter)
10 component.

In the exemplary implementation, Vin 326 and Vip 328 are outputs of the first integrator 226 at point A of FIG. 2. CB+ and CB- are reference voltage values for the integrator 226 of FIG. 2. At FIG. 2, at the input 220, the outputs at the first integrator 226 at point A are summed and
15 the output of the gain stage 222 are subtracted and this function is implemented by the switching capacitor circuits 304 and 302. For example, the subtraction happens in the charge domain between capacitors C2 324 and C1 322 of the switched capacitor circuit 302.

In the exemplary implementation, C+ and C- are the two bit outputs from the comparators
20 212, 214 of the quantizer device 208 transmitted via the feedback loop connection 218 of FIG. 2. CB+ and CB- are the respective inverted values for the same. For the switched capacitor circuit 302, the subtraction between Vip 328 and C+/C- happens by subtracting the charges in capacitors C1 322 and C2 324 of the switched capacitor circuit 302. The charge in C1 322 is caused by Vip and the charge in C2 324 is caused by C+ and C-. The ratio between C1 322 and C2 324 provides
25 the gain stage 222 in FIG. 2. For the switched capacitor circuit 304, the subtraction between Vin 326 and CB+/CB- is substantially identical, i.e. it happens by subtracting the charges in respective capacitors (not shown) in the switch capacitor circuit 304. The charge in a first capacitor in the switch capacitor circuit 304 (compare C1 322) is caused by Vin 326 and the charge in a second capacitor in the switch capacitor circuit 304 (compare C2 324) is caused by CB+ and CB-. The
30 switched capacitor circuit 304 provides the differential signal equivalent to the switched capacitor circuit 302.

In the exemplary implementation, the circuitry shown in FIG. 3 including the switched capacitor circuits 302, 304 can provide the gain stage 222 of FIG. 2 and a digital-to-analog
35 converter to perform digital-to-analog conversion of the quantized outputs C+, C- of the plurality of comparators 212, 214 of FIG. 2. The circuitry shown in FIG. 3 is disposed within the feedback loop connection 218 of FIG. 2. The outputs, e.g. 316 are provided at node B

221 of FIG. 2. The gain stage 222 factored into the subtraction of V_{in} 326 and V_{ip} 328 (against $C+/C-$ and $CB+/CB-$) can improve the stability of the sigma delta loop of the modulator 204 as the integrator swing at node B 221 of FIG. 2 cannot exceed $2 \cdot V_{REF}$. The outputs, e.g. 316 are then processed by the first comparator 212 and the second comparator 214 of FIG. 2, i.e. compared against the voltage reference V_{REF} .

Referring to FIG. 2, the quantizer device 208 uses delta modulation, where the comparator output 2-bit (for 2 comparators) or N-bit (for N comparators) represents the change in the input (at node B 221) with respect to a previous sample, i.e. if $C+, C-$ is 1,0 it means that the input has gone up more than one quantization level and hence, the output (of the quantizer device 208) is to be appended with +1, if $C+, C-$ is 0,0 then the change in input is less than one quantization level and the output (of the quantizer device 208) should remain the same. If $C+, C-$ is 0,1 then the input has reduced and the output (of the quantizer device 208) should also be reduced.

FIG. 4 is a diagram illustrating waveforms obtained from the ADC of FIG. 2 in the exemplary embodiment. Reference numerals used in FIG. 2 are maintained in the description of FIG. 4 for consistency. An analog input signal 402 is shown. The analog input signal 402 is a sinusoidal wave. The input signal 402 is obtained at the input node 205. An N-bit digital output waveform 404 is combined with the input signal 402. The N-bit digital output waveform 404 represents the N-bit digital output obtained at the N-bit output 216 of a previous sample. At node B 221, two output waveforms 406, 407 are obtained. The output waveform 406 showing a dashed line is the node B output transmitted to the first comparator 212 and the output waveform 407 showing a solid line is the node B output transmitted to the second comparator 214. The output waveforms 406, 407 are differential signals, i.e. they are the same and move opposite to each other (compare FIG. 3; the switched capacitor circuit 304 provides the differential signal equivalent to the switched capacitor circuit 302). Each of the output waveforms 406, 407 are illustrating the differences between the analog input signal 402 and the N-bit digital output waveform 404. A V_{REF} line 408 is shown to illustrate the quantization consideration by the first comparator 212 and the second comparator 214 of FIG. 2. A 2-bit comparator output waveform 410 is provided showing the changes in quantization levels of the N-bit digital output waveform 404. For ease of understanding, at each sampling instance (denoted by the vertical lines), if the output waveform 407 exceeds the V_{REF} line 408 at the respective sampling instance, the output of the comparators 212, 214 of FIG. 2 is 0,1 or -1. If the output waveform 406 exceeds the V_{REF} line 408 at the respective sampling instance, the output of the comparators 212, 214 of FIG. 2 is 1,0 or +1. If neither of the output waveforms 406, 407 exceed the V_{REF} line 408, the output of the comparators 212, 214 of FIG. 2 is 0,0 or 0. For example, at segment 412, at the first vertical line 411 or at the sampling instance, neither of the output waveforms 406, 407 exceed the V_{REF} line

408, as a result, it is shown the integer value of 0 at this segment 412. At segment 414, at each vertical line (sampling instance), the output waveform 407 exceeds the V_{REF} line 408, as a result, it is shown the integer value is -1 at this segment 414. At segment 416, at the vertical line, neither of the output waveforms 406, 407 exceed the V_{REF} line 408, as a result, it is shown the integer value of 0 at this segment 416. At segment 418, at each vertical line (sampling instance), the output waveform 406 exceeds the V_{REF} line 408, as a result, it is shown the integer value is 1 at this segment 418. At segment 420, at the vertical line, the output waveform 407 exceeds the V_{REF} line 408, as a result, it is shown the integer value is -1.

FIG. 5 is a fast Fourier transform of the output of the ADC 202 of FIG. 2. It can be observed that, with the structure of FIG. 2, the FFT spectrum 502 has reduced harmonics and improved noise floor, as compared to the FFT spectrum shown in FIG. 1B.

FIG. 6 shows output waveforms from the ADC 202 of FIG. 2. The output waveforms are for signal amplitude as a function of time. A node B output waveform 602 shows the differential output obtained at node B 221 of FIG. 2. A quantizer output waveform 604 shows a quantizer output of the quantizer device 208 of FIG. 2. It can be observed that with the internal N-bit (e.g. 2-bit) feedback (compare feedback loop connection 218), the stability of the ADC 202 system has improved, as compared to that of FIG. 1A.

In the exemplary embodiment, the inventor recognizes that the ADC of FIG. 2 is able to utilize a single voltage reference, i.e. V_{REF} . That is, a single voltage reference is provided to, for example, the two comparators 212, 214. The use of a single voltage reference can reduce design complexity as well as provide potentially a technical advantage over the present designs (such as Flash ADC). It is recognised by the inventor that in conventional designs, creating more than one voltage reference increases the power consumption as each reference has to be adequately buffered. Having more than one voltage reference also increases chip area. Further, creating a buffer design for each voltage reference can also be appreciably complex as the buffer designs should support a large input common mode voltage (rail to rail).

In the exemplary embodiment, it may be observed that in addition to the internal feedback (via feedback loop connection 218) provided by the quantizer device 208, the digital logic component 224 also provides for linearity for the quantizer device 208 output as the digital logic component 224 can perform integration and inherent DEM for the quantizer device 208 output, thus eliminating a need for an additional DEM block beyond the N-bit output 216 of the ADC 202.

In the exemplary embodiment, the 2-bit output from the comparators, which can be interpreted as integer values of the logic states of the output +1, 0 and -1, can be converted to N-bits by continuous integration using digital logic. See e.g. the N-bit output 216. The level/number N can be determined by the choice of voltage reference. For example, for a voltage reference of $4/7 \cdot V_{DD}$, the number of bits that can be achieved is 7, and for a 15-bit output, a voltage reference of $8/15 \cdot V_{DD}$ may be used and so on. For example, the denominator can determine the number of states while the number is the half-way point or midpoint. For a quantizer with $(2n+1)$ states, the midpoint is $(n+1)/(2n+1)$ where n is any integer. The exemplary embodiment is appreciably different from conventional delta modulation where integration results in a so-called N-bit thermometer code which does not contain DEM patterns in such a code. That is, additional DEM is typically needed for the conventional devices.

In the following description, two example techniques to achieve DEM with CLA (Clocked Level Averaging) and with DWA (Data Weighted Averaging), i.e. CLA-DEM and DWA-DEM are discussed. In the example techniques, only a $\frac{1}{2}$ clock cycle delay is incurred. The example techniques are implemented with a view of obtaining the DEM patterns as desired, as exemplarily shown in Table 3 below. In the example techniques, a shift register-based structure is used so that DEM may be implemented along with accumulation/counting of the comparator outputs.

FIG. 7 is a schematic diagram for illustrating a digital logic component in an exemplary embodiment for implementing digital integration and CLA-DEM. The digital logic component 702 comprises two AND gates 704, 706, each coupled to a respective output of a comparator (compare the first comparator 212 and the second comparator 214 of FIG. 2). In the exemplary embodiment, the AND gate 704 is coupled to an output C- 703 of a comparator and the AND gate 706 is coupled to an output C+ 705 of another comparator. The digital logic component 702 further comprises a plurality of cyclic shift registers. In the exemplary embodiment, two N-bit cyclic shift registers 708, 710 are provided. In addition, the digital logic component 702 comprises a digital member 716 to process a state difference of the cyclic shift registers 708, 710. In the exemplary embodiment, the digital member is an XOR gate 716. The XOR gate 716 is coupled to the outputs 718, 720 of the respective cyclic shift registers 708, 710. In the exemplary embodiment, the digital logic component 702 can convert 2-bits (from the two comparators) to N-bits.

In the exemplary embodiment, the shift registers 708, 710 may be implemented using flip-flops (bistable gates).

In the exemplary embodiment, the digital logic component 702 utilises the comparator outputs C+, C- to perform integration and DEM generation in combination, within the digital logic component 702, i.e. inherent DEM is achieved. Excess loop delay from DEM generation may be avoided with the digital logic component 702.

In the exemplary embodiment, the two N-bit cyclic shift registers 708, 710 are each clocked by a gated clock, see clock inputs 712, 714. The clock gating is achieved using the respective outputs of the comparators C+, C-. An input of the AND gate 704 and an input of the AND gate 706 are coupled to a system clock signal CLK 722.

The XOR gate 716 is provided to generate the state difference between the two N-bit cyclic shift registers 708, 710. Thus, the XOR gate 716 generates an N-bit output 724 (compare N-bit output 216 of FIG. 2).

In the exemplary embodiment, the shift registers 708, 710 complete one round of shifting at a rate of about $1/(2*N)*F_{CLK}$. Thus, the output N-bit digital code or the N-bit output 724 is rotated at about $1/(N)*F_{CLK}$ resulting in a CLA-DEM rotation pattern. The CLA-DEM rotation pattern may be exemplarily discussed in Table 3 below. This N-bit output code or the N-bit output 724 thus assists to alleviate DAC nonlinearity for a quantizer device.

The circuit shown in FIG. 7 may be used to, for example, implement a 2-bit to 4-bit conversion, of the C+/C- comparators outputs to the N-bit output 724. Table 1 below is a table for illustrating an exemplary 2-bit to 4-bit conversion that may be carried out by the digital logic component 702 described with reference to FIG. 7. The terms and reference numerals in the column headers of Table 1 refer to the terms and components described with reference to FIG. 7 respectively.

30

C+, C-	714/712	720	718	724	Integer equivalent
0,0	0/0	0000	1100	1100	0
0,1	0/1	0000	1110	1110	1
0,0	0/0	0000	1110	1110	1
1,0	1/0	1000	1110	0110	0

1,0	1/0	1100	1110	0010	-1
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Table 1: Example implementation of a 2-bit to 4-bit conversion.

In the example, in a 2-bit to 4-bit conversion process, shift registers 708, 710 of FIG. 7 shift up if there is a respective clock pulse at clock inputs 714, 712, and these inputs 714, 712 depend on output C+ 705 and output C- 703 respectively. Further, at the most right column in Table 1, there is provided an integer equivalent number of the 4-bit output which shows the differences in the number of 1's and 0's at N-bit output 724.

In the example, in the initial state upon reset (see line 1 of Table 1), based on output C+ 705 and output C- 703 being 0,0, the clock pulse at clock inputs 714/712 is 0/0. In this initial state, outputs 720 and 718 are provided as 0000 and 1100 respectively. Further, the 4-bit output 724 is 1100 and the integer equivalent number is 0.

When output C+ 705 and the output C- 703 is 0,1 (see line 2 of Table 1), at CLK 722 pulse, the clock pulse at clock inputs 714/712 is 0/1. In this scenario, output 720 remains as 0000 while output 718 changes/flips/rotates to 1110. Further, 4-bit output 724 changes to 1110 (due to XOR gate 716 and output 718). The integer equivalent number is 1.

When output C+ 705 and output C- 703 returns to 0,0 (see line 3 of Table 1), at CLK 722 pulse, the clock pulse at clock inputs 714/712 is 0/0. In this scenario, output 720 remains as 0000 and output 718 remains as 1110 respectively. Further, 4-bit output 724 remains as 1110 and the integer equivalent number remains as 1.

When output C+ 705 and output C- 703 changes to 1,0 (see line 4 of Table 1), at CLK 722 pulse, the clock pulse at clock inputs 714/712 is 1/0. In this scenario, output 720 changes/flips/rotates to 1000 while output 718 remains as 1110. Further, 4-bit output 724 changes to 0110 (due to XOR gate 716). The integer equivalent number changes to 0.

When output C+ 705 and output C- 703 is again 1,0 (see line 5 of Table 1), at CLK 722 pulse, the clock pulse at clock inputs 714/712 is 1/0. In this scenario, output 720 changes/flips/rotates to 1100 while output 718 remains as 1110. Further, 4-bit output 724 changes to 0010 (due to XOR gate 716). The integer equivalent number changes to -1.

FIG. 8 shows a set of waveforms obtained from the digital logic component of FIG. 7. The waveforms, e.g. 802, 804, show a 7-bit output rotated at a frequency of about 50Hz. Each waveform, e.g. 802, 804, shows each of the bits in the N-bits output 724 of FIG. 7.

Thus, the seven waveforms in FIG. 8 are for each of the 7 bits of the N-bits output 724. It can be observed that bit activation is rotated between each bits. It can be observed that not all bits are flipping at the same time and flipping is performed one at a time.

5 In the exemplary embodiment, since the DEM logic is inherently implemented in the digital logic component 702 of FIG. 7, the inventor recognize that no additional delay is added to a quantizer device system, leading to stable operation of ADC.

10 The digital logic component 702 of FIG. 7 can perform integration in about up to half a clock cycle and can perform the DEM in about a remaining half a clock cycle. For example, the digital logic component 702 of FIG. 7 may then comply with a requirement of one clock cycle to provide an output of a quantizer device (compare the output 216 of the quantizer device 208), i.e. the output can be feed back to an input stage of a system/device (compare the input node 205 of the ADC 202) for processing with an input signal of the next clock cycle.

15 As described, the digital logic component 702 of FIG. 7 can perform a digital integration based on the outputs of the two comparators and the DEM is based on CLA (Clocked Level Averaging).

20 The inventor recognizes that even though CLA-DEM suppresses DAC non-linearity, it may in some cases increase the noise floor of the output and may reduce SNR. Hence, alternatively, Barrel shifting DEM or DWA-DEM can be used e.g. if a higher resolution is desired.

25 FIG. 9A is a schematic diagram for illustrating a digital logic component in an exemplary embodiment for implementing digital integration and DWA-DEM. FIG. 9B is a flow sheet providing an algorithm for data generation for digital integration in the exemplary embodiment.

30 The digital logic component 900 comprises an integration block 902 coupled to a DWA-DEM generation block 904. Data may flow from the integration block 902 to the DWA-DEM generation block 904 via connection 916. Data may flow from the DWA-DEM generation block 904 to the integration block 902 via connection 918.

35 The integration block 902 comprises a plurality of unit cells e.g. 906, 908. In the exemplary embodiment, the connection of the unit cells e.g. 906, 908 and the logical implementation of each single unit cell forms a digital integrator for a quantizer device (compare quantizer device 208 of FIG. 2).

In the exemplary embodiment, the plurality of unit cells e.g. 906, 908 are implemented using digital logic and may be implemented using flip-flops (bistable gates). The unit cells e.g. 906, 908 are synchronised by a system clock clk 910.

5

In the exemplary embodiment, the digital logic component 900 utilises respective outputs C+, C- of comparators (compare the first comparator 212 and the second comparator 214 of FIG. 2 providing the 2-bit outputs) to perform integration and DEM generation in combination, within the digital logic component 900, i.e. inherent DEM is achieved. Excess
10 loop delay from DEM generation may be avoided with the digital logic component 900. The desired DWA-DEM rotation pattern may be exemplarily discussed in Table 3 below.

Each of the unit cells e.g. 906, 908 are coupled to the outputs of the comparators C+ 912 and C- 914. The data in the unit cells e.g. 906, 908 are rotated depending upon the
15 values of C+ 912 and C- 914, for the data in the unit cells to undergo digital integration.

In the exemplary embodiment, the unit cells e.g. 906, 908 are coupled to each other in an ordered manner. Each of the unit cells e.g. 906, 908 has its inputs coupled to a previous-ordered unit cell, a next-ordered unit cell and to its own output. For example, for unit cell 906,
20 it may be denoted as a zero-th cell or N0. The next ordered unit cell 919 may be denoted as N1. The unit cell 919 can receive as its inputs the output of the unit cell 906 (or N0), see Q<0>, the output of the next-ordered unit cell, see Q<2> and its own output D<1>. The output of each unit cell is based on the values of C+ 912 and C- 914 (i.e. the outputs of comparators of a quantizer device). Thus, each unit cell e.g. 906 is capable of outputting data from a
25 previous-ordered unit cell or from a next-ordered unit cell or its own data, the unit cell output being dependent on the quantized outputs of the plurality of comparators. The algorithm for operating the unit cells e.g. 906, 908 is provided as a flow sheet in FIG. 9B.

FIG. 9C is a schematic diagram illustrating the DWA-DEM generation block 904 in the
30 exemplary embodiment. The DWA-DEM generation block 904 is a combinatorial logic circuit that generates a DWA pattern from the present/current state of the N-bit unit cells outputs using a series of multiplexer units implementing mux logic connected as shown in FIG. 9C.

In FIG. 9C, the DWA-DEM generation block 904 comprises a plurality of multiplexer
35 units e.g. 920, 922 connected in series. The DWA-DEM generation block 904 functions to realign inputs to the DWA-DEM generation block 904 i.e. Q<0:N> 924 to produce an output of D<0:N> 926. In the example, the realignment is performed using the multiplexer units e.g.

920, 922. For example, a multiplexer unit 920 can conduct multiplexing between $Q<1:N>$, $Q<0>$ or $Q<0:N>$ based on the control signal input $Q<0>$ 928. It is explained that the notation D shown at the inputs of the multiplexer unit 920 can be referred to using notation Q, and that the notation D reflected at this portion is different from the final output $D<0:N>$ 926. Similarly, a next multiplexer unit 922 realigns the output of the multiplexer unit 920 i.e. $Q<1:N>$ 930, based on the control signal input $Q<1>$ 932. As such, the multiplexer units e.g. 920, 922 are identical or similar cells/units acting on different input signals and control bits, e.g. 928, 932. In the example, the multiplexing and realignment continues N times until the final output $D<0:N>$ 926 is produced.

10

With the digital logic component 900, DEM is inbuilt (or inherent) along with digital integration causing no additional delay. Table 2 below shows a 4-bit output based on a 2-bit comparator output.

C_1, C_0	$Q<0:3>$	$D<0:3>$
	0001	1000
0,0	1000	0100
1,0	0110	1001
0,1	0001	1000

15

Table 2: Example implementation for 4-bit output with digital integration and DWA-DEM.

In the above examples, 2-bit outputs with two comparators have been shown. In some exemplary embodiments, having an N-Bit output with N-comparators can apply correspondingly. That is, instead of a difference in input of 1,0 and -1, the input could vary from $-N$, $-N+1 \dots 0 \dots$ to $N-1$ and N . Hence, the output may be appended correspondingly. For example, see Table 3 below.

In addition, in the above examples, for a two bit case (or 2 comparators), a +1 indicates a change in 1 flip flop value in shift registers. In other exemplary embodiments, for N-comparators, a +N indicates a change in N flip-flop outputs. Thus, changing from a 2-bit implementation to an N-bit implementation is a shear extension.

In the above examples, the digital logic component comprises one or more state-machine based digital logic gates (e.g. flip flops) and the digital logic component is capable

of utilising the quantized outputs of the plurality of comparators to change a state of the one or more state-machine based digital logic gates to perform both digital integration and dynamic element matching (DEM) together within the digital logic component.

5 In the above described examples, desired DEM rotation patterns may be obtained. It will be appreciated that other digital logic circuits may also be possible to obtain the desired DEM rotation patterns. In the digital logic component of exemplary embodiments, the digital integration and inherent DEM are performed based on the outputs of the plurality of comparators (e.g. 2 comparators or N comparators).

10

Table 3 below is a sample truth table for an exemplary 2-bit to 8-bit conversion. The truth table shows different comparator outputs for a 2-bit case (C+,C-) for without DEM, with CLA-DEM and with DWA-DEM. In the example, the 2-bits comparator outputs are integrated to 8-bits. The digital integration and inherent DEM provided may be implemented by the digital logic component of exemplary embodiments (e.g. compare FIG. 7 and FIGs. 9A to 9C).

15

Comp Output	Without DEM		With CLA DEM		With DWA DEM	
	prev state	next state	prev state	next state	prev state	next state
1,0	10000000	11000000	10000000	01100000	10000000	01100000
1,0	11000000	11100000	01100000	00111000	01100000	00011100
0,0	11100000	11100000	00111000	00011100	00011100	10000011
0,1	11100000	11000000	00011100	00001100	10000011	01100000
0,1	11000000	10000000	00001100	00000100	01100000	00010000

Table 3: sample truth table for an exemplary 2-bit to 8-bit conversion

20

From Table 3, without DEM, the output appears like a so-called thermometer code.

For CLA-DEM, the output code is rotated at 1-bit per cycle. For example, for a comparator or comp output of 1,0, the next state can be seen as adding "1" and rotating one place; for 0,0, there is a rotation of one place for the next state; and for 0,1, the next state can be seen as dropping "1" and rotating one place.

25

Thus, the desired CLA-DEM pattern for a next state is based on a value of the previous state (adding or dropping "1" or maintaining) and followed by a rotation of one place.

30

For DWA-DEM, the output is shifted as a barrel shifting pattern. For example, the number of places rotated is equal to the last value of the code itself, i.e. if the last/previous

code is 0111000 then the code is rotated 3 places; i.e. 0000111 for 0,0 input (or comparators' outputs). As for 1,0 and 0,1, a value '1' is added or subtracted respectively from the previous state respectively along with rotation of 3 places, in this case for value of 3. For example, for the first line under DWA-DEM, the next state has a '1' added with a rotation of 1 place. For the second line, the next state has a '1' added with a rotation of 2 places. For the third line, there is a rotation of 3 places. For the fourth line, the next state has a '1' subtracted with a rotation of 3 places. For the fifth line, the next state has a '1' subtracted with a rotation of 2 places.

Thus, the desired DWA-DEM pattern for a next state is based on a value of the previous state (adding or dropping "1" or maintaining) and followed by a rotation of a number of places determined by the value of the previous state.

In various exemplary embodiments, one reason for sub clock cycle delay for DEM (1/2 clock cycle in the described example techniques) may be as follows. The output of a sigma delta modulator for feedback is set to be generated at 1 clock cycle. The integrators in exemplary embodiments take up $\frac{1}{2}$ cycle to integrate, and DEM takes up the remaining $\frac{1}{2}$ cycle thus complying to the requirement of 1 clock cycle. The $\frac{1}{2}$ cycle is ensured in the DEM block (whether it is CLA-DEM or DWA-DEM) by use of flip-flop components (digital gate components).

FIG. 10 is an output spectrum obtained from a second order sigma delta modulator using a quantizer device of an exemplary embodiment. The spectrum is obtained as amplitude as a function of frequency. The spectrum 1002 is superimposed with three different scenarios.

In a first scenario, the quantizer device (e.g. compare quantizer device 208 of FIG. 2) has its output processed without DEM (i.e. only digital integration). In a second scenario, the quantizer device (e.g. compare quantizer device 208 of FIG. 2) has its output processed with CLA-DEM (i.e. with digital integration and inherent CLA-DEM; compare digital logic component 224 of FIG. 2 and digital logic component 702 of FIG. 7). In a third scenario, the quantizer device (e.g. compare quantizer device 208 of FIG. 2) has its output processed with DWA-DEM (i.e. with digital integration and inherent DWA-DEM; compare digital logic component 224 of FIG. 2 and digital logic component 900 of FIG. 9A).

For the first scenario, without any DEM, a waveform 1004 that is oscillating and having multiple spikes can be observed. For the second scenario, with CLA-DEM, a waveform 1006

with small white spikes can be observed. For the third scenario, with DWA-DEM, a waveform 1008 with the grey part can be observed.

It can be observed that using DEM techniques can eliminate output nonlinearity from a DAC process. Further, it can be observed that DWA-DEM has a lower noise floor than CLA_DEM for a given DAC nonlinearity. In addition, it is recognized that implicit DEM does not cause a change in spectrum which indicates that the output with inherent DEM is stable.

In the above described exemplary embodiments, a quantizer device comprising two comparators has been described. It will be appreciated that the exemplary embodiments are not limited as such, and N number of comparators may be used instead. The quantizer device may be extended to provide more output bits (for undergoing digital integration and inherent DEM). The quantizer device may also be extended for a higher order case where the input to the quantizer device exceeds $2 \cdot V_{REF}$. The $2 \cdot V_{REF}$ case is shown with the two comparators of FIG. 2 with V_{REF} provided to each comparator.

FIG. 11 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in another exemplary embodiment. The ADC 1102 is substantially similar to the ADC 202 of FIG. 2 but with more numbers of comparators. The quantizer device of this exemplary embodiment is an extended version for a higher order sigma modulator and/or to provide more number of bits.

In the ADC 1102, a quantizer device 1104 is provided. The quantizer device 1104 comprises four comparators 1106, 1108, 1110, 1112, each coupled to an output 1116 of an integrator 1114 of a sigma delta modulator. The four comparators 1106, 1108, 1110, 1112 can perform four-bit quantization on the output 1116. In the exemplary embodiment, a first comparator 1106 and a fourth comparator 1112 each compare against a voltage reference V_{REF2} while a second comparator 1108 and a third comparator each compare against a voltage reference V_{REF} . The four-bit output represents five logic states 1100, 0100, 0000, 0010, 0011 of the four comparators 1106, 1108, 1110, 1112 and the states correspond to integer values +2, +1, 0, -1 and -2 respectively.

In the exemplary embodiment, the quantizer device 1104 further comprises a digital logic component 1118. The outputs of the comparators 1106, 1108, 1110, 1112 are coupled to the digital logic component 1118. The digital logic component 1118 is disposed prior to providing the final N-bit output 1120 of the ADC 1102. In the exemplary embodiment, the digital logic component 1118 is provided to perform at least integration of the outputs of the comparators

1106, 1108, 1110, 1112. The digital logic component 1118 is also provided to perform DEM (dynamic element matching) within the digital logic component 1118.

5 In the exemplary embodiment, the outputs of the comparators 1106, 1108, 1110, 1112 (i.e. the 4-bit output) are coupled via a feedback path/loop connection 1122 to an input 1124 of the last integrator stage of the modulator, e.g. comprising the last integrator 1114. The feedback loop connection 1122 can facilitate transmission of quantized outputs of the comparators 1106, 1108, 1110, 1112 as a comparator feedback signal to the input 1124 of the integrator stage.

10

Therefore, with the above arrangement, it may be observed that an analog integrator (e.g. the integrator 1114) is embedded in a delta modulation architecture (at the input stage of the quantizer device 1104).

15 In addition, the feedback loop connection 1122 comprises a gain stage 1126 inserted within the loop connection 1122 prior to the outputs of the comparators 1106, 1108, 1110, 1112 being provided to the input 1124. Thus, a gain can be provided to the comparator feedback signal. In the exemplary embodiment, the gain stage 1126 is provided with a digital-to-analog conversion/converter. In the exemplary embodiment, the internal feedback of the outputs of the comparators 1106, 1108, 1110, 1112 (e.g. the four-bit output) via the feedback loop connection 20 1122 to the input 1124 may be implemented using any type of N-bit (digital-to-analog converters) DACs such as resistive DAC, capacitive DAC and/or current DAC types. Compare FIG. 3.

25 The inventor recognises that for higher order delta sigma modulators, the variance of the input to the quantizer device may be larger and may thus saturate the quantizer device. To mitigate such saturation, the total number of comparators is increased and the number of feedback bits (the quantized output) is also increased. The inventor recognises that additional power and chip area is needed when the number of components increase. The desired quantization is carefully considered for each design requirement.

30

In the exemplary embodiments, for example having four comparators coupled to a last integrator stage, two different voltage references (i.e. 2 Vrefs) may be used. For scaling the architecture for higher orders, additional voltage references (or Vref) may be used.

35 In the above described exemplary embodiments, a quantizer device is used to quantize a differential output of a last integrator stage. It will be appreciated that the exemplary embodiments are not limited as such. For example, in other exemplary

embodiments, the quantization may be performed on a single-ended output of a last integrator stage.

FIG. 12 is a schematic block diagram of an analog-to-digital converter (ADC) comprising a quantizer device in another exemplary embodiment. The ADC 1202 is substantially similar to the ADC 202 of FIG. 2 but with the comparators comparing against different voltage references.

In the ADC 1202, a quantizer device 1204 is provided. The quantizer device 1204 comprises a first comparator 1206 and a second comparator 1208, each coupled to an output 1216 of an integrator 1214 of a sigma delta modulator. The first comparator 1206 and the second comparator 1208 can perform two-bit quantization on the output 1216. In the exemplary embodiment, the output 1216 is a single-ended output (as contrasted to a differential signal output at node B of FIG. 2).

15

In the exemplary embodiment, complementary references (V_{REF} and $VDD-V_{REF}$) instead of a single reference (compare FIG. 2) may be used to compensate for the missing differential signal at the output 1216.

20

In the exemplary embodiment, the first comparator 1206 is provided to compare against a voltage reference V_{REF} while the second comparator 1208 is provided to compare against a voltage reference $VDD-V_{REF}$. The two-bit output represents three logic states 10, 00 and 01 (or tri-states) of the outputs of the first comparator 1206 and the second comparator 1208 and the states correspond to integer values 1, 0 and -1 respectively.

25

In the exemplary embodiment, the quantizer device 1104 further comprises a digital logic component 1218. The outputs of the comparators 1206, 1208 are coupled to the digital logic component 1218. The digital logic component 1218 is disposed prior to providing the final N-bit output 1220 of the ADC 1202. In the exemplary embodiment, the digital logic component 1218 is provided to perform at least integration of the outputs of the comparators 1206, 1208. The digital logic component 1218 is also provided to perform DEM (dynamic element matching) within the digital logic component 1218.

In the exemplary embodiment, the outputs of the comparators 1206, 1208 (i.e. the 2-bit output) are coupled via a feedback path/loop connection 1222 to an input 1224 of the last integrator stage of the modulator, e.g. comprising the last integrator 1214. The feedback loop

35

connection 1222 can facilitate transmission of quantized outputs of the comparators 1206, 1208 as a comparator feedback signal to the input 1224 of the integrator stage.

Therefore, with the above arrangement, it may be observed that an analog integrator (e.g. the integrator 1214) is embedded in a delta modulation architecture (at the input stage of the quantizer device 1204).

In addition, the feedback loop connection 1222 comprises a gain stage 1226 inserted within the loop connection 1222 prior to the outputs of the comparators 1206, 1208 being provided to the input 1224. Thus, a gain can be provided to the comparator feedback signal. In the exemplary embodiment, the gain stage 1226 is provided with a digital-to-analog conversion/converter. In the exemplary embodiment, the internal feedback of the outputs of the comparators 1206, 1208 (e.g. the two-bit output) via the feedback loop connection 1222 to the input 1224 may be implemented using any type of N-bit (digital-to-analog converters) DACs such as resistive DAC, capacitive DAC and/or current DAC types. Compare FIG. 3.

In the described exemplary embodiments, the inventor recognises that a novel architecture has been provided that embeds an analog integrator in a delta modulation structure. This can lead to a low output swing for the integrators, i.e. a multi-bit quantizer device based on delta modulation may be used in sigma delta modulators and can alleviate voltage swing at the integrators. Stability issues arising from embedding an analog integrator in delta modulation may be solved by adding an additional gain stage and use of e.g. a tri-state comparator. The tri-state delta output is feedback to an input of an integrator, instead of conventional delta modulation that uses the multibit output of a quantizer device (after integration and as final output) as feedback.

The inventor also recognises that the architecture is further novel in that it combines digital integration with DEM, i.e. provides inherent DEM prior to providing a final quantizer device output. In the described exemplary embodiments, a N-bit comparator output may be converted to a N-bit final output of the quantizer device with inherent DEM. This may minimise loop delay. For example, state-machine based digital logic can be used instead of digital integrators to produce a multi-bit digital output with DEM.

With regard to power consumption, the inventor set out to perform a quantitative estimate. A ball park number for current consumption by opamp/comparator/other blocks is used and an assumption is made that a same circuitry for a ADC is used but with different quantizer types.

It is recognised that integrators with larger output swings require larger currents in order to maintain linearity. Typically, such integrators consume about three times more current than a simple differential pair. Further, it is recognised that external/explicit DEM consumes more current than inherent DEM as the circuit blocks are reused for inherent DEM. If the current consumption for a differential pair of an integrator (I) is 2uA, comparator current (C) is 1uA, a DEM block consumes (D) 1uA, an estimate of the power consumption for a 3-bit (final output) quantizer current consumption can be as follows in Table 4.

Quantizer Type	Integrator	Comparator	DEM Block	Other blocks	Total Power	Remarks
Flash	$4 * I = 8 \mu A$	$7 * C = 7 \mu$	$D = 1 \mu A$	-	16uA	Uses a 2 stage opamp, 7 comparators and explicit DEM
SAR ADC	$4 * I = 8 \mu A$	$1 * C = 1 \mu$	$D = 1 \mu A$	Cap DAC = 1uA	10uA	Uses 2 stage opamp, 1 comparator and explicit DEM and DAC
VCO-based	$4 * I = 8 \mu A$	0	0	VCO + Current DAC = 2uA	10uA	Uses 2 stage opamp, additional VCO and DAC
Proposed exemplary embodiment	$I = 2 \mu A$	$2 * C = 2 \mu$	$D/2 = 0.5 \mu A$	Digital = 0.5uA	3uA	Uses 1 stage opamp, 2 comparators and integrated DEM for lesser power with additional digital overheads

Table 4: Comparison of estimated power consumption across different quantizer types

It can be observed from Table 4 that power consumption for an exemplary embodiment is lower than other quantizer types when used in an ADC (compare 3uA against 10uA or 16uA).

Table 5 below summarizes the characteristics demonstrated by an exemplary embodiment with respect to other quantizer types.

Quantizer Type	Quantizer Linearity	DAC Linearity	Input swing required	Speed / Bandwidth	Power
Flash	Linear	Need additional DEM	Large	Fast / Large	High
SAR ADC	Linear	Need additional DEM	Large	Moderate / Medium	Moderate
VCO-based	Non-linear	Inherent DEM	Large	Slow / Low	Moderate
Proposed exemplary embodiment	Linear	Inherent DEM	Small	Moderate / Medium	Low

Table 5: Comparison of characteristics of different quantizer types

It can be observed that an exemplary embodiment performs competitively in substantially all specifications.

5 From the described exemplary embodiments, a quantizer device may be provided that is linear in terms of quantizer linearity; incorporates inherent DEM; has a small input swing; has a moderate speed and an appreciable bandwidth and has low power consumption.

10 FIG. 13 is a schematic flowchart for illustrating a method of quantizing a signal in an exemplary embodiment.

At step 1302, a signal is inputted into a sigma delta modulator. At step 1304, a plurality of comparators is coupled to an integrator output of an integrator stage of the modulator. At
15 step 1306, multi-bit quantization of the integrator output using the plurality of comparators is performed. At step 1308, a feedback of quantized outputs of the plurality of comparators is provided to an input of the integrator stage, the quantized outputs of the plurality of comparators being a comparator feedback signal to the input of the integrator stage. At step
20 1310, a digital-to-analog conversion of the quantized outputs of the plurality of comparators is performed to generate the comparator feedback signal. At step 1312, a gain to the comparator feedback signal is provided.

With the described exemplary embodiments, a novel multi-bit quantizer device can be provided for an oversampled data converter. The exemplary embodiments using delta
25 modulation can quantize an analog signal to any number of bits, alleviate the output swing and produce thermometer code that is scrambled according to different Dynamic Element Matching (DEM) techniques such as barrel shifting DEM (DWA-DEM) or CLA-DEM. The exemplary embodiments use substantially digital logic and a reduced number of comparators for quantization, thereby reducing the overall power consumption of the quantizer device.
30 The multi-bit quantizer device can combine DEM and the delta modulation quantizes a signal within half a clock cycle thus improving loop stability by minimizing loop delay.

It has been recognised that other quantizer devices require explicit DEM and have large output swing requirements for integrators and therefore, may require linearity. With the
35 described exemplary embodiments, implicit/inherent DEM may be provided with no additional delay (thus providing better stability) and with the architecture(s), linearity requirements of opamps in a sigma delta loop may be alleviated (i.e. reduced output swing

requirements for op-amps and thus improving linearity). The described exemplary embodiments also use minimally comparators and voltage references.

5 The described exemplary embodiments may provide a low power quantizer device that can be used for realizing better and efficient sigma delta modulators (that may be used in high resolution ADC) and sensor interfaces.

The described exemplary embodiments may provide an ADC (analog-to-digital) converter comprising the quantizer device of the described exemplary embodiments. The
10 ADC converter may be a sigma-delta ADC.

For various exemplary embodiments, it is recognized by the inventor that the described exemplary embodiments may be distinctive as follows. In various exemplary embodiments, the quantizer device is directed to quantize a change in input within a clock
15 cycle (instead of expecting the actual signal and trying to quantize the signal as a whole as is otherwise done by conventional quantizers). In various exemplary embodiments, the input to the quantizer device is inherently small, due to delta modulation. This may be contrasted to some conventional quantizers that try to avoid saturation of the quantizers and minimize harmonics by using additional internal feedback, while such conventional quantizers still
20 expect the full signal. In various exemplary embodiments, DEM is embedded/inherent within the quantizer device itself, thus potentially saving time. This may be contrasted to conventional quantizers that typically use external DEM, if at all, as an additional block or process after obtaining an output of the quantizers, thus taking up more conversion time i.e. more than $\frac{1}{2}$ clock cycle, leading to loop delay.

25

The terms "coupled" or "connected" as used in this description are intended to cover both directly connected or connected through one or more intermediate means, unless otherwise stated.

30 The terms "configured to (perform a task/action)", "configured for (performing a task/action)" and the like as used in this description include being programmable, programmed, connectable, wired or otherwise constructed to have the ability to perform the task/action when arranged or installed as described herein. The terms "configured to (perform a task/action)", "configured for (performing a task/action)" and the like are intended to cover "when in use, the
35 task/action is performed", e.g. specifically to and/or specifically configured to and/or specifically arranged to and/or specifically adapted to do or perform a task/action.

The term "and/or", e.g., "X and/or Y" is understood to mean either "X and Y" or "X or Y" and should be taken to provide explicit support for both meanings or for either meaning.

5 The terms "associated with", "related to" and the like used herein when referring to two elements refers to a broad relationship between the two elements. The relationship includes, but is not limited to, a physical, a chemical or a biological relationship. For example, when element A is associated with element B, elements A and B may be directly or indirectly attached to each other or element A may contain element B or vice versa.

10 The terms "exemplary embodiment", "example embodiment", "exemplary implementation", "exemplarily" and the like used herein are intended to indicate an example of matters described in the present disclosure. Such an example may relate to one or more features defined in the claims and is not necessarily intended to emphasise a best example or any essentialness of any features.

15 The description herein may be, in certain portions, explicitly or implicitly described as algorithms and/or functional operations that operate on data within a computer memory or an electronic circuit. These algorithmic descriptions and/or functional operations are usually used by those skilled in the information/data processing arts for efficient description. An algorithm is
20 generally relating to a self-consistent sequence of steps leading to a desired result. The algorithmic steps can include physical manipulations of physical quantities, such as electrical, magnetic or optical signals capable of being stored, transmitted, transferred, combined, compared, and otherwise manipulated.

25 Further, unless specifically stated otherwise, and would ordinarily be apparent from the following, a person skilled in the art will appreciate that throughout the present specification, discussions utilizing terms such as "scanning", "calculating", "determining", "replacing", "generating", "initializing", "outputting", and the like, refer to action and processes of an instructing processor/computer system, or similar electronic circuit/device/component, that
30 manipulates/processes and transforms data represented as physical quantities within the described system into other data similarly represented as physical quantities within the system or other information storage, transmission or display devices etc.

35 Additionally, when describing some embodiments, the disclosure may have disclosed a method and/or process as a particular sequence of steps. However, unless otherwise required, it will be appreciated the method or process should not be limited to the particular sequence of steps disclosed. Other sequences of steps may be possible. The particular order of the steps

disclosed herein should not be construed as undue limitations. Unless otherwise required, a method and/or process disclosed herein should not be limited to the steps being carried out in the order written. The sequence of steps may be varied and still remain within the scope of the disclosure.

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Further, in the description herein, the word "substantially" whenever used is understood to include, but not restricted to, "entirely" or "completely" and the like. In addition, terms such as "comprising", "comprise", and the like whenever used, are intended to be non-restricting descriptive language in that they broadly include elements/components recited after such terms, in addition to other components not explicitly recited. For an example, when "comprising" is used, reference to a "one" feature is also intended to be a reference to "at least one" of that feature. Terms such as "consisting", "consist", and the like, may, in the appropriate context, be considered as a subset of terms such as "comprising", "comprise", and the like. Therefore, in embodiments disclosed herein using the terms such as "comprising", "comprise", and the like, it will be appreciated that these embodiments provide teaching for corresponding embodiments using terms such as "consisting", "consist", and the like. Further, terms such as "about", "approximately" and the like whenever used, typically means a reasonable variation, for example a variation of +/- 5% of the disclosed value, or a variance of 4% of the disclosed value, or a variance of 3% of the disclosed value, a variance of 2% of the disclosed value or a variance of 1% of the disclosed value.

Furthermore, in the description herein, certain values may be disclosed in a range. The values showing the end points of a range are intended to illustrate a preferred range. Whenever a range has been described, it is intended that the range covers and teaches all possible sub-ranges as well as individual numerical values within that range. That is, the end points of a range should not be interpreted as inflexible limitations. For example, a description of a range of 1% to 5% is intended to have specifically disclosed sub-ranges 1% to 2%, 1% to 3%, 1% to 4%, 2% to 3% etc., as well as individually, values within that range such as 1%, 2%, 3%, 4% and 5%. It is to be appreciated that the individual numerical values within the range also include integers, fractions and decimals. Furthermore, whenever a range has been described, it is also intended that the range covers and teaches values of up to 2 additional decimal places or significant figures (where appropriate) from the shown numerical end points. For example, a description of a range of 1% to 5% is intended to have specifically disclosed the ranges 1.00% to 5.00% and also 1.0% to 5.0% and all their intermediate values (such as 1.01%, 1.02% ... 4.98%, 4.99%, 5.00% and 1.1%, 1.2% ... 4.8%, 4.9%, 5.0% etc.) spanning the ranges. The intention of the above specific disclosure is applicable to any depth/breadth of a range.

It will be appreciated by a person skilled in the art that other variations and/or modifications may be made to the specific embodiments without departing from the scope of the claimed invention as broadly described. For example, in the description herein, features of different exemplary embodiments may be mixed, combined, interchanged, incorporated, adopted, 5 modified, included etc. or the like across different exemplary embodiments. For example, exemplary embodiments are not necessarily mutually exclusive as some may be combined with one or more embodiments to form new exemplary embodiments. Furthermore, it will be appreciated that while the present disclosure provides embodiments having one or more of the features/characteristics discussed herein, one or more of these features/characteristics may also 10 be disclaimed in other alternative embodiments and the present disclosure provides support for such disclaimers and these associated alternative embodiments. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. A quantizer device, the quantizer device comprising,
a plurality of comparators for coupling to an integrator output of an integrator stage of
5 a signal modulator, the plurality of comparators to perform multi-bit quantization of the
integrator output;
a feedback loop connection coupled to outputs of the plurality of comparators and
coupled to an input of the integrator stage, the feedback loop connection for transmitting
quantized outputs of the plurality of comparators as a comparator feedback signal to the input
10 of the integrator stage;
a digital-to-analog converter disposed within the feedback loop connection to perform
digital-to-analog conversion of the quantized outputs of the plurality of comparators to
generate the comparator feedback signal; and
a gain stage disposed within the feedback loop connection to provide a gain to the
15 comparator feedback signal.
2. The quantizer device as claimed in claim 1, the quantizer device further comprising a
digital logic component coupled to the plurality of comparators, the digital logic component
to receive the quantized outputs of the plurality of comparators and the digital logic
20 component disposed to provide a final output of the quantizer device.
3. The quantizer device as claimed in claim 2, wherein the digital logic component
comprises one or more state-machine based digital logic gates and the digital logic
component is capable of utilising the quantized outputs of the plurality of comparators to
25 change a state of the one or more state-machine based digital logic gates to perform digital
integration and dynamic element matching (DEM) within the digital logic component.
4. The quantizer device as claimed in claim 3, wherein the DEM is based on CLA
(Clock Level Averaging), and wherein the digital logic component comprises a plurality of
30 cyclic shift registers each clocked by a gated clock, the gated clock based on the quantized
outputs of the plurality of comparators.
5. The quantizer device as claimed in claim 4, wherein the digital logic component further
comprises a digital member to process a state difference of the plurality of cyclic shift
35 registers to produce a final N-bit output of the quantizer device.
6. The quantizer device as claimed in claim 4, wherein the digital member is a XOR gate.

7. The quantizer device as claimed in claim 3, wherein the DEM is based on DWA (Data Weighted Averaging), and wherein the digital logic component comprises a plurality of unit cells, each unit cell coupled to the quantized outputs of the plurality of comparators and each unit cell clocked based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.
8. The quantizer device as claimed in claim 7, wherein the unit cells are coupled to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.
9. The quantizer device as claimed in claim 8, wherein the digital logic component further comprises a DWA-DEM generation element that is disposed to generate a DEM pattern based on a current/present state of the each unit cell output.
10. The quantizer device as claimed in claim 9, wherein the DWA-DEM generation element comprises a plurality of multiplexer units connected in series.
11. The quantizer device as claimed in claim 1, wherein the plurality of comparators each have an input coupled to a single voltage reference and the multi-bit quantization of the integrator output is performed based on the single voltage reference.
12. A method of quantizing a signal, the method comprising,
inputting a signal into a sigma delta modulator;
coupling a plurality of comparators to an integrator output of an integrator stage of the modulator;
performing multi-bit quantization of the integrator output using the plurality of comparators;
providing a feedback of quantized outputs of the plurality of comparators to an input of the integrator stage, the quantized outputs of the plurality of comparators being a comparator feedback signal to the input of the integrator stage;
performing digital-to-analog conversion of the quantized outputs of the plurality of comparators to generate the comparator feedback signal; and
providing a gain to the comparator feedback signal.

13. The method as claimed in claim 12, the method further comprising coupling a digital logic component to the plurality of comparators, receiving the quantized outputs of the plurality of comparators into the digital logic component and using the digital logic component to provide a final output of the quantizer device.

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14. The method as claimed in claim 13, the method further comprising utilising the quantized outputs of the plurality of comparators to change a state of one or more state-machine based digital logic gates of the digital logic component to perform digital integration and dynamic element matching (DEM) within the digital logic component.

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15. The method as claimed in claim 14, wherein the DEM is based on CLA (Clocked Level Averaging), and the method further comprises clocking a plurality of cyclic shift registers of the digital logic component, with each clocked by a gated clock, the gated clock based on the quantized outputs of the plurality of comparators.

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16. The method as claimed in claim 15, the method further comprising processing a state difference of the plurality of cyclic shift registers to produce a final N-bit output of the quantizer device using a digital member of the digital logic component.

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17. The method as claimed in claim 14, wherein the DEM is based on DWA (Data Weighted Averaging), and the method further comprises coupling a plurality of unit cells of the digital logic component, each coupled to the quantized outputs of the plurality of comparators; clocking each unit cell based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.

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18. The method as claimed in claim 17, further comprising coupling the unit cells to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.

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19. The method as claimed in claim 18, further comprising using a DWA-DEM generation element of the digital logic component to generate a DEM pattern based on a current/present state of the each unit cell output.

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20. The method as claimed in claim 12, further comprising coupling an input of each of the plurality of comparators to a single voltage reference and performing the multi-bit quantization of the integrator output based on the single voltage reference.