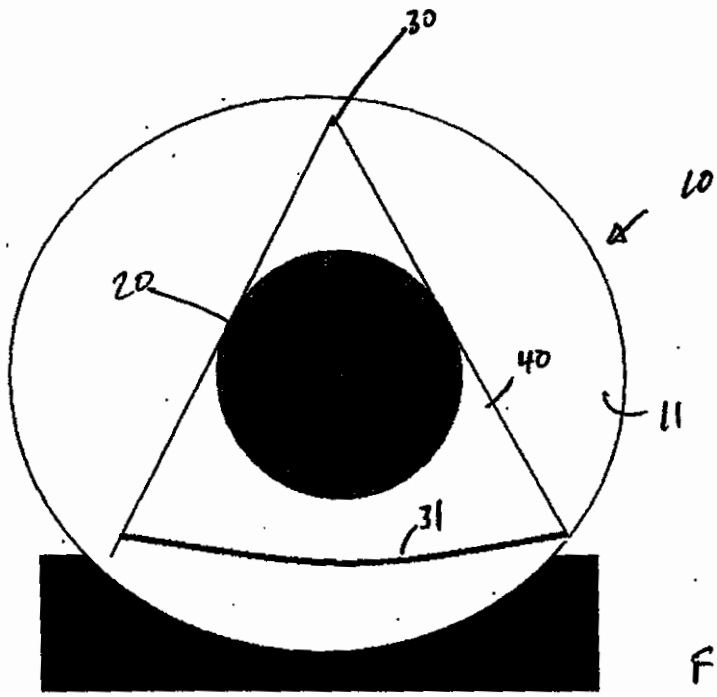


FIG. 1

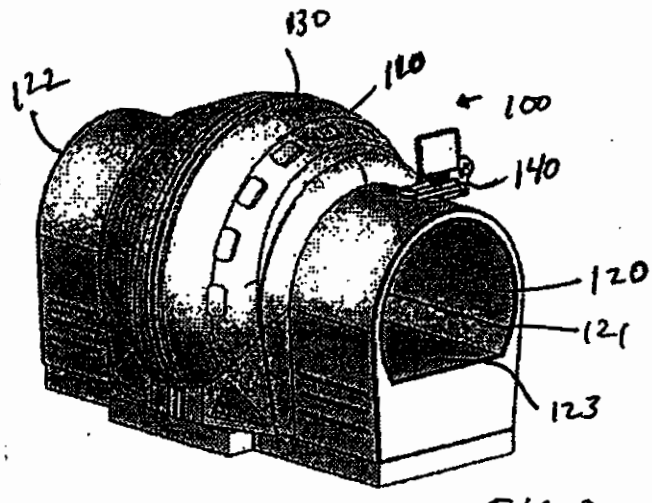


FIG. 2

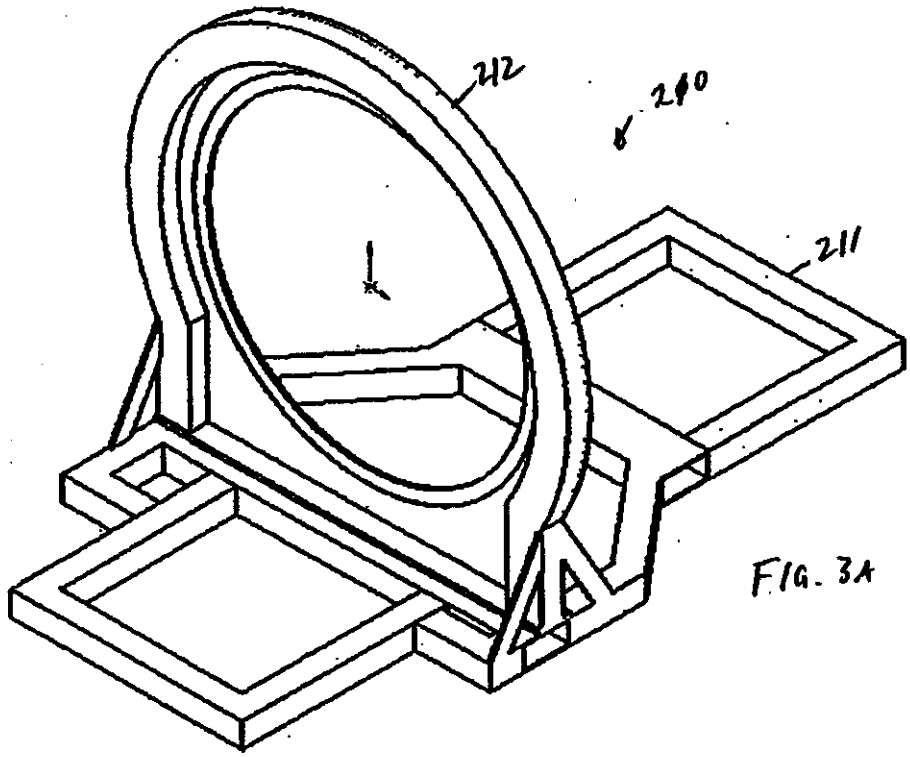


FIG. 3A

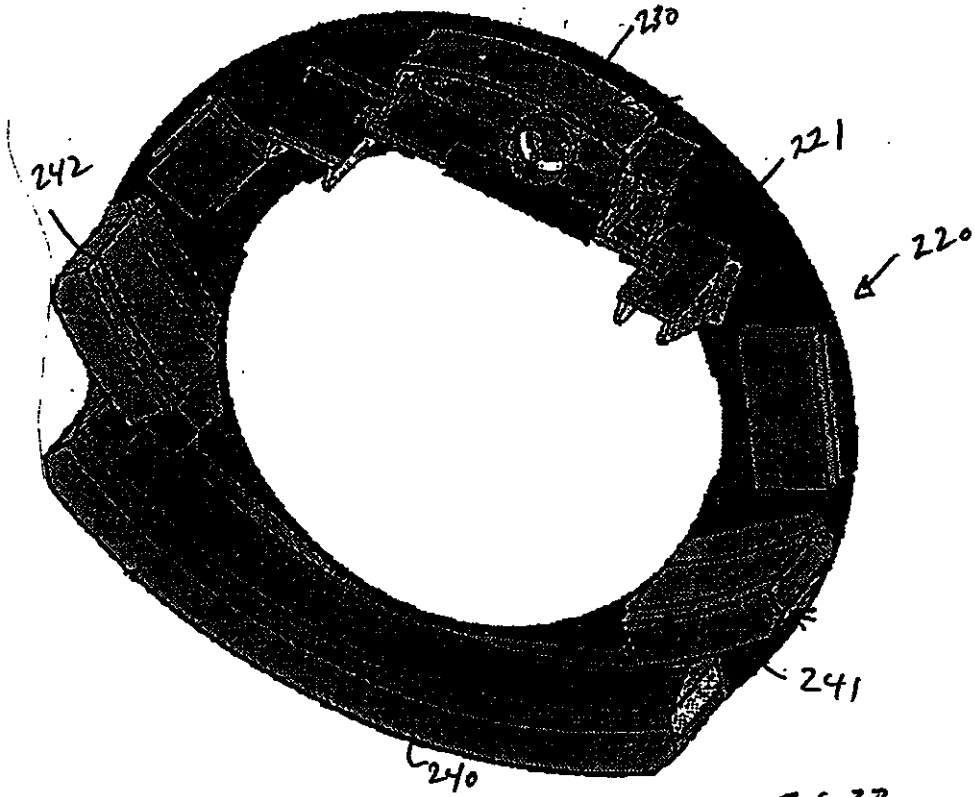


FIG 3B

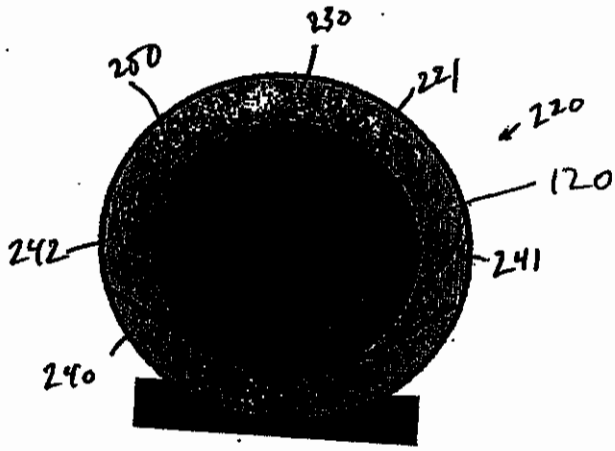


FIG. 4

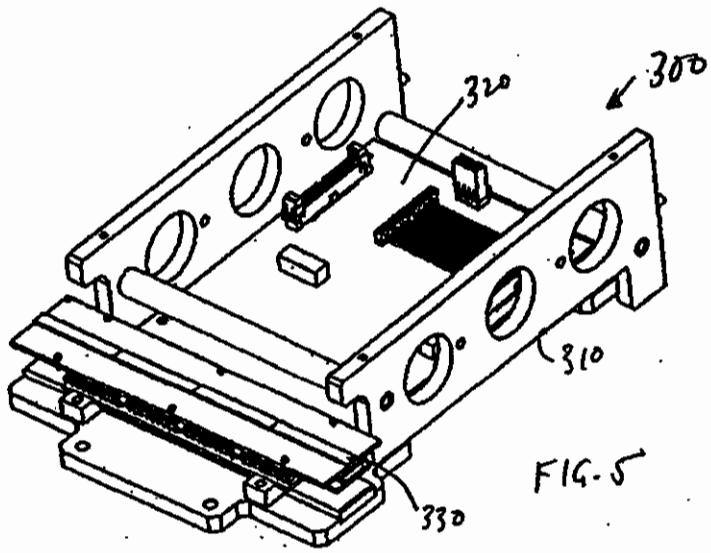


FIG. 5

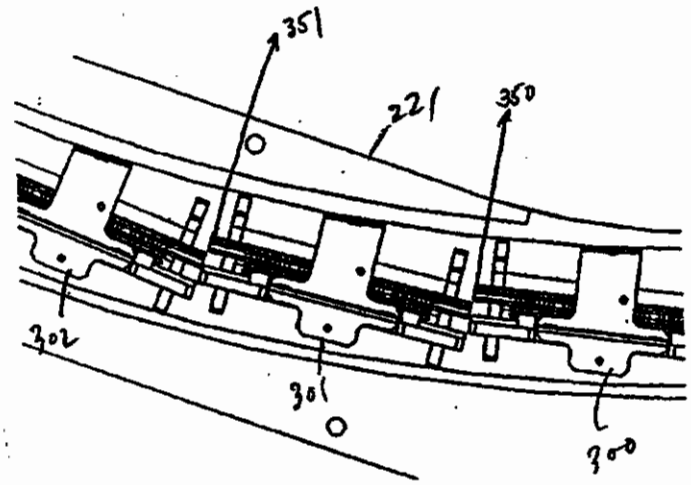


FIG. 6

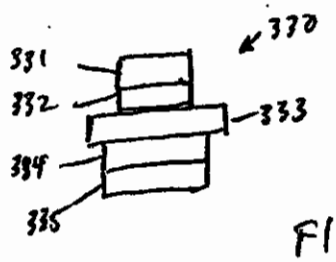


FIG 7

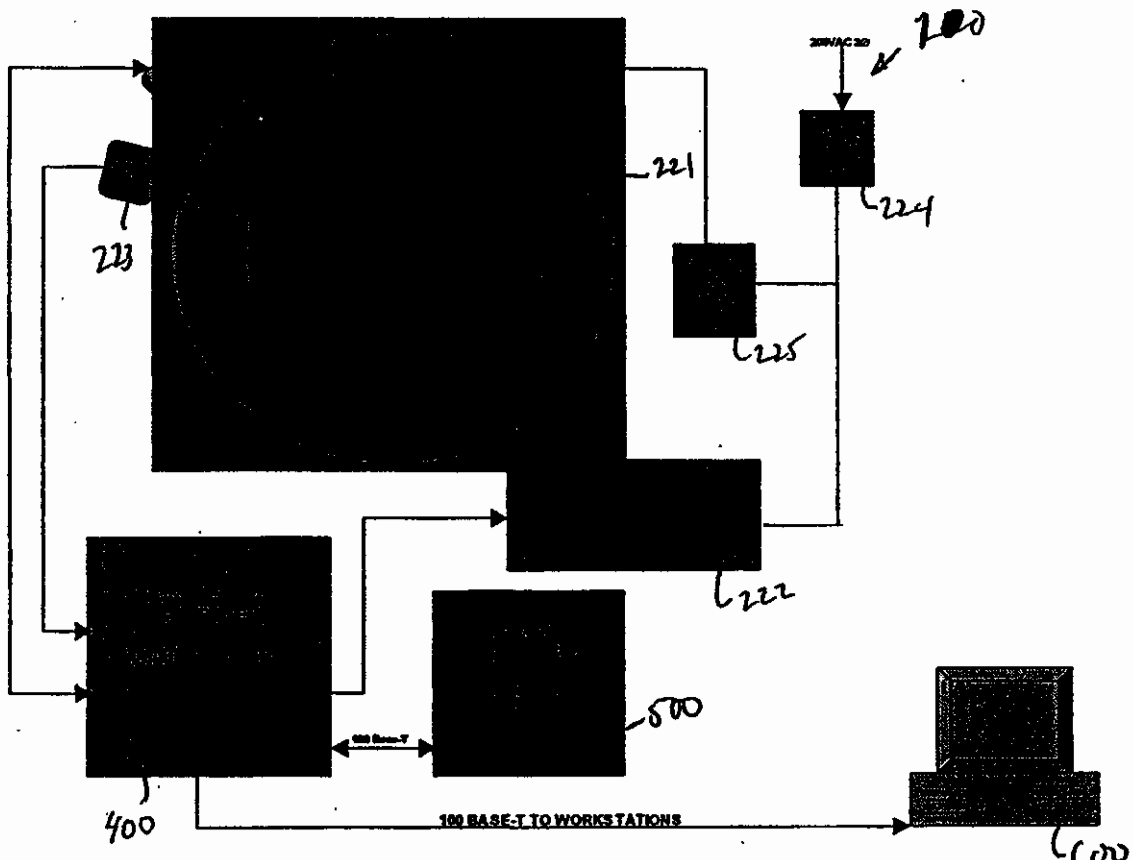


FIG. 8

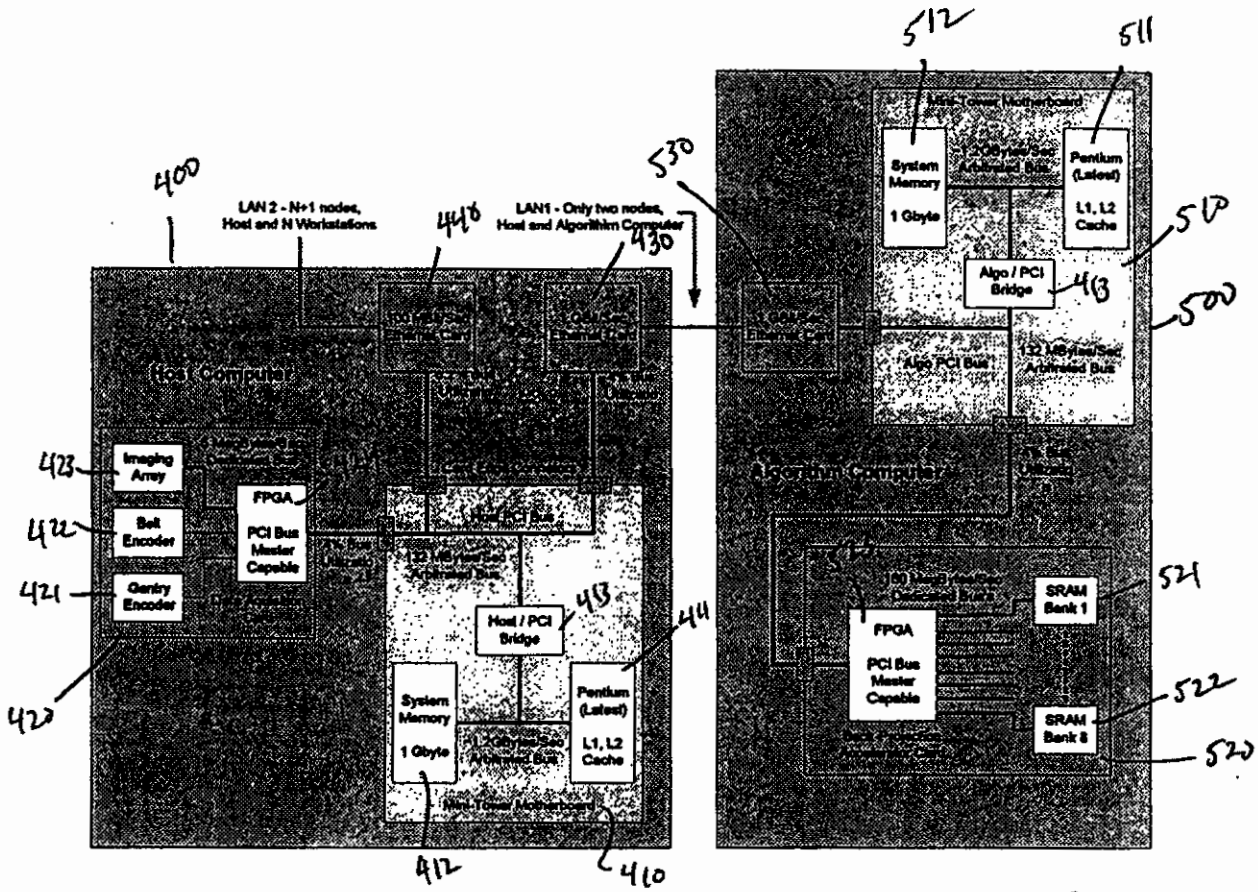

512
511
400
LAN 2 - N+1 nodes, Host and N Workstations
448
LAN1 - Only two nodes, Host and Algorithm Computer
430
530
510
500
Host Computer
Algorithm Computer
Imaging Array
423
FPGA
PCI Bus Master Capable
422
Belt Encoder
421
Gantry Encoder
420
Host / PCI Bridge
413
414
System Memory
1 Gbyte
Pentium (Latest)
L1, L2 Cache
412
410
Algo / PCI Bridge
Algo PCI Bus
513
SRAM Bank 1
521
FPGA
PCI Bus Master Capable
522
SRAM Bank 2
520

FIG. 9

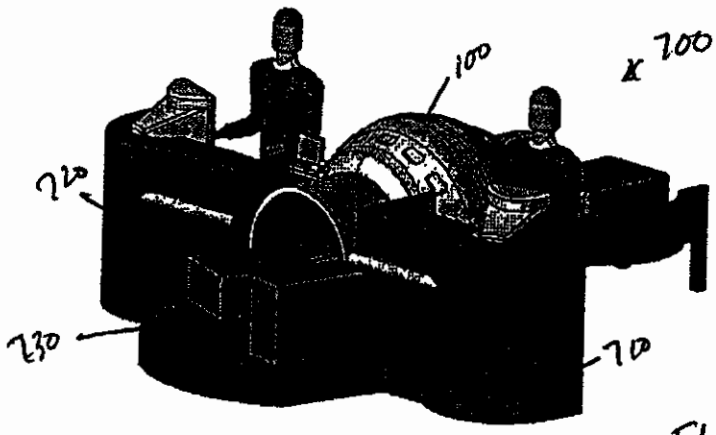

100
700
720
730
710

FIG. 10

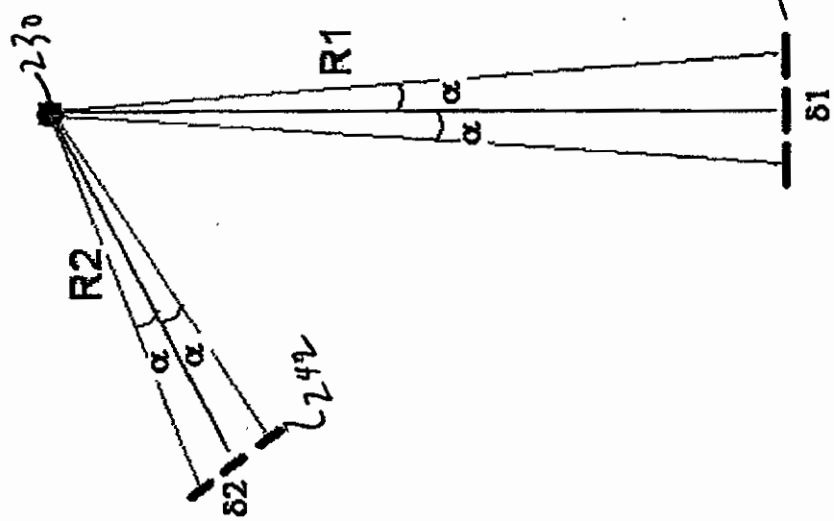

230
R1
α
α
241
81
R2
α
α
242
82

FIG 12

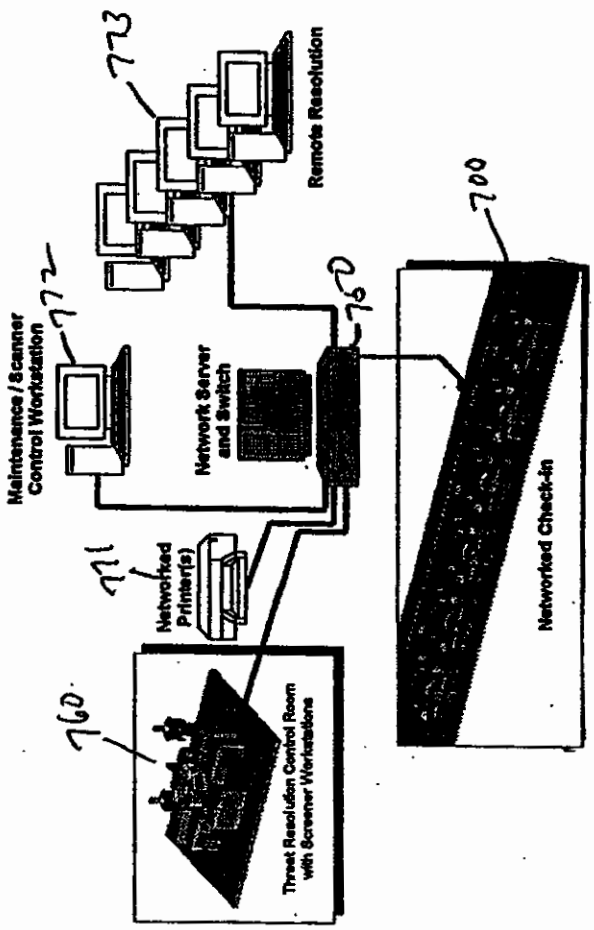

Maintenance / Scanner Control Workstation
772
Network Server and Switch
750
Remote Resolution
773
700
Networked Check-in
771
Networked Printer(s)
760
Threat Resolution Control Room with Scanner Workstations

FIG 11

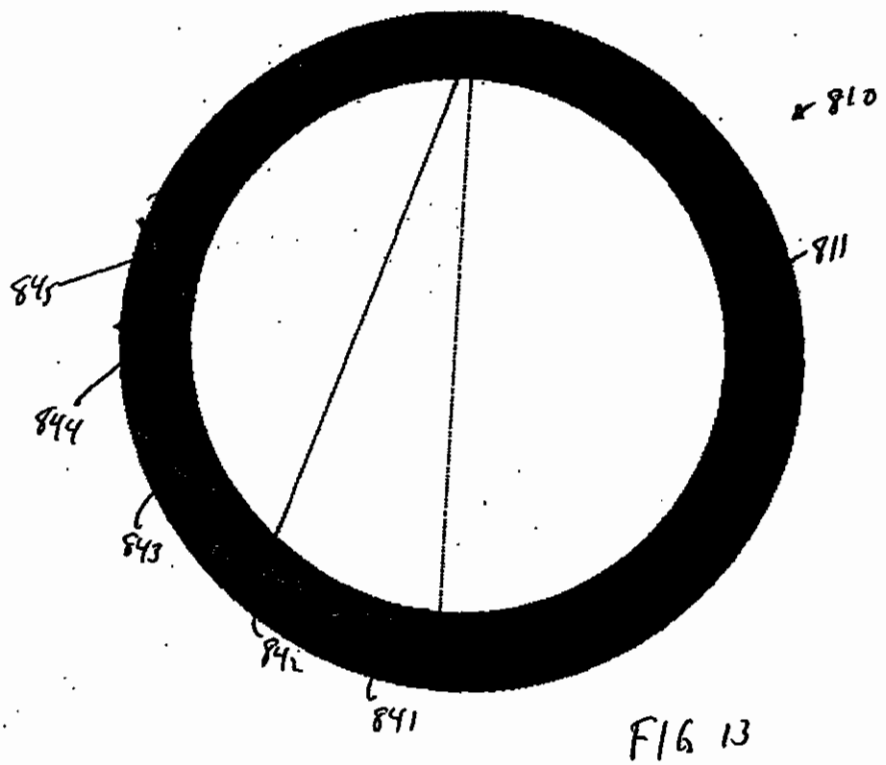

810
811
845
844
843
842
841

FIG 13

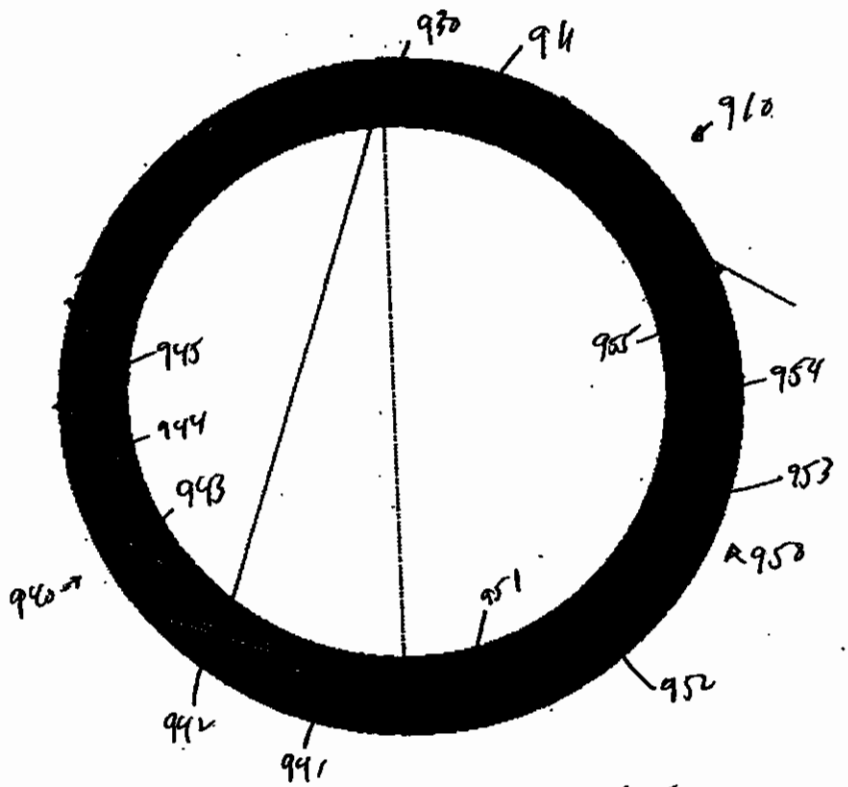

930
94
910
945
944
943
946
941
942
951
952
955
954
953
950

FIG 15

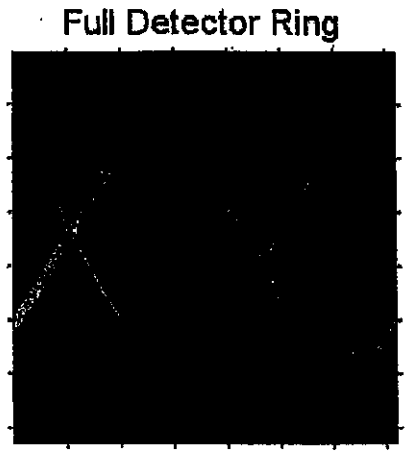


FIG. 14A

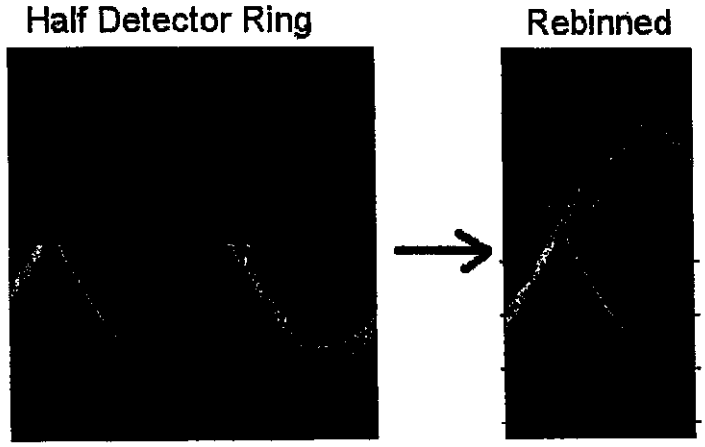


FIG. 14B

FIG. 14C