ABSTRACT

A semiconductor device, may include an active region extending in a first direction; a plurality of channel layers on the active region to be spaced apart from each other; a gate structure, surrounding the plurality of channel layers, respectively; and source/drain regions on the active region on at least one side of the gate structure, and contacting the plurality of channel layers, wherein the gate structure may include an upper portion on an uppermost channel layer among the plurality of channel layers and lower portions between each of the plurality of channel layers in a region vertically overlapping the plurality of channel layers, wherein a width of each of the plurality of channel layers in the first direction may be less than a width of lower portions of the gate structure, adjacent to the respective channel layers among the lower portions of the gate structure in the first direction.

FIG. 2A