METHOD FOR REVERSIBLY MOUNTING A DEVICE WAFER TO A CARRIER SUBSTRATE

BACKGROUND OF THE INVENTION

Related Applications

The present invention claims the benefit of U.S. Provisional Application No. 61/023,379, filed January 24, 2008, entitled METHOD FOR REVERSIBLY MOUNTING A DEVICE WAFER TO A CARRIER SUBSTRATE, incorporated by reference herein.

Field of the Invention

The present invention is broadly concerned with novel temporary wafer bonding methods that can support a device wafer on a carrier substrate during wafer thinning and other backside processing.

Description of the Prior Art

Integrated circuits, power semiconductors, light-emitting diodes, photonic circuits, microelectromechanical systems (MEMS), embedded passive arrays, packaging interposers, and a host of other silicon- and compound semiconductor-based microdevices are produced collectively in arrays on wafer substrates ranging from 1-12 inches in diameter. The devices are then separated into individual devices or dies that are packaged to allow practical interfacing with the macroscopic environment, for example, by interconnection with a printed wiring board. It has become increasingly popular to construct the device package on or around the die while it is still part of the wafer array. This practice, which is referred to as wafer-level packaging, reduces overall packaging costs and allows a higher interconnection density to be achieved between the device and its microelectronic environment than with more traditional packages that usually have outside dimensions several times larger than the actual device.

Until recently, interconnection schemes have generally been confined to two dimensions, meaning the electrical connections between the device and the corresponding board or packaging surface to which it is mounted have all been placed in a horizontal, or x-y, plane. The microelectronics industry has now recognized that significant increases in device interconnection density and corresponding reductions in signal delay (as a result of shortening the distance between electrical connection points) can be achieved by stacking and interconnecting devices

vertically, that is, in the z-direction. Two common requirements for device stacking are: (1) thinning of the device in the through-wafer direction from the backside; and (2) subsequently forming through-wafer electrical connections, commonly referred to as through-silicon-vias or "TSVs," that terminate on the backside of the device. For that matter, semiconductor device thinning has now become a standard practice even when devices are not packaged in a stacked configuration because it facilitates heat dissipation and allows a much smaller form factor to be achieved with compact electronic products such as cellular telephones.

There is growing interest in thinning semiconductor devices to less than 100 microns to reduce their profiles, especially when they or the corresponding packages in which they reside are stacked, and to simplify the formation of backside electrical connections on the devices. Silicon wafers used in high-volume integrated circuit production are typically 200 or 300 mm in diameter and have a through-wafer thickness of about 750 microns. Without thinning, it would be nearly impossible to form backside electrical contacts that connect with front-side circuitry by passing the connections through the wafer. Highly efficient thinning processes for semiconductor-grade silicon and compound semiconductors based on mechanical grinding (back-grinding) and polishing as well as chemical etching are now in commercial use. These processes allow device wafer thickness to be reduced to less than 100 microns in a few minutes while maintaining precise control over cross-wafer thickness uniformity.

Device wafers that have been thinned to less than 100 microns, and especially those thinned to less than 60 microns, are extremely fragile and must be supported over their full dimensions to prevent cracking and breakage. Various wafer wands and chucks have been developed for transferring ultra-thin device wafers, but the problem still exists of how to support the wafers during back-grinding and TSV-formation processes that include steps such as chemical-mechanical polishing (CMP), lithography, etching, deposition, annealing, and cleaning, because these steps impose high thermal and mechanical stresses on the device wafer as it is being thinned or after thinning. An increasingly popular approach to ultra-thin wafer handling involves mounting the full-thickness device wafer face down to a rigid carrier with a polymeric adhesive. It is then thinned and processed from the backside. The fully processed, ultra-thin wafer is then removed, or debonded, from the carrier by thermal, thermomechanical, or chemical processes after the backside processing has been completed.

Common carrier materials include silicon (e.g., a blank device wafer), soda lime glass, borosilicate glass, sapphire, and various metals and ceramics. The carriers may be square or rectangular but are more commonly round and are sized to match the device wafer so that the bonded assembly can be handled in conventional processing tools and cassettes. Sometimes the carriers are perforated to speed the debonding process when a liquid chemical agent is used to dissolve or decompose the polymeric adhesive as the means for release.

The polymeric adhesives used for temporary wafer bonding are typically applied by spin coating or spray coating from solution or laminating as dry-film tapes. Spin- and spray-applied adhesives are increasingly preferred because they form coatings with higher thickness uniformity than tapes can provide. Higher thickness uniformity translates into greater control over cross-wafer thickness uniformity after thinning. The polymeric adhesives exhibit high bonding strength to the device wafer and the carrier.

The polymeric adhesive may be spin-applied onto the device wafer, the carrier, or both, depending on the thickness and coating planarity (flatness) that is required. The coated wafer is baked to remove all of the coating solvent from the polymeric adhesive layer. The coated wafer and carrier are then placed in contact in a heated mechanical press for bonding. Sufficient temperature and pressure are applied to cause the adhesive to flow and fill into the device wafer structural features and achieve intimate contact with all areas of the device wafer and carrier surfaces.

Debonding of a device wafer from the carrier following backside processing is typically performed in one of four ways:

(1) Chemical - The bonded wafer stack is immersed in, or sprayed with, a solvent or chemical agent to dissolve or decompose the polymeric adhesive.

(2) Photo-Decomposition - The bonded wafer stack is irradiated with a light source through a transparent carrier to photo-decompose the adhesive boundary layer that is adjacent to the carrier. The carrier can then be separated from the stack, and the balance of the polymeric adhesive is peeled from the device wafer while it is held on a chuck.

(3) Thermo-Mechanical - The bonded wafer stack is heated above the softening temperature of the polymeric adhesive, and the device wafer is then slid or pulled away from the carrier while being supported with a full-wafer holding chuck.

(4) Thermal Decomposition - The bonded wafer stack is heated above the decomposition temperature of the polymeric adhesive, causing it to volatilize and lose adhesion to the device wafer and carrier.

Each of these debonding methods has drawbacks that seriously limit its use in a production environment. For example, chemical debonding by dissolving the polymeric adhesive is a slow process because the solvent must diffuse over large distances through the viscous polymer medium to effect release. That is, the solvent must diffuse from the edge of the bonded substrates, or from a perforation in the carrier, into the local region of the adhesive. In either case, the minimum distance required for solvent diffusion and penetration is at least 3-5 mm and can be much more, even with perforations to increase solvent contact with the adhesive layer. Treatment times of several hours, even at elevated temperatures (> 60°C), are usually required for debonding to occur, meaning wafer throughput will be low.

Photo-decomposition is likewise a slow process because the entire bonded substrate cannot be exposed at one time. Instead, the exposing light source, which is usually a laser having beam cross-section of only a few millimeters, must be focused on a small area at a time to deliver sufficient energy for decomposition of the adhesive bond line to occur. The beam is then scanned (or rastered) across the substrate in a serial fashion to debond the entire surface, which leads to long debonding times.

While thermo-mechanical (TM) debonding can be performed typically in a few minutes, it has other limitations that can reduce device yield. Backside processes for temporarily bonded device wafers often involve working temperatures higher than 200°C or even 300°C. The polymeric adhesives used for TM debonding must neither decompose nor soften excessively at or near the working temperature, otherwise, debonding would occur prematurely. As a result, the adhesives are normally designed to soften sufficiently at 20-50°C above the working temperature for debonding to occur. The high temperature required for debonding imposes significant stresses on the bonded pair as a result of thermal expansion. At the same time, the high mechanical force required to move the device wafer away from the carrier by a sliding, lifting, or twisting motion creates additional stress that can cause the device wafer to break or produces damage within the microscopic circuitry of individual devices, which leads to device failure and yield loss.

Thermal decomposition (TD) debonding is also prone to wafer breakage. Gases are produced when the polymeric adhesive is decomposed, and these gases can become trapped between the device wafer and the carrier before the bulk of the adhesive has been removed. The accumulation of trapped gases can cause the thin device wafer to blister and crack or even rupture. Another problem with TD debonding is that polymer decomposition is often accompanied by the formation of intractable, carbonized residues that cannot be removed from the device wafer by common cleaning procedures.

The limitations of these prior art debonding methods for polymeric adhesives have created the need for new modes of carrier-assisted thin wafer handling that provide high wafer throughput and reduce or eliminate the chances for device wafer breakage and internal device damage.

SUMMARY OF THE INVENTION

The present invention broadly provides a novel temporary bonding method. In one embodiment, the method comprises providing a stack comprising a first substrate having a back surface and a device surface, where the device surface has a peripheral region and a central region. The stack further comprises a second substrate having a carrier surface and an edge bond bonded to the peripheral region and to the carrier surface. The edge bond is absent from at least some of the central region, thus forming a fill zone, with a fill material being present in the fill zone. The method further comprises separating the first and second substrates.

In a further embodiment, the method comprises providing a first substrate having front and back surfaces, where the front surface has a peripheral region and a central region. An edge bond is formed on the peripheral region, and the edge bond is absent from at least some of the central region. A fill material is deposited into the central region.

In yet another embodiment, the invention provides an article comprising a first substrate having front and back surfaces. The front surface of the first substrate has a peripheral region and a central region. The article further comprises an edge bond bonded to the peripheral region, with the edge bond being absent from at least some of the central region so as to form a fill zone, which includes a fill material therein.

In a further embodiment, the invention is directed towards an article comprising a substrate having front and back surfaces. The front surface of the substrate has a peripheral

region and a central region, and a layer of material is on the front surface at the central region. The layer is absent from the peripheral region and is selected from the group consisting of a low adhesive strength layer and a surface modification of the front surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic drawing showing one embodiment for bonding substrates according to the invention;

Fig. 2 is a schematic drawing showing an alternative embodiment of the present invention, wherein two of the process steps have been reversed;

Fig. 3 is a schematic drawing depicting an alternative embodiment of the invention wherein a laminate can be utilized as the fill layer;

Fig. 4 is a schematic drawing depicting a further alternative embodiment of the invention where a second layer is utilized adjacent the fill layer;

Fig. 5 is a schematic drawing showing a possible commercial variation of the embodiment of Fig. 4; and

Fig. 6 is a schematic drawing showing a further variation of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 depicts one process by which the peripheral bonding of the present invention can be carried out. Referring to step (a) of Fig. 1, a precursor structure 10 is depicted in a schematic and cross-sectional view. Structure 10 includes a first substrate 12. In this embodiment, first substrate 12 is a device wafer. That is, substrate 12 has a front or device surface 14, a back surface 16, and an outermost edge 17. Although substrate 12 can be of any shape, it would typically be circular in shape. Regardless of the shape, the front or device surface 14 has a peripheral region 18 and a central region 20.

Preferred first substrates 12 include device wafers whose device surfaces comprise arrays of devices selected from the group consisting of integrated circuits, MEMS, microsensors, power semiconductors, light-emitting diodes, photonic circuits, interposers, embedded passive devices, and other microdevices fabricated on or from silicon and other semiconducting materials such as silicon-germanium, gallium arsenide, and gallium nitride. The surfaces of these devices

commonly comprise structures formed from one or more of the following materials: silicon, polysilicon, silicon dioxide, silicon (oxy)nitride, metals (e.g., copper, aluminum, gold, tungsten, tantalum), low k dielectrics, polymer dielectrics, and various metal nitrides and silicides. The device surface 14 can also include raised structures such as solder bumps and metal posts and pillars.

A fill material is applied to the device surface 14 of substrate 12 so as to form a fill layer 22. Fill layer 22 has first and second surfaces 24, 26 as well as outermost portion 28. It is preferred that the fill layer 22 be applied so that it has a thickness (measured at its thickest point) of from about 5 μm to about 100 μm, more preferably from about 5 μm to about 50 μm, and even more preferably from about 10 μm to about 30 μm.

Application of the fill material can be carried out via any conventional means, including spin coating, casting from solution (e.g., meniscus coating or roller coating), ink jetting, and spray coating. When applied via spin coating, the material forming fill layer 22 will typically be spin coated at speeds of from about 500 rpm to about 5,000 rpm for a time period of from about 60 seconds to about 120 seconds. The layer would then be baked near or above the boiling point of the solvent(s) present in the fill layer 22 (e.g., from about 80°C to about 250°C) for a time period of from about 1 minute to about 15 minutes to reduce the residual solvent content in fill layer 22 to less than about 1% by weight.

Fill layer 22 is typically formed of a material comprising monomers, oligomers, and/or polymers dispersed or dissolved in a solvent system. If the fill layer will be applied via spin coating, it is preferred that the solids content of this material be from about 1% by weight to about 50% by weight, more preferably from about 5% by weight to about 40% by weight, and even more preferably from about 10% by weight to about 30% by weight. Examples of suitable monomers, oligomers, and/or polymers include those selected from the group consisting of cyclic olefin polymers and copolymers and amorphous fluoropolymers with high atomic fluorine content (greater than about 30% by weight) such as fluorinated siloxane polymers, fluorinated ethylene-propylene copolymers, polymers with pendant perfluoroalkoxy groups, and copolymers of tetrafluoroethylene and 2,2-bis-trifluoromethyl-4,5-difluoro-1,3-dioxole being particular preferred. It will be appreciated that the bonding strength of these materials will depend upon their specific chemical structures and the coating and baking conditions used to apply them.

Examples of suitable solvent systems for cyclic olefin polymers and copolymers include solvents selected from the group consisting of aliphatic solvents such as hexane, decane, dodecane, and dodecene; alkyl-substituted aromatic solvents such as mesitylene; and mixtures thereof. Suitable solvent systems for amorphous fluoropolymers include fluorocarbon solvents sold, for example, by 3M Corporation under the FLUORINERT® label.

In another embodiment, the fill layer 22 could also be formed of a polymeric material that contains dispersed nanoparticles. Suitable nanoparticle materials include those selected from the group consisting of alumina, ceria, titania, silica, zirconia, graphite, and mixtures thereof.

The material of which fill layer 22 is formed should remain stable at temperatures of from about 150°C to about 350°C, and preferably from about 200°C to about 300°C. Furthermore, this material should be stable under the chemical exposure conditions encountered in the particular backside processes to which they will be subjected. Fill layer 22 should not decompose (i.e., less than about 1% weight loss) or otherwise lose its mechanical integrity, for example, by melting, under these conditions. The fill layer 22 also should not exhibit outgassing that might cause the thin device wafers to blister or deform, especially when subjected to high-vacuum processes such as during the deposition of CVD dielectric layers.

In this embodiment, the fill layer 22 preferably does not form strong adhesive bonds, thus facilitating separation later. Generally speaking, amorphous polymeric materials that: (1) have low surface free energies; (2) are tack-free and known to not bond strongly to glass, silicon, and metal surfaces (i.e., would typically have very low concentrations of hydroxyl or carboxylic acid groups, and preferably no such groups); (3) can be cast from solution or formed into a thin film for lamination; (4) will flow under typical bonding conditions to fill device wafer surface topography, forming a void-free bond line between substrates; and (5) will not crack, flow, or redistribute under mechanical stresses encountered during backside processing, even when carried out at high temperatures or under high vacuum conditions, are desirable. As used herein, low surface free energy is defined as a polymeric material that exhibits a contact angle with water of at least about 90° and a critical surface tension of less than about 40 dynes/cm, preferably less than about 30 dynes/cm, and more preferably from about 12 dynes/cm to about 25 dynes/cm, as determined by contact angle measurements.

Low bonding strength refers to polymeric materials that do not stick or can be peeled from a substrate with only light hand pressure such as might be used to debond an adhesive note

paper. Thus, anything with an adhesion strength of less than about 50 psig, preferably from less than about 35 psig, and more preferably from about 1 psig to about 30 psig would be desirable for use as fill layer 22. As used herein, adhesion strength is determined by ASTM D4541/D7234. Examples of suitable polymeric materials exhibiting the above properties include some cyclic olefin polymers and copolymers sold under the APEL® by Mitsui, TOPAS® by Ticona, and ZEONOR® by Zeon brands, and solvent-soluble fluoropolymers such as CYTOP® polymers sold by Asahi Glass and TEFLON® AF polymers sold by DuPont. The bonding strength of these materials will depend upon the coating and baking conditions used to apply them.

Next, and referring to step (b) of Fig. 1, the outermost portion 28 of fill layer 22 is removed. This can be accomplished by any means that will allow for removal of the desired quantity without damaging the first substrate 12, including dissolving the outermost portion 28 with a solvent that is known to be a good solvent for the material of which fill layer 22 is formed. Examples of such solvents include those selected from the group consisting of aliphatic solvents (e.g., hexane, decane, dodecane, and dodecene), fluorocarbon solvents, and mixtures thereof. After edge removal, fill layer 22 has an outermost edge 30, which is spaced a distance "D" from outer edge 17. "D" is typically from about 2 mm to about 15 mm, preferably from about 2 mm to about 10 mm, and more preferably from about 2 mm to about 5 mm. Contact with the edge removal solvent can be maintained for a sufficient time to dissolve the desired amount of fill layer 22 to achieve the desired distance "D," but typical contact times would be from about 5 seconds to about 60 seconds.

Referring to step (c) of Fig. 1, a second substrate 32 is depicted. In this particular embodiment, second substrate 32 is a carrier substrate. Second substrate 32 includes a carrier surface 34, a back surface 36, and an outer edge 38. As was the case with first substrate 12, second substrate 32 can be of any shape, although it would typically be circular in shape. Furthermore, second substrate 32 would preferably be sized to be approximately equal in size to first substrate 12, so that outer edge 38 of second substrate 32 will lie along substantially the same plane as outer edge 17 of first substrate 12. Regardless of the shape, carrier surface 34 has a peripheral region 40 and a central region 42.

Preferred substrates 32 comprise a material selected from the group consisting of silicon, sapphire, quartz, metals (e.g., aluminum, copper, steel), and various glasses and ceramics. Substrate 32 can also include other materials deposited on its surface 34. For example, silicon

nitride can be deposited onto a silicon wafer to change the bonding characteristics of the fill layer 22.

Second substrate 32 is contacted with fill layer 22, leaving a void 44 between the peripheral region 18 of first substrate 12 and the peripheral region 40 of second substrate 32. This contact is preferably carried out under heat and pressure, so as to cause the material of which fill layer 22 is formed to distribute substantially uniformly along the front surface 14 of first substrate 12 as well as along the carrier surface 34 of second substrate 32. The pressure and heat are adjusted based upon the chemical make-up of fill layer 22, and will be selected such that the distance "D" remains substantially the same after pressing the second substrate 32 to the first substrate 12 as before such pressing together. That is, the fill layer 22 will experience little to no flow into the void 44, and the distance "D" after pressing together will be within about 10% of the distance "D" prior to pressing together. Typical temperatures during this step will range from about 150°C to about 375°C, and preferably from about 160°C to about 350°C, with typical pressures ranging from about 1,000 N to about 5,000 N, and preferably from about 2,000 N to about 4,000 N.

Next, a bonding material is introduced into void 44 (see step (d) of Fig. 1) to form an edge bond 46, which will have a thickness corresponding to that described above with respect to fill layer 22. Because the void 44 was limited to the outer perimeter of the substrates 12 and 32, the edge bond 46 will likewise be limited. In instances where the substrates 12 or 32 are circular in shape, the edge bond 46 will be ring-shaped. Thus, there is a non-uniform material distribution across the substrates 12 and 32, unlike prior art adhesives which have a uniform layer of the same material between and across the two substrates 12, 32.

The edge bonding material can be introduced by any number of means, with one suitable mechanism being the use of a needle, syringe, or tip dispense instrument to dispense the material into the void 44 while the structure 10 is slowly rotated until the void 44 is filled with the bonding material, thus forming the edge bond 46. The edge bond 46 may also be applied via capillary filling of void 44 or via chemical vapor deposition. In a further application process, a liquid (100% solids or solution), edge bonding material can be spin-applied onto the edge of the carrier or device wafer using an edge-wrapping baffle system before contacting the substrates 12 and 32. One such system is disclosed by Dalvi-Malhotra et al., "Use of silane-based primer on silicon wafers to enhance adhesion of edge-protective coatings during wet etching: Application

of the TALON Wrap™ process," Proceedings of SPIE, vol. 6462, 2007, pp. 64620B-1 - 64620B-7, incorporated by reference herein. The edge bond 46 is then subjected to the appropriate curing or hardening process (e.g., UV curing).

The materials from which edge bond 46 are formed should be capable of forming a strong adhesive bond with the substrates 12 and 32. Anything with an adhesion strength of greater than about 50 psig, preferably from about 80 psig to about 250 psig, and more preferably from about 100 psig to about 150 psig, would be desirable for use as edge bond 46. In addition, the adhesion strength of the edge bond 46 is at least about 0.5 psig, preferably at least about 20 psig, and more preferably from about 50 psig to about 250 psig greater than the adhesion of the fill layer 22. Furthermore, the material of which edge bond 46 is formed must meet the thermal and chemical stability requirements of backside processing. The edge bond 46 should remain stable at temperatures of from about 150°C to about 350°C, and preferably from about 200°C to about 300°C. Furthermore, this material should be stable under the chemical exposure conditions encountered in the backside processes to which the bonded stack will be subjected. Edge bond 46 should not decompose (i.e., less than about 1% weight loss) or otherwise lose its mechanical integrity at the above described backside processing temperatures. These materials also should not release volatile compounds that might cause blistering of thin device wafers, especially when subjected to high vacuum processes such as CVD dielectric deposition.

Preferred edge-sealing or edge-bonding materials include commercial temporary wafer bonding compositions such as the WaferBOND® materials (sold by Brewer Science Inc., Rolla, MO) along with resins and polymers that exhibit high adhesion strength to semiconductor materials, glass, and metals. Especially preferred are: (1) high solids, UV-curable resin systems such as reactive epoxies and acrylics; (2) related thermosetting resin systems such as two-part epoxy and silicone adhesives; (3) thermoplastic acrylic, styrenic, vinyl halide (non-fluoro-containing), and vinyl ester polymers and copolymers along with polyamides, polyimides, polysulfones, polyethersulfones, and polyurethanes applied from the melt or as solution coatings that are baked after application to dry and render the peripheral regions 18 and 40 more dense; and (4) cyclic olefins, polyolefin rubbers (e.g., polyisobutylene), and hydrocarbon-based tackifier resins. As was the case with the materials used to form fill layer 22, it will be appreciated that the bonding strength of edge bond materials will also depend upon their specific chemical structures and the coating and baking conditions used to apply them.

At this stage, the first substrate 12 can be safely handled and subjected to further processes that might otherwise have damaged first substrate 12 without being bonded to second substrate 32. Thus, the structure can safely be subjected to backside processing such as back-grinding, CMP, etching, metal and dielectric deposition, patterning (e.g., photolithography, via etching), passivation, annealing, and combinations thereof, without separation of substrates 12 and 32 occurring, and without infiltration of any chemistries encountered during these subsequent processing steps into central regions 20 and 42 between substrates 12 and 32.

Advantageously, the dried or cured layers of the stacked structure in this and all embodiments will possess a number of highly desirable properties. For example, the layers will exhibit low outgassing during heating and/or vacuum deposition processes. That is, baking at about 150-300°C for up to about 60 minutes results in a film thickness change of fill layer 22 and edge bond 46 of less than about 5%, preferably less than about 2%, and even more preferably less than about 1.0%. Thus, the dried layers can also be heated to temperatures of up to about 350°C, preferably up to about 320°C, and more preferably up to about 300°C, without chemical reactions occurring in the layer. In some embodiments, the layers in the bonded stack can also be exposed to polar solvents (e.g., *N*-methyl-2-pyrrolidone) at a temperature of about 80°C for about 15 minutes without reacting or dissolving.

The bond integrity of edge bond 46 can be maintained even upon exposure to an acid or base. That is, a dried edge bond 46 having a thickness of about 15 μm can be submerged in an acidic media (e.g., concentrated sulfuric acid) at room temperature for about 10 minutes or in a basic media (e.g., 30 wt. % KOH) at about 85°C for about 45 minutes while maintaining bond integrity. Bond integrity can be evaluated by using a glass carrier substrate and visually observing the edge bond 46 through the glass carrier substrate to check for bubbles, voids, etc.

Once the desired processing is completed, first substrate 12 and second substrate 32 can be readily separated. In one separation method, the edge bond 46 is first dissolved with the aid of a solvent or other chemical agent. This can be accomplished by immersion in the solvent, or by spraying a jet of the solvent onto edge bond 46 in order to dissolve it. The use of thermoplastic materials is especially desirable if solvent dissolution is to be used to disrupt the edge bond 46. Solvents that could typically be used during this removal process include those selected from the group consisting of ethyl lactate, cyclohexanone, *N*-methyl pyrrolidone, aliphatic solvents (e.g., hexane, decane, dodecane, and dodecene), and mixtures thereof.

The substrates 12 and 32 can also be separated by first mechanically disrupting or destroying the continuity of the edge bond 46 using laser ablation, plasma etching, water jetting, or other high energy techniques that effectively etch or decompose the edge bond 46. It is also suitable to first saw or cut through the edge bond 46 or cleave the edge bond 46 by some equivalent means.

Regardless of which of the above means is utilized, a low mechanical force (e.g., finger pressure, gentle wedging) can then be applied to completely separate the substrates 12 and 32. Advantageously, and unlike prior art bonding methods, separation does not require having to overcome strong adhesive bonds between the fill layer 22 and the substrates 12 or 32. Instead, it is only necessary to release the adhesive bonds at edge bond 46 in the peripheral regions 18 and 40 for separation to occur. The surfaces of the substrates 12 and/or 32 can then be rinsed clean with appropriate solvents as necessary to remove any residual material.

While the above describes the primary method of practicing the present invention, there are several alternative embodiments of the invention. For example, the above embodiment described first substrate 12 as a device wafer and second substrate 32 as a carrier substrate. It is also acceptable that first substrate 12 is the carrier substrate and second substrate 32 is the device wafer. In that instance, front surface 14 of first substrate 12 will not be a device surface, but rather will be a carrier surface. Also, surface 34 of second substrate 32 will not be a carrier surface, but instead will be a device surface. In other words, the fill layer can be applied to the carrier rather than the device wafer with the same quality of stacked structure being formed during the subsequent bonding step.

Furthermore, the above embodiment described the sequential application of the fill layer 22 and edge bond 46 to the same substrate 12. It is also suitable to apply one of fill layer 22 and edge bond 46 to first substrate 12, and the other of fill layer 22 and edge bond 46 to second substrate 32. The first and second substrates could then be pressed together in a face-to-face relationship under heat and/or pressure as described above in order to bond the two.

Finally, while in some embodiments it is preferred that the fill layer 22 does not form strong adhesive bonds with either device surface 14 or carrier surface 34, in other embodiments it may be desirable to formulate fill layer 22 so that it does not form strong adhesive bonds with only one of device surface 14 or carrier surface 34.

Referring to Fig. 2, another alternative embodiment of the present invention is depicted, with like parts being numbered as in Fig. 1. As illustrated in this figure, the substrates 12 and 32, fill layer 22, and edge bond 46 are formed of the same materials as described above with respect to Fig. 1, except that the process order has been altered. That is, referring to step (c') of Fig. 2, the bonding or sealing material used to form edge bond 46 is applied to void 44 after application of fill layer 22 but before contacting of second substrate 32 with fill layer 22 (shown in step (d')).

As was also the case with the embodiment of Fig. 1, first substrate 12 could be the carrier substrate and second substrate 32 could be the device wafer. Again, in this instance, front surface 14 of first substrate 12 will not be a device surface, but rather will be a carrier surface. Also, surface 34 of second substrate 32 will not be a carrier surface, but instead will be a device surface. This alternative arrangement is particularly advantageous because the structure 10 shown in step (c') of Fig. 2 could be fabricated with first substrate 12 being provided as a carrier wafer. This structure could then be provided to an end user who would bond a device wafer to the structure and subject the stack to further processing. Thus, an adhesive-ready carrier would be available to the end user for added convenience, eliminating processing steps for the end user.

Fig. 3 depicts yet a further embodiment of the present invention, again with like numbering being used for like parts. In this embodiment, fill layer 22 is provided as a laminate that is adhered to first substrate 12 under heat, pressure, and/or vacuum as necessary for the particular material to ensure there are no voids between the fill layer 22 and the front surface 14 (see step (A) of Fig. 3). The laminate is pre-cut to the appropriate shape (e.g., circular) or mechanically trimmed after application so that the appropriately sized void 44 will be created, as discussed above. The bonding or sealing material used to form edge bond 46 is applied to void 44 after application of the laminate used to form fill layer 22 and before contacting of second substrate 32 with fill layer 22 (shown in step (C)).

As was also the case with the embodiments of Figs. 1 and 2, first substrate 12 could be the carrier wafer and second substrate 32 could be the device wafer. Again, in this instance, front surface 14 of first substrate 12 will not be a device surface, but rather will be a carrier surface. Also, surface 34 of second substrate 32 will not be a carrier surface, but instead will be a device surface. As was the case with the embodiment of Fig. 2, this alternative arrangement is particularly advantageous because the structure 10 shown in step (B) of Fig. 3 could be fabricated

with first substrate 12 being provided as a carrier substrate. This structure could then be provided to an end user who would bond a device wafer to the structure and subject the stack to further processing.

A further alternative embodiment is depicted in Fig. 4, with like numbering being used to depict like parts. A structure 48 is depicted. Structure 48 is similar to structure 10 shown in step (d) of Fig. 1 (and is similarly formed) except that structure 48 further comprises a second layer 50. Layer 50 can be a low adhesive strength layer such as an anti-stick coating (e.g., mold release agent) applied to facilitate separation after backside or other processing. The use of the anti-stick coating lessens the requirement for the fill layer 22 to form a non-stick or low adhesion strength interface with the first or second substrates 12 or 32.

Instead of being in the form of a low adhesive strength layer, layer 50 (not to scale) could also represent an area on the front surface 14 of the first substrate 12 that has been chemically modified to obtain a permanent non-stick surface layer or a surface layer to which a fill material cannot strongly bond. Such modifications may include, for example: (a) chemical treatment of a silicon surface with a hydrophobic organosilane such as a (fluoro)alkyl silane (e.g., perfluoroalkyltrichlorosilane) or a (fluoro)alkyl phosphonate to reduce its surface free energy; or (b) chemical vapor deposition of a low surface free energy coating (e.g., fluorinated parylenes or parylene AF4) onto the carrier to create a permanent non-stick surface. The advantage of this approach is that the filling layer(s) can be selected for any combination of properties (e.g., thickness, solubility, thermal stability) other than providing a non-stick or low adhesive strength interface with the substrate. When a surface modification is carried out, the thickness of layer 50 will generally be on the order of from about 1 nm to about 5 nm.

Finally, instead of being a low adhesive strength layer or a surface modification, layer 50 could also represent a second polymeric layer. Layer 50 could be a polymer coating selected from the group consisting of cyclic olefin polymers and copolymers having low adhesion strength to the substrate 12 or 32 onto which it is applied or to the fill layer 22 in which it is contact, or layer 50 could also be a permanent anti-stick layer such as a fluoropolymer coating (e.g., those sold under the name Teflon® by DuPont). When layer 50 is a low adhesive strength polymer layer, it is preferably applied (e.g., via spin coating) at a thickness of at least about 0.5 μm, and more preferably from about 1 μm to about 10 μm.

The use of a polymer coating as layer 50 allows for customization benefits to the end user. For example, layer 50 could form a non-stick or low adhesive strength interface with first substrate 12 to facilitate easy separation of that substrate once the edge bond 46 has been broken or removed while fill layer 22 is firmly bonded to second substrate 32. The advantage of this configuration is that the fill layer 22 can be very thick (up to several hundred microns) and can be chosen for rapid dissolution in a cleaning solvent but does not have to form a non-stick or low adhesive strength interface with the first substrate 12, or the roles of the layers could be reversed. The application of the layer 50 and fill layer 22 can occur sequentially on first substrate 12 or, alternatively, they can be coated separately, with one of the layers 50 or 22 first placed on each substrate, and then placed into contact with one another.

Regardless of the layer 50 utilized, it should not intermix with, dissolve in, or react with fill layer 22. Furthermore, it should be selected to coat uniformly and without voids or other defects.

As was also the case with the embodiments previously discussed, the substrates 12 and 32 could be reversed so that first substrate 12 would be the carrier substrate and second substrate 32 would be the device wafer. Again, in this instance, front surface 14 of first substrate 12 will not be a device surface, but rather will be a carrier surface. Also, surface 34 of second substrate 32 will not be a carrier surface, but instead will be a device surface. This alternative arrangement would again be advantageous because the structure 48' shown in Fig. 5 could be fabricated with first substrate 12 being provided as a carrier wafer. This structure could then be provided to an end user who would bond a device wafer to the structure and subject the stack to further processing. Thus, as with previous embodiments, an adhesive-ready carrier would be available to the end user for added convenience, eliminating processing steps for the end user.

A further embodiment of the invention is depicted in Fig. 6. In this embodiment, structure 52 is similar to structure 48' shown in Fig. 5, except that structure 52 only comprises substrate 12 and layer 50. In this embodiment, substrate 12 would preferably be a carrier substrate such as those described above. This structure could be provided to an end user who would then use it as a carrier substrate to support a device wafer during processing.

Finally, the materials used to form fill layer 22, edge bond 46, and layer 50 have been described above. It will be appreciated that the mechanism for hardening or curing these materials can be readily selected and adjusted by those of ordinary skill in the art. For example,

in some embodiments, it may be desirable to use a non-curing composition for easier dissolving in later removal and cleaning processes. For each of these materials, thermoplastic or rubber-like compositions (typically having a weight average molecular weight of at least about 5,000 Daltons), resin- or rosin-type compositions (typically having a weight average molecular weight of less than about 5,000 Daltons), and mixtures of the foregoing would be suitable.

In other embodiments, a thermosetting material may be better suited, and thus a composition that cures or crosslinks upon heating would be selected. This would require the use of a crosslinking agent and potentially a catalyst in the system as well as a step to induce crosslinking.

In yet another embodiment, a photocurable system may be preferable. This would require the use of a free-radical photoinitiator or photogenerated catalyst in the system as well as a step (e.g., exposure to UV light) to induce curing. This system provides an advantage in some instances in that it can be applied as a 100% solids composition, if necessary.

It will be appreciated that the above can be used to fabricate a number of integrated microdevices, including those selected from the group consisting of silicon-based semiconductor devices, compound semiconductor-based devices, arrays of embedded passive devices (e.g., resistors, capacitors, inductors), MEMS devices, microsensors, photonic circuit devices, light emitting diodes, heat management devices, and planar packaging substrates (e.g., interposers) to which one or more of the foregoing devices has been or will be attached.

EXAMPLES

The following examples set forth preferred methods in accordance with the invention. It is to be understood, however, that these examples are provided by way of illustration and nothing therein should be taken as a limitation upon the overall scope of the invention.

Example 1

Edge Surface Adhesively Bonded and

Center Surface Chemically Modified

An epoxy-based photoresist (SU-8 2002, Microchem, Newton, MA) was dispensed onto the surface of a 100-mm silicon wafer (wafer 1) at the outer edge to coat a section of the wafer surface that was about 3-5 mm wide. A fluorinated silane ((heptadecafluoro-1,1,2,2-tetrahydradecyl) trichlorosilane) was diluted to a 1% solution using FC-40 solvent (perfluoro compound with primarily C_{12}, sold under the name Fluorinert, obtained from 3M). The solution was spin coated onto the surface of wafer 1. The wafer 1 was baked on a hotplate at 100°C for 1 minute. It was rinsed with FC-40 solvent in a spin coater and baked at 100°C for an additional 1 minute. The epoxy-based photoresist was removed using acetone in a spin coater, leaving the edge untreated from the fluorinated silane solution.

The surface of another 100-mm silicon wafer (wafer 2) was coated with a bonding composition (WaferBOND® HT10.10, available from Brewer Science Inc., Rolla, MO) via spin coating. This wafer was baked at 110°C for 2 minutes followed by 160°C for 2 minutes. The coated wafers were bonded in a face-to-face relationship under vacuum at 220°C for 3 minutes in a heated vacuum and pressure chamber. They were debonded by inserting a razor blade at the edge between the two wafers. After the separation, only a 3-5 mm wide ring of the bonding composition coating transferred to the edge of wafer 1, while the rest of coating remained on wafer 2. Either wafer in this example could be considered the device wafer or the carrier wafer.

Example 2

Edge Surface Adhesively Bonded,

Center Surface Chemically Modified, and

Debonding Using Solvent Jet at Edge with Wedge

An epoxy-based photoresist was dispensed onto the surface of a 200-mm silicon wafer (wafer 1) at the outer edge to coat a section of the wafer surface that was about 3-5 mm wide. A fluorinated silane ((heptadecafluoro-1,1,2,2-tetrahydradecyl) trichlorosilane) was diluted to a 1% solution using FC-40 solvent. The solution was spin coated onto the surface of wafer 1. The wafer 1 was baked on a hotplate at 100°C for 1 minute. It was rinsed with FC-40 solvent in a spin coater and baked at 100°C for an additional 1 minute. The epoxy-based photoresist was

removed using acetone in a spin coater, leaving the edge untreated from the fluorinated silane solution.

The surface of another 200-mm silicon wafer (wafer 2) was coated with WaferBOND® HT10.10 bonding composition via spin coating. This wafer was baked at 110°C for 2 minutes and 160°C for 2 minutes. The coated wafers were bonded in a face-to-face relationship with one another under vacuum at 220°C for 2 minutes in a heated vacuum and pressure chamber. The wafers were debonded by dispensing dodecene, the solvent in the WaferBOND® HT10.10, directly at the edge of the bonded wafers to dissolve the bonding composition while spinning the wafers to expose the edge of the bonded wafers to the solvent. After the solvent dissolved the material to approximately 0.5-1mm from the edge, a sharpened round disk was inserted at the edge between the wafers while they were still spinning. This caused the bonding composition to fail at the edge, and the wafers were separated. After the separation, only a 3-5mm wide ring of the HT10.10 coating transferred to the edge of wafer 1, while the rest of coating remained on wafer 2. Either wafer in this example could be considered the device wafer or the carrier wafer.

Example 3

Edge Surface Adhesively Bonded and

Center Surface Coated with Release Material

A negative epoxy-based photoresist (sold under the name SU-8 2010, obtained from MicroChem) was spin coated onto the surface of a 100-mm glass wafer. The wafer was baked at 110°C for 2 minutes. A Teflon® AF solution (Teflon® AF2400 in FC-40, obtained from DuPont) was spin coated over the SU-8 2010. Then, FC-40 solvent was dispensed onto the surface of the wafer at the outer edge to remove about a 3-5 mm wide section of the Teflon® AF coating from the wafer surface. The wafer was baked at 110°C for 2 minutes. The wafer was bonded in a face-to-face relationship with a blank, 100-mm silicon wafer under vacuum at 120°C for 3 minutes in a heated vacuum & pressure chamber. The bonded wafers were exposed to broadband UV light from the outer side of the glass wafer. The exposed wafers were baked at 120°C for 2 minutes to crosslink the SU-8 2010 coating. They were debonded by inserting a razor blade at the edge between the two wafers. After separation, the silicon wafer had only a

ring of material at the outer 3-5 mm, while there was no material transfer in the center. Either wafer in this example could be considered the device wafer or the carrier wafer.

Example 4

Edge Surface Adhesively Bonded and

Center Surface of Coated with Adhesion Promoter

A silicone acrylate copolymer was prepared by first mixing the following to prepare a monomer solution: 624 g of methacryloxypropyl tris(tris-methylsiloxy)silane; 336 g of glycidyl methacrylate; and 9.6 g of dicumyl peroxide. Next, 1430.4 g of 1-butanol was added to a reactor and heated to 116°C in one hour. The monomer solution was drop-added over 4 hours, and polymerization was carried out for 20 hours at 116°C to yield a silicone acrylate copolymer solution having a percent solids of 40.4%.

The copolymer solution was spin coated onto the surface of a 100-mm silicon wafer (wafer 1). Then 1-butanol was dispensed onto the surface of the wafer at the outer edge to remove about a 3-5 mm wide section of the silicone acrylate copolymer coating from the wafer surface. The wafer was baked on a hotplate at 110°C for 2 minutes. The surface of another 100-mm silicon wafer (wafer 2) was coated with Brewer Science's WaferBOND® HT10.10 wafer bonding composition via spin coating. This wafer was then baked at 110°C for 2 minutes and 160°C for 2 minutes. The coated wafers were bonded in a face-to-face relationship with one another under vacuum at 220°C for 3 minutes in a heated vacuum and pressure chamber. They were debonded by inserting a razor blade at the edge between the two wafers. After the separation, only a 3-5 mm wide ring of the HT10.10 coating remained on the edge of wafer 2, while the rest of coating was cleanly transferred to wafer 1. Either wafer in this example could be considered the device wafer or the carrier wafer.

Example 5

Edge Surface Adhesively Bonded and

Center Surface Filled with Material

Having Low Adhesion to Either Substrate

The Teflon® AF solution used in Example 3 was spin coated onto the surface of a 100-mm silicon wafer (wafer 1). Next, FC-40 solvent was dispensed onto the surface of the

wafer at the outer edge to remove about a 3-5 mm wide section of the Teflon® AF coating from the wafer surface. The wafer was baked at 110°C for 2 minutes. The edge of the wafer was coated with WaferBOND® HT10.10 bonding composition via spin coating, with the material only being dispensed at the edge. The wafer was bonded in a face-to-face relationship with a blank, 100-mm silicon wafer (wafer 2) under vacuum at 220°C for 2 minutes in a heated vacuum and pressure chamber. The wafers were debonded by inserting a razor blade at the edge between the two wafers. After separation, wafer 2 had only a ring of the bonding material on the outer 3-5 mm, while there was no material transfer in the center. Either wafer in this example could be considered the device wafer or the carrier wafer.

We Claim:

1. A temporary bonding method comprising:

providing a stack comprising:

a first substrate having a back surface and a device surface, said device surface having a peripheral region and a central region;

a second substrate having a carrier surface; and

an edge bond bonded to said peripheral region and to said carrier surface, said edge bond being absent from at least some of said central region so as to form a fill zone; and

a fill material in said fill zone;

separating said first and second substrates.

2. The method of claim 1, wherein said device surface comprises an array of devices selected from the group consisting of integrated circuits; MEMS; microsensors; power semiconductors; light-emitting diodes; photonic circuits; interposers; embedded passive devices; and microdevices fabricated on or from silicon, silicon-germanium, gallium arsenide, and gallium nitride.

3. The method of claim 1, wherein said second substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

4. The method of claim 1, said device surface comprising at least one structure selected from the group consisting of: solder bumps; metal posts; metal pillars; and structures formed from a material selected from the group consisting of silicon, polysilicon, silicon dioxide, silicon (oxy)nitride, metal, low k dielectrics, polymer dielectrics, metal nitrides, and metal silicides.

5. The method of claim 1, wherein said fill material presents a first surface in contact with said carrier surface, and a second surface in contact with said device surface, said fill material being a uniform material from said first surface to said second surface.

6. The method of claim 1, wherein said fill material presents a first surface and a second surface, said article further comprising a second layer in contact with one of said first and second surfaces, the other of said first and second surfaces being in contact with one of said carrier surface and said device surface.

7. The method of claim 6, wherein said second layer is selected from the group consisting of a low adhesive strength layer, a polymeric layer, and a surface modification of said carrier surface or of said device surface.

8. The method of claim 7, wherein said second layer is in contact with said carrier surface.

9. The method of claim 1, wherein said edge bond has a width of from about 2 mm to about 15 mm.

10. The method of claim 1, wherein said edge bond is formed from a material comprising monomers, oligomers, or polymers selected from the group consisting of epoxies, acrylics, silicones, styrenics, vinyl halides, vinyl esters, polyamides, polyimides, polysulfones, polyethersulfones, cyclic olefins, polyolefin rubbers, and polyurethanes.

11. The method of claim 1, wherein said fill material comprises monomers, oligomers, and/or polymers selected from the group consisting of cyclic olefins and amorphous fluoropolymers.

12. The method of claim 1, further comprising subjecting said stack to processing selected from the group consisting of back-grinding, chemical-mechanical polishing, etching, metal and dielectric deposition, patterning, passivation, annealing, and combinations thereof, prior to separating said first and second substrates.

13. The method of claim 1, further comprising exposing said edge bond to a solvent to dissolve said edge bond prior to said separating.

14. The method of claim 1, further comprising mechanically disrupting said edge bond prior to said separating.

15. The method of claim 1, wherein said separating comprises applying a low force to at least one of said first and second substrates so as to pull them apart.

16. An article comprising:

a first substrate having front and back surfaces, said front surface having a peripheral region and a central region;

an edge bond bonded to said peripheral region, said edge bond being absent from at least some of said central region so as to form a fill zone; and

a fill material in said fill zone.

17. The article of claim 16, wherein said first substrate comprises a device wafer having a device surface comprising an array of devices selected from the group consisting of integrated circuits; MEMS; microsensors; power semiconductors; light-emitting diodes; photonic circuits; interposers; embedded passive devices; and microdevices fabricated on or from silicon, silicon-germanium, gallium arsenide, and gallium nitride.

18. The article of claim 16, wherein said first substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

19. The article of claim 16, further comprising a second substrate having a carrier surface, said edge bond being further bonded to said carrier surface.

20. The article of claim 19, wherein said second substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

21. The article of claim 17, said device surface comprising at least one structure selected from the group consisting of: solder bumps; metal posts; metal pillars; and structures formed from a material selected from the group consisting of silicon, polysilicon, silicon dioxide, silicon (oxy)nitride, metal, low k dielectrics, polymer dielectrics, metal nitrides, and metal silicides.

22. The article of claim 16, wherein said fill material presents a first surface and a second surface, said article further comprising a second layer in contact with one of said first and second surfaces.

23. The article of claim 22, wherein said second layer is selected from the group consisting of a low adhesive strength layer, a polymeric layer, and a surface modification of said carrier surface or of said device surface.

24. The article of claim 23, wherein said second layer is in contact with said carrier surface.

25. The article of claim 16, wherein said edge bond has a width of from about 2 mm to about 15 mm.

26. The article of claim 16, wherein said edge bond is formed from a material comprising monomers, oligomers, or polymers selected from the group consisting of epoxies, acrylics, silicones, styrenics, vinyl halides, vinyl esters, polyamides, polyimides, polysulfones, polyethersulfones, cyclic olefins, polyolefin rubbers, and polyurethanes.

27. The article of claim 16, wherein said fill material comprises monomers, oligomers, and/or polymers selected from the group consisting of cyclic olefins and amorphous fluoropolymers.

28. A method of forming a temporary wafer bonding structure, said method comprising:

providing a first substrate having front and back surfaces, said front surface having a peripheral region and a central region;

forming an edge bond on said peripheral region, said edge bond being absent from said central region; and

depositing a fill material in said central region.

29. The method of claim 28, wherein said depositing a fill material is carried out prior to said forming an edge bond.

30. The method of claim 28, wherein said first substrate comprises a device wafer having a device surface comprising an array of devices selected from the group consisting of integrated circuits; MEMS; microsensors; power semiconductors; light-emitting diodes; photonic circuits; interposers; embedded passive devices; and microdevices fabricated on or from silicon, silicon-germanium, gallium arsenide, and gallium nitride.

31. The method of claim 28, wherein said first substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

32. The method of claim 28, further comprising bonding a second substrate having a carrier surface to said edge bond.

33. The method of claim 32, wherein said second substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

34. The method of claim 28, said device surface comprising at least one structure selected from the group consisting of: solder bumps; metal posts; metal pillars; and structures formed from a material selected from the group consisting of silicon, polysilicon, silicon dioxide, silicon (oxy)nitride, metal, low k dielectrics, polymer dielectrics, metal nitrides, and metal silicides.

35. The method of claim 28, wherein said fill material presents a first surface and a second surface, said article further comprising a second layer in contact with one of said first and second surfaces.

36. The method of claim 35, wherein said second layer is selected from the group consisting of a low adhesive strength layer, a polymeric layer, and a surface modification of said carrier surface or of said device surface.

37. The method of claim 36, wherein said second layer is in contact with said carrier surface.

38. The method of claim 28, wherein said edge bond has a width of from about 2 mm to about 15 mm.

39. The method of claim 28, wherein said edge bond is formed from a material comprising monomers, oligomers, or polymers selected from the group consisting of epoxies, acrylics, silicones, styrenics, vinyl halides, vinyl esters, polyamides, polyimides, polysulfones, polyethersulfones, cyclic olefins, polyolefin rubbers, and polyurethanes.

40. The method of claim 28, wherein said fill material comprises monomers, oligomers, and/or polymers selected from the group consisting of cyclic olefins and amorphous fluoropolymers.

41. An article comprising:

a substrate having front and back surfaces, said front surface having a peripheral region and a central region; and

a layer of material on said front surface at said central region, said layer being absent from said peripheral region and being selected from the group consisting of a low adhesive strength layer and a surface modification of said front surface.

42. The article of claim 41, wherein said substrate comprises a material selected from the group consisting of silicon, sapphire, quartz, metal, glass, and ceramics.

43. The article of claim 42, wherein said substrate comprises silicon.

44. The article of claim 41, wherein said peripheral region has a width of from about 2 mm to about 15 mm.

45. The article of claim 41, said layer having a thickness of from about 1 nm to about 5 nm.