

## **Abstract**

### **CAPACITOR TOP PLATE OVER SOURCE/DRAIN TO FORM A 1T MEMORY DEVICE**

A method and structure for a memory device, such as a 1T-SRAM, having a capacitor top plate directly over a doped bottom plate region. An example device comprises the following. An isolation film formed as to surround an active area on a substrate. A gate dielectric and gate electrode formed over a portion of the active area. A source element and a drain element in the substrate adjacent to the gate electrode. The drain element is comprised of a drain region and a bottom plate region. The drain region is between the bottom plate region and the gate structure. A capacitor dielectric and a capacitor top plate are over at least portions of the bottom plate region.

**Fig. 7A**