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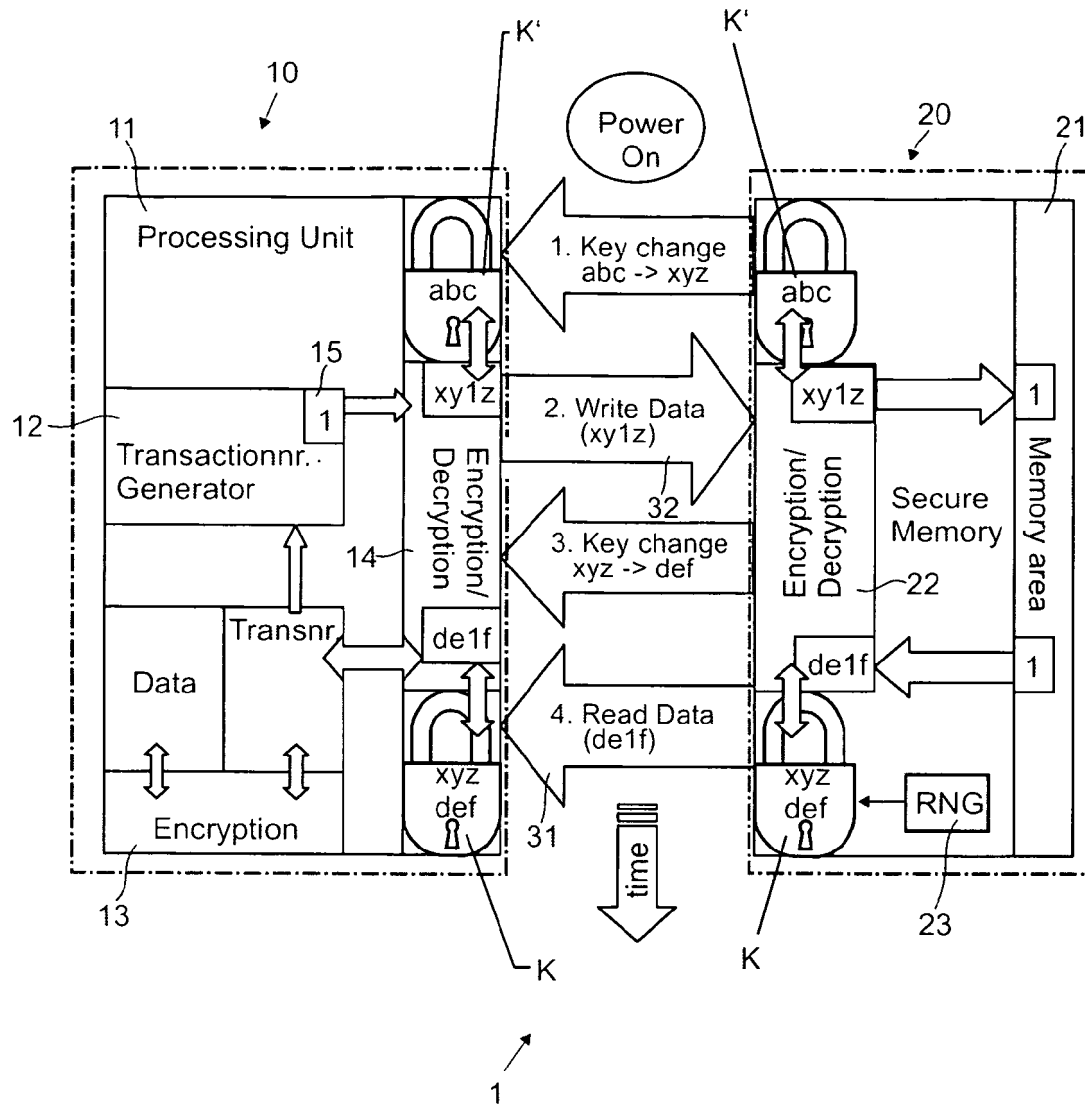


FIG. 1

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step	Transaction number (Data)	Key processor	Communication line	Key Memory	Memory
Power up	-	abc (default)		abc(default)	-
Key change	-	xyz	axbycz ->	abc	-
Key changed	-	xyz	-	xyz	-
Data write	1	xyz	xy1z ->	xyz	1
Key change	-	def	xdyez f ->	xyz	1
Key changed	-	def	-	def	1
Data read	1	def	<- de1f	def	1
Data write	2	def	de2f ->	def	2
...	2 -> 10	...	...	...	10
Power Down					
Power up		abc (default)	-	abc(default)	10
Hacking		(ghi)	axbycz ->	abc	10
Hacking		(ghi)	-	xyz	10
Hacking		(ghi)	xy1z ->	xyz	1
Hacking		(mno)	xdyez f ->	xyz	1
Hacking		(mno)	-	def	1
Hacking	Invalid Data	mno	<- de1f	def	1
Hacking		(mno)	de2f ->	def	2
Power Down					2
Power up		abc(default)		abc(default)	2
	...	...	...	...	...

FIG. 2

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step	Transaction number (Data)	Key processor	Communication line	Key Memory	Memory
Power up	-	abc (default)	-	abc (default)	10
Key change	-	abc	<- axbycz	xyz	10
Key changed	-	xyz	-	xyz	10
Data read	10	xyz	<- xy10z	xyz	10
Data write	11	xyz	xy11z ->	xyz	11
Key change	-	xyz	<- xdyez f	def	11
Key changed	-	def	-	def	11
Data read	11	def	<- de11f	def	11
Data write	12	def	de12f ->	def	12
...	12 -> 24	...	...	...	24
Power Down					
Power up	-	abc (default)	-	abc (default)	24
Hacking	-	abc	<- axbycz	(ghi)	24
Hacking		xyz	-	(ghi)	24
Hacking	10	xyz	<- xy10z	(ghi)	24
Hacking	11	xyz	xy11z ->	ghi	Invalid Data

FIG. 3

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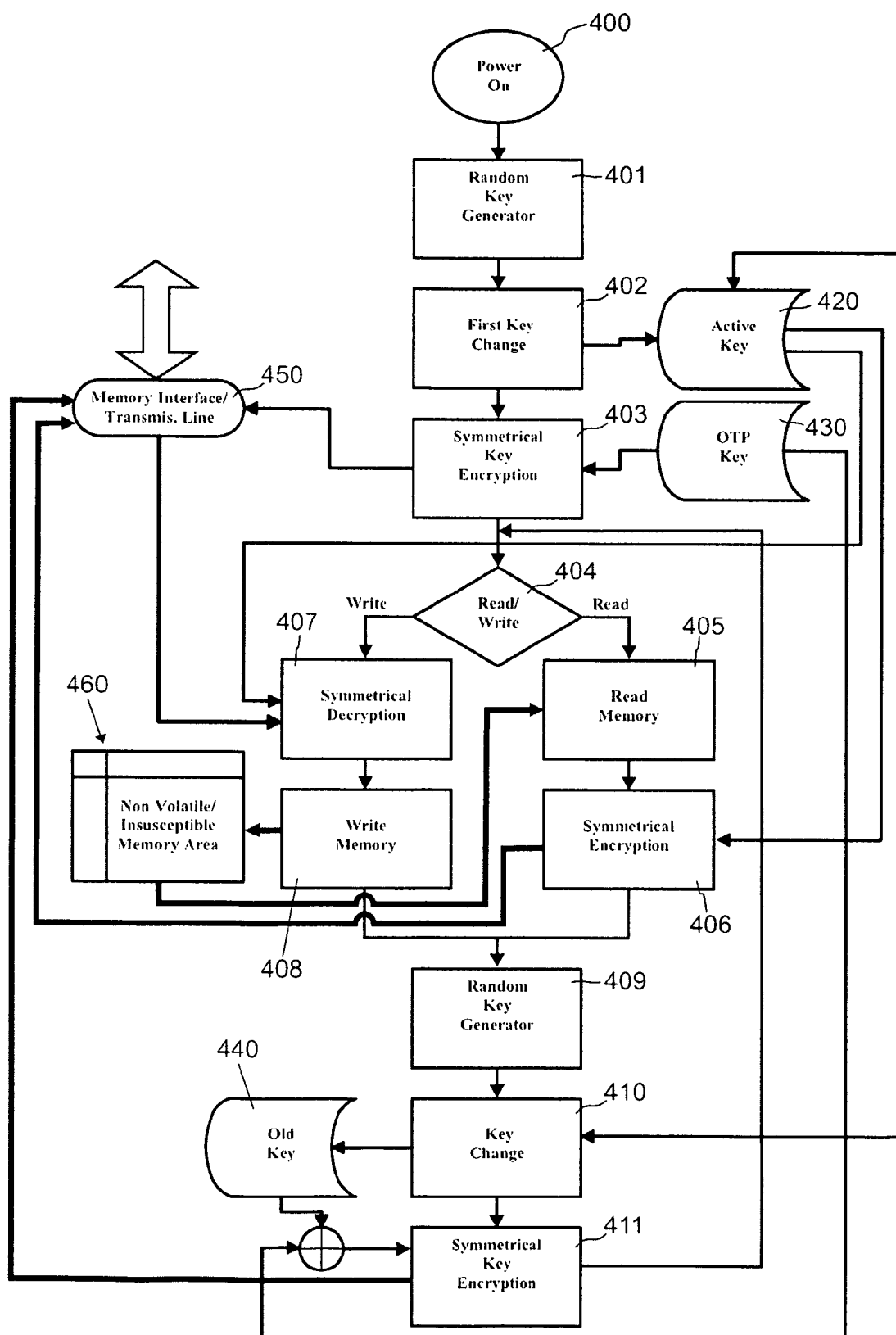


FIG. 4

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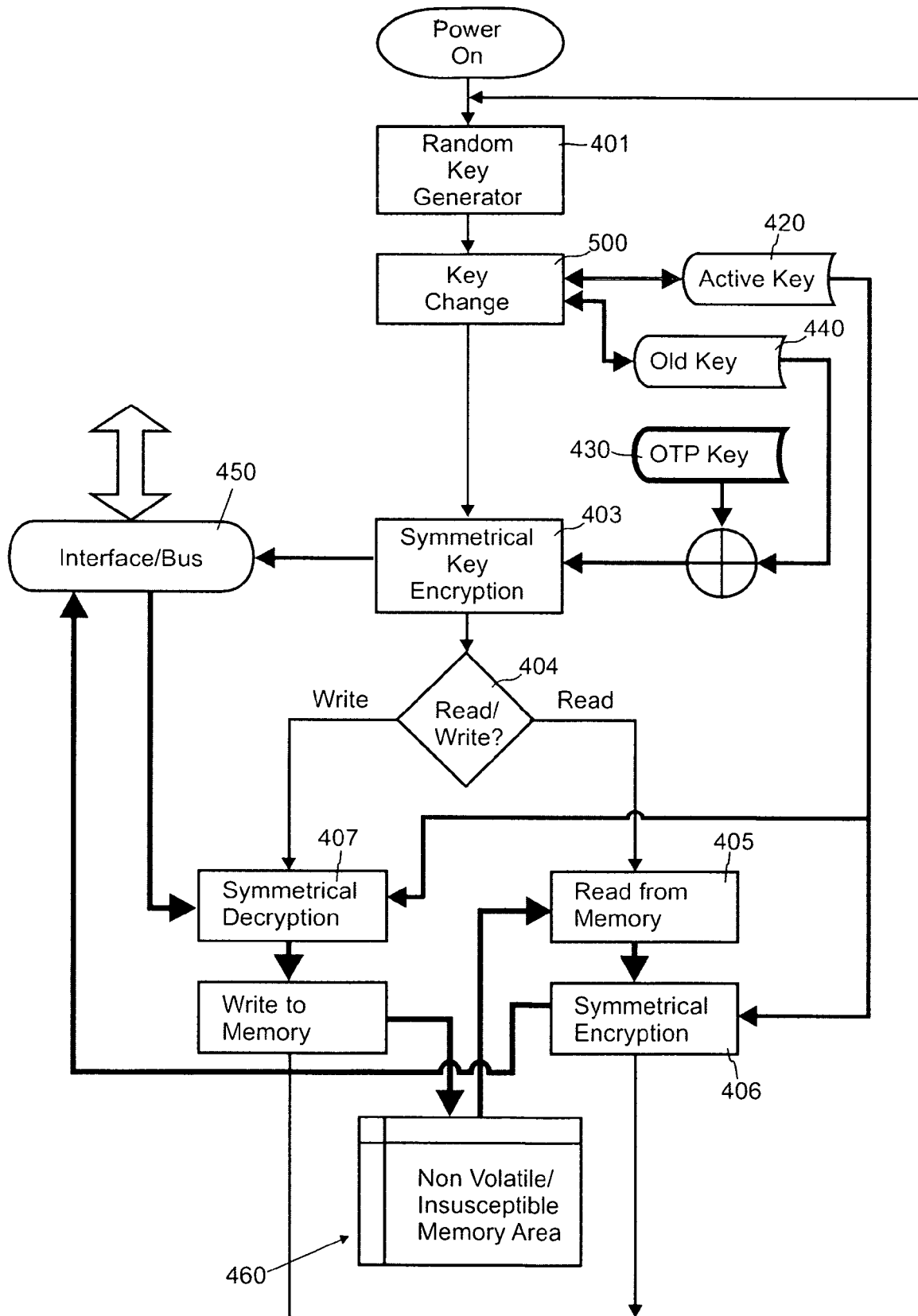


FIG. 5

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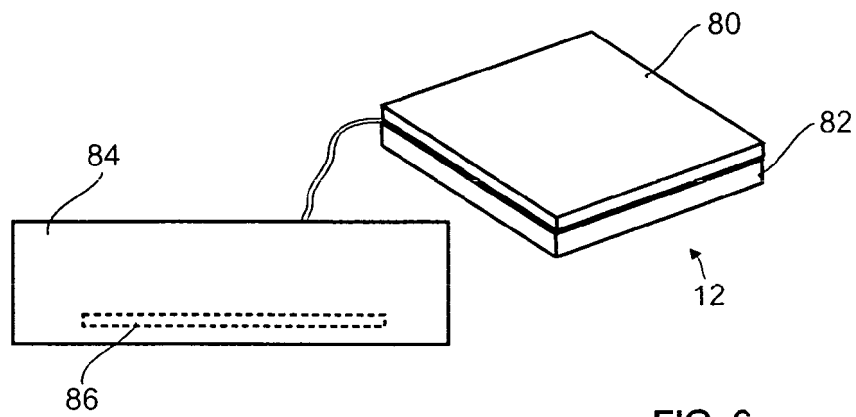


FIG. 6

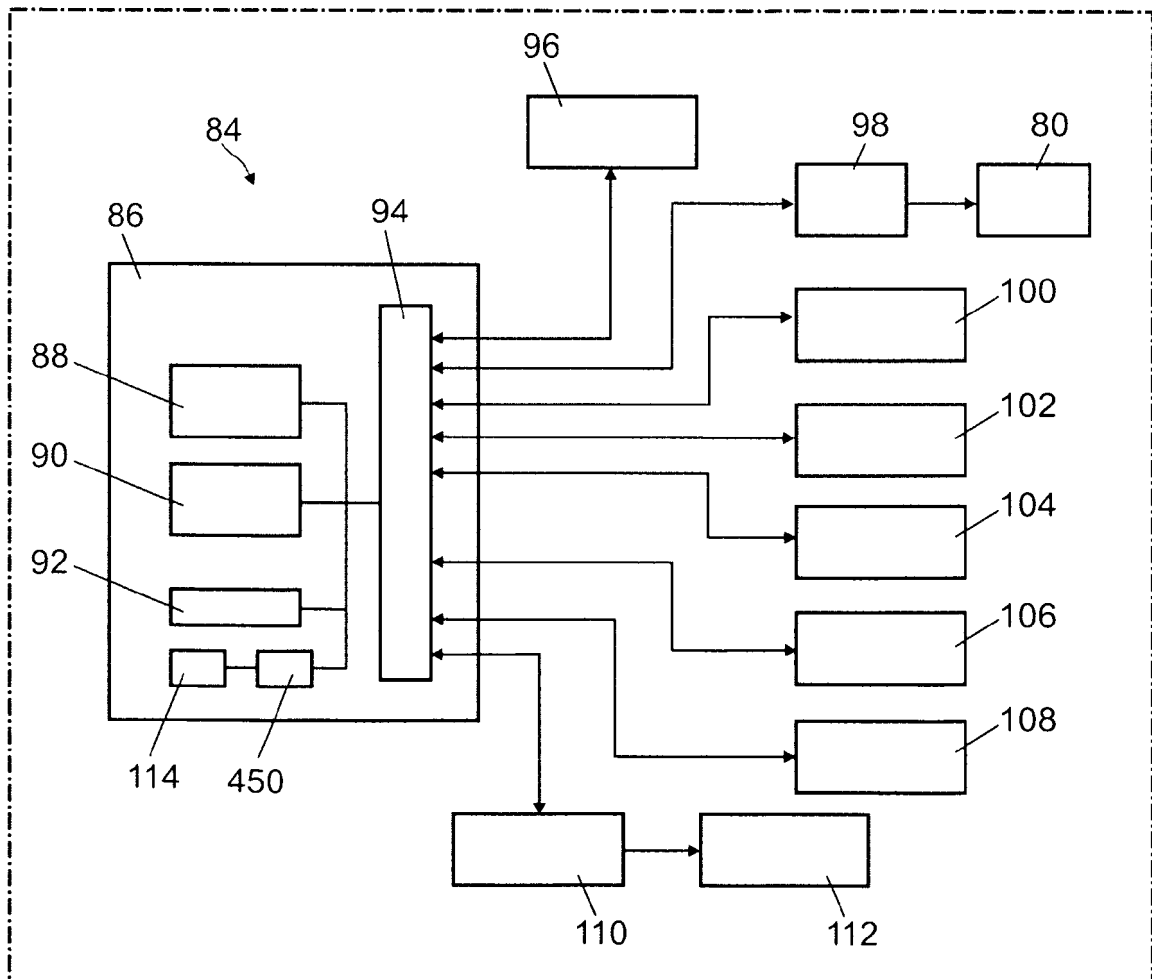


FIG. 7