Claims

What is claimed:

1. A semiconductor device, comprising:

a carrier;

a semiconductor die ~~having~~including an optically active region, the semiconductor die mounted to the carrier such that there is a separation between the carrier and the semiconductor die;

a passivation layer disposed over a surface of the semiconductor die, the passivation layer ~~having~~including a clear portion for passage of light to the optically active region of the semiconductor die;

a glass layer disposed over a surface of the passivation layer;

an encapsulant disposed over the carrier within the separation to form an expansion region around a periphery of the semiconductor die;

a first via penetrating the expansion region, glass layer, and passivation layer;

a second via penetrating the glass layer and passivation layer to expose a contact pad on the semiconductor die; and

a conductive material filling the first via and filling the second via.

2. The semiconductor device of claim 1, further comprising:

a conductive layer disposed between the conductive material in the first and second vias; and

an interconnect structure disposed over the conductive layer.

3. The semiconductor device of claim 1, further comprising:

a conductive layer disposed over a surface of the semiconductor die opposite the optically active region, the conductive layer electrically connected to the conductive material in the first via; and

an interconnect structure disposed over the conductive layer.

4. The semiconductor device of claim 1, wherein the passivation layer is disposed over an entire surface of the semiconductor die.

5. The semiconductor device of claim 4, wherein the glass layer is disposed over an entire surface of the passivation layer.

6. The semiconductor device of claim 1, the expansion region comprising an enclosure disposed around the semiconductor die, the encapsulant filling the enclosure.

7. A semiconductor device, comprising:

a carrier;

a semiconductor die ~~having~~including an optically active region, the semiconductor die mounted to the carrier such that there is a separation between the carrier and the semiconductor die;

a passivation layer disposed over a surface of the semiconductor die, the passivation layer ~~having~~including a clear portion for passage of light to the optically active region of the semiconductor die;

a glass layer disposed over a surface of the passivation layer;

a first conductive via penetrating through the glass layer and the passivation layer to contact a contact pad on the semiconductor die; and

an encapsulant disposed over the carrier within the separation to form an expansion region around the semiconductor die.

8. The semiconductor device of claim 7, further comprising:

a second conductive via penetrating through the expansion region, the glass layer, and the passivation layer;

a conductive layer disposed between the first conductive via and second conductive via; and

an interconnect structure disposed over the conductive layer.

9. The semiconductor device of claim 7, further comprising an enclosure disposed around the semiconductor die, the enclosure filled with the encapsulant.

10. The semiconductor device of claim 7, further comprising a second conductive via penetrating the semiconductor die, the second conductive via electrically connected to the first conductive via.

11. The semiconductor device of claim 10, further comprising:

a conductive layer disposed over a surface of the semiconductor die opposite the optically active region, the conductive layer electrically connected to the second conductive via; and

an interconnect structure disposed over the conductive layer.

12. A semiconductor device, comprising:

~~a carrier;~~

a semiconductor die ~~mounted to the carrier, the semiconductor die having~~ including an optically active region;

a passivation layer disposed over the semiconductor die in contact with the optically active region, the passivation layer ~~having~~ including a clear portion on the optically active region for passage of light to the optically active region of the semiconductor die;

an encapsulant disposed ~~over~~around a periphery of the ~~carrier within the separation~~ semiconductor die to form an ~~expansion~~extension region around the semiconductor die; and

a first conductive via formed through the ~~expansion~~ extension region around the periphery of the semiconductor die.

13. The semiconductor device of claim 12, further comprising a glass layer disposed over the passivation layer.

14. The semiconductor device of claim 12, further comprising a glass layer disposed over the clear portion of the passivation layer.

15. The semiconductor device of claim 12, further comprising a conductive layer disposed over a surface of the semiconductor die ~~common with the optically active region~~, the conductive layer electrically connected to the first conductive via.

16. The semiconductor device of claim 15, further comprising an interconnect structure disposed over the conductive layer.

17. The semiconductor device of claim 12, wherein the first conductive via extends through the passivation layer.

18. The semiconductor device of claim 12, further comprising:

a conductive layer disposed over a surface of the semiconductor die opposite the optically active region, the conductive layer electrically connected to the first conductive via; and

an interconnect structure disposed over the conductive layer.

19. The semiconductor device of claim 12, further comprising a second conductive via extending through the passivation layer to the semiconductor die.

20. A semiconductor device, comprising:

a semiconductor die ~~having~~including an optically active region that converts light to an electrical signal;

a passivation layer formed ~~over~~ on the optically active region of the semiconductor die, the passivation layer allowing for passage of light to the optically active region of the semiconductor die;

a glass layer disposed on the passivation layer to pass the light through the glass layer to the optically active region of the semiconductor die; and

an interconnect structure disposed around a periphery of the semiconductor die~~providing electrical connection between a contact pad of the semiconductor die and front and back sides of the semiconductor package~~.

21. The semiconductor device of claim 20, wherein the interconnect structure comprises:

an expansion region formed around the semiconductor die;

a through hole via (THV) formed in the expansion region;

a conductive material deposited in the THV;

a first intermediate conduction layer electrically connected between the THV and a contact pad of the semiconductor die; and

a first under bump metallization (UBM) layer formed over and electrically connected to the first intermediate conduction layer.

22. The semiconductor device of claim 2~~0~~1, wherein the interconnect structure further comprises a second intermediate conduction layer over the passivation layer and electrically connected between the THV and the first UBM layer.

23. The semiconductor device of claim 21, further comprising:

a second intermediate conduction layer formed on a backside of the semiconductor die; and

a second UBM layer formed over and electrically connected to the second intermediate conduction layer.

~~24. The semiconductor device of claim 20, further comprising a glass layer disposed over the passivation layer.~~

2~~5~~4. The semiconductor device of claim 2~~4~~0, wherein the glass layer is disposed over a clear portion of the passivation layer.

25. A semiconductor device, comprising:

a semiconductor die including an optically active region;

a passivation layer disposed over the semiconductor die and including a clear portion for passage of light to the optically active region of the semiconductor die;

an encapsulant disposed over the semiconductor die to form an extension region around the semiconductor die; and

a first conductive via formed through the extension region around the semiconductor die.

26. The semiconductor device of claim 25, further including a glass layer disposed over the clear portion of the passivation layer.

27. The semiconductor device of claim 25, further comprising a conductive layer disposed over a surface of the semiconductor die and electrically connected to the first conductive via.

28. The semiconductor device of claim 27, further comprising an interconnect structure disposed over the conductive layer.