

PATENT SPECIFICATION

(11) 1 534 556

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- (21) Application No. 46800/76 (22) Filed 10 Nov. 1976
(31) Convention Application No. 50/135565
(32) Filed 11 Nov. 1975 in
(33) Japan (JP)
(44) Complete Specification published 6 Dec. 1978
(51) INT CL² G04C 3/00 G04F 10/00
(52) Index at acceptance
G3T 101 301 402 403 AAA



(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic timepieces and has for its object to provide improved and relatively simple electronic timepieces which can be used at will as a chronograph timepiece (stop watch) or to display time in accordance with either of two desired time standards, e.g. GMT or Japanese standard time.

The invention, though not limited to its application thereto, is very advantageously applicable to electronic digital wrist watches.

With the advances made in recent years in the technology of miniaturisation, and especially in integrated circuit construction the space necessary to accommodate time measuring circuits has become very small so that even in a wrist watch, there is space to spare after the apparatus necessary to count and display time in the ordinary way has been fitted in the watch case. It would be very attractive to a timepiece user who travels a great deal to provide a timepiece which can, at will, display ordinary time (e.g. GMT in the United Kingdom) or some other time (e.g. BST or Eastern Standard Time, or Japanese time or, indeed any other selected time) as may be desired. It would also be very attractive to many users, whether travellers or not, to provide a timepiece which can be used, at will, as a stop watch or chronograph, displaying chronograph time.

As will be seen later the invention provides improved, simple and easily operated timepieces which can be used as chronographs as well as ordinary time keepers and which will display, at will, time in either of a plurality of different chosen time standard times or chronograph time.

According to this invention there is provided an electronic timepiece comprising a time standard oscillator, at least first,

secondary and additional time counting means for counting time signals derived from said oscillator, means for controlling said additional time counting means to operate as chronograph time counting means, a common-display, and means, operable at will and comprising a plurality of selecting gate circuits each controllable to select, as its output, one of a plurality of count inputs, one from each of the time counting means, for selecting the count in any one of said time counting means for display by said common display.

Preferably each of the timekeeping means comprises a seconds counter, a minutes counter and a 24 hours counter.

Each of the selecting gate circuits may comprise a plurality of sets of transmission gates each set being connected to receive BCD bit outputs from the respective counters, each in one of the time counting means, and means for selectively rendering said sets conductive, one at a time, to transmit the input signals thereto to output terminals, and control of the selecting gate circuits may be effected by a display selecting control circuit including a manually operable display selecting switch and having a plurality of output terminals, at which a control signal successively appears in response to successive operations of said switch.

Chronograph operation of the counter in the additional time-keeping means may be controlled by a chronograph control circuit in turn controlled by a manually operable chronograph switch successive operations of which reset said counters and effect the starting and stopping of counting therein.

The timepiece may comprise separate independently operable means for correcting and adjusting the time counting means other than the aforesaid additional time counting means.

The common display may be a numeric liquid crystal display but other suitable forms of display may be used.

The invention is illustrated in and further explained in connection with the accompanying drawings in which:—

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Figure 1 is a block diagram of one embodiment of this invention;

Figure 2 is a circuit diagram of a preferred form for the 24 hours counters included in Figure 1;

Figure 3 is a waveform diagram explanatory of the operation of Figure 2;

Figure 4 is a circuit diagram of a preferred form of the chronograph control circuit included in Figure 1;

Figure 5 is a waveform diagram explanatory of the operation of the circuit shown in Fig. 4;

Figure 6 is a circuit diagram of a preferred form of the display selecting circuit shown in Figure 1;

Figure 7 is a waveform diagram explanatory of the operation of the circuit shown in Figure 6; and

Figure 8 is a circuit diagram of a preferred form for the selecting gate circuits included in Figure 1.

Referring to Figure 1, block 1 represents a relatively high frequency time standard time oscillator constituted by a quartz crystal controlled oscillator the output from which is divided in frequency by a multi-stage frequency divider 2 to produce a standard frequency signal, in the present example a frequency of 1 Hz, which is used as the standard frequency for time measurement. The 1 Hz output from divider 2 is fed to a first time counter 3 comprising a seconds counter 4 consisting of a 10-counter and a 6-counter, the minutes counter 5 also consisting of a 10-counter and a 6-counter and a 24-hours counter 6. The 1 Hz signal from divider 2 is also fed to a second time counter 7 comprising a seconds counter 8 consisting of a 10-counter and a 6-counter, a minutes counter 9 also consisting of a 10-counter and a 6-counter and another 24-hours counter 10. The said 1 Hz signal from divider 2 is also fed to a chronograph unit 12 comprising a chronograph control circuit 13, another seconds counter 14, another minutes counter 15 and another 24-hours counter 16. Time adjustment and setting of the first and second time counters 3 and 7 can be made by time adjusting and setting circuit means represented by block 11.

The BCD coded count content of the seconds counter 4 in the first time counter 3 is fed to a selecting gate circuit 17; the BCD coded count content of the minutes counter 5 is fed to a selecting gate circuit 18; and the count content of the hour counter 6 is similarly fed to a selecting gate circuit 19.

The BCD coded count content of the seconds counter 8 of the second time counter 7 is also fed to the selecting gate circuit 17; and the count contents from the minutes counters 9 and 10 are similarly fed to the selecting gate circuits 18 and 19 respectively.

When a switch (not separately shown in

Figure 1) is actuated the chronograph control circuit 13 passes the 1 Hz signal it receives from the divider 2 to the seconds counter 14 and at the same time produces a reset pulse which is fed to the three counters 14, 15 and 16 and resets them. The 1 Hz output from the control circuit 13 is fed, as above stated, to the seconds counter 14, the BCD coded count content of which is fed to the selecting gate circuit 17. Similarly the count contents of the counters 15 and 16 are fed to the selecting gate circuits 18 and 19 respectively.

The selecting gate circuit 17 thus has three count inputs (from counters 4, 8 and 14); selecting gate circuit 18 has three count inputs (from counters 5, 9 and 15); and selecting gate circuit 19 has similarly three count inputs (from counters 6, 10 and 16). Each selecting gate circuit can select only one of its three count inputs and pass it on to a decoder-driver 21. Thus, in dependence upon the way in which the selecting gate circuits 17, 18 and 19 are controlled, the decoder-driver 21 will receive BCD coded counts from the first time counter 3 or from the second time counter 7 or from the counters in the chronograph unit 12. The decoder-driver 21 converts in any convenient manner well known per se the selected BCD coded inputs it receives into signals in a code suitable for operating a numeric display 22, such as a liquid crystal display comprising 7-segment alpha-numeric display elements as known per se and applies the converted signals to operate said display which will accordingly display numerically the counts from the counters in the first time counter 3 or from the counters in the second time counter 7 or from the counters in the chronograph unit 12, depending upon the selection effected by the selecting gates 17, 18 and 19.

Figure 2 is a circuit diagram of a preferred form for the 24-hours counter 6 of Figure 1. The hours counters 10 and 16 of Figure 1 are similar.

Referring to Figure 2, the 24-hours counter therein shown is a 6-bit counter comprising six flip-flops (hereinafter referred to as "FF") 23, 24, 25, 26, 27 and 28. The lower four bits of this counter, i.e. the bits having output terminals referenced 6A, 6B, 6C and 6D, provide the hour units outputs and the upper two bits, i.e. the bits having output terminals 6E and 6F, provide the tens hour outputs.

1-hour pulses from the minutes counter 5 of Figure 1 are fed to the clock input terminals C_{23} and C_{25} of FF 23 and FF 25 and also to one input of a NOR gate 32. The output terminal Q_{23} of FF 23 is connected to terminal 6A and to one input terminal of a NOR gate 29 the output of which is connected to the data input terminal D_{23} of FF

23. The inverted output terminal $\bar{Q}_{23}$ is connected to the clock input terminal C_{24} of FF

24 and also to one input of a NOR gate 30 the output of which is connected to the data input terminal D_{25} of FF 25. The output terminal Q_{24} of FF 24 is connected to output terminal 6B and the inverted output terminal $\bar{Q}_{24}$ is connected to the data input terminal D_{24} of said FF 24 and also to the remaining input terminal of NOR gate 30.

The output terminal Q_{25} of FF 25 is connected to the output terminal 6C and also to the remaining input of NOR gate 29. The inverted output terminal $\bar{Q}_{25}$ of FF 25 is connected to the clock terminal C_{26} of FF 26 and also to one input of a NOR gate 31.

The output terminal Q_{26} of FF 26 is connected to the output terminal 6D and the inverted output terminal $\bar{Q}_{26}$ is connected to the data input terminal D_{26} and also to the clock terminal C_{27} of FF 27.

The output terminal Q_{27} is connected to the output terminal 6E and the inverted output terminal $\bar{Q}_{27}$ is connected to the data input terminal D_{27} and also to the remaining input terminal of NOR gate 31.

The output of NOR gate 31 is connected to one input of a NOR gate 33 the output of which is connected to the remaining input terminal of NOR gate 32. The output of NOR gate 32 is connected to the remaining input of NOR gate 33 and also to all the reset terminals R of the six flip-flops 23 to 28. The output of each flip-flop changes at the leading edge of a signal fed to its clock terminal.

The action of the counter shown in Figure 2, will now be explained with reference to the waveform diagram shown in Figure 3 in which waveforms occurring at various points in Figure 2 are identified by the same references which are used for the respective points with an added α suffix. Line 5a of Figure 3 shows the 1-hour pulses fed from the minute counter 5, 9 or 15, to the counter 6, 10 or 16, as the case may be. These 1-hour pulses have, in the present example, a duration of 0.5 sec. and, of course, a period of 1 hour. For obvious reasons of difficulty of drawing the pulse width (0.5 sec.) is shown much exaggerated in Figure 3.

Before the first 1-hour pulse is fed out from the minutes counter, i.e. at a time after 0 hour but before 1 hour, the outputs of FF 23 and FF 25 are both logic "0", and output from NOR gate 29 to the data input terminal D_{23} of FF 23 is logic "1". When the first output pulse appears from the minutes counter, the output of FF 23 changes to "1", its inverted output changes to "0" and the output of NOR gate 29 changes to "0". Since the inverted output of FF 24 at the time the leading edge of the pulse from the minutes counter 5 appears is "1", the output of NOR

gate 30 is "0", and therefore the output of FF 25 remains "0" even when the said minutes counter output pulse appears.

Since the output of NOR gate 29 is "0", the output of FF 23 changes to "0" when the second hour pulse appears from the minutes counter, its inverted output changes to "1", the output of FF 24 changes to "1", and its inverted output changes to "0". However, at the time when the above mentioned second pulse is applied, the output of NOR gate 30 and therefore the data input terminal D_{25} of FF 25 is "0" and the output of FF 25 remains unchanged at "0".

Next, when the third hour output pulse appears from the minutes counter, the output of FF 23 changes to "1" and the output of NOR circuit 29 changes to "0". At this time, the data terminal D_{25} that is the output of NOR circuit 30, changes to "1" and the output of FF 25 does not change.

When the fourth hour pulse appears from the minutes counter the output of FF 23 changes to "0" and its inverted output changes to "1". Accordingly, the output of FF 24 changes to "0" and the output of FF 25 changes to "1" for the first time.

Next, when the fifth hour pulse appears from the minutes counter, the output of FF 25 changes to "0" but the outputs of FF 23 and of FF 24 do not change. Consequently, the inverted output of FF 25 changes from "0" to "1" at this time and the output of FF 26 changes to "1" for the first time.

From the sixth hour pulse to the twenty-third hour pulse from the minutes counter, the above described actions are repeated by FF 23 to FF 25, the output of FF 26 changing at the instant when the inverted output of FF 25 changes from "0" to "1", the output of FF 27 changing at the instant when the inverted output of FF 26 changes from "0" to "1" and the output of FF 28 changing at the instant when the inverted output of FF 27 changes from "0" to "1". Therefore, the states of the outputs of the flip-flops 23 to 28 between the time when the twenty-third pulse is applied from the minutes counter and the time when the twenty-fourth hour pulse appears is as follows:— the output of FF 23 is "1", the output of FF 24 is "1", the output of FF 25 is "0", the outputs of FF 26 and FF 27 are "0" and the output of FF 28 is "1". Also the output of NOR gate 29 is "0", the output of NOR gate 30 is "1", the output of NOR gate 31 is "0" and the output of NOR gate 32 is "0".

The inverted output of FF 25 changes to "0" when the twenty-fourth hour pulse appears from the minutes counter and the output of NOR gate 31 changes to "1" since the inverted output of FF 28 remains "0". Accordingly the output of NOR gate 33 changes to "0" and the output of NOR gate 32 becomes "1" at the instant when the

twenty-fourth hour pulse ceases, i.e. at its trailing edge, and this output resets all six flip-flops 23 to 28. This output from NOR gate 32, which resets all the flip-flops changes to "0" at the instant when the next hour pulse, i.e. the twenty-fifth pulse, appears from the minutes counter, the reset of the flip-flops is released and the cycle of operations is repeated.

In this way, since the outputs of the flip-flops 23 to 25 are outputs indicative of the units hours count and the outputs of flip-flops 27 and 28 are indicative of the tens hours count, a 24-hour count is achieved. Although the signals provided at the terminals 6A to 6F are not in accordance with the general BCD code, it will be seen that they are so coded as to be easily converted (in the decoder-driver 21, Figure 1) into coded signals suitable for driving a numeric display (display 22, Figure 1) incorporating alpha-numeric display elements of the customary seven-segment type.

Figure 4 is a circuit diagram of a preferred form of chronograph control circuit constituting the chronograph control circuit 12 of Figure 1. Referring to Figure 4, 34 is a manually operated switch for chronograph operation. One terminal of this switch 34 is connected to the higher voltage terminal 35 of a power supply (not shown) and the other end is connected to the input side of a known anti-chatter circuit 36 for eliminating switch chatter effects which might occur on operation of the switch 34. The output side of circuit 36 is connected to the clock input terminals C_{37} , C_{38} and C_{39} of three flip-flops 37, 38 and 39 and also to the input of an inverter 40. The output terminal Q_{37} of FF 37 is connected to the data input terminal D_{38} and also to an output terminal 13A and to one input of a three-input NOR gate 41. The terminal 13A provides a reset signal which, when it appears, resets the counters 14, 15 and 16 in the chronograph unit 12. The output terminal Q_{38} of FF 38 is connected to the data input terminal D_{39} of FF 39 and also to a second input of the NOR gate 41 and to one input of an AND gate 42. The output terminal Q_{39} of FF 39 is connected to the data terminal D_{37} of FF 37 and also to the remaining input terminal of NOR gate 41. The 1 Hz output from the divider 2 (Figure 1) is fed to the remaining input of AND gate 42 the output from which is fed to the seconds counter 14 (Figure 1) from terminal 13B.

The output of NOR gate 41 is connected to one input of a NOR gate 43 the output of which is connected to one input of a NOR gate 44. The output of inverter 40 is connected to the other input of this NOR gate, the output of which is connected to the remaining input of NOR gate 43 and also to the set terminal S_{37} of FF 37.

The operation of Figure 4 will now be

described with reference to Figure 5 in which waveforms appearing at various points in Figure 4 are identified by the references of said points with an added suffix *a*. Line 2a (which for obvious reasons of difficulty of drawing, does not show the actual numbers of pulses occurring) of Figure 5 represents the 1 Hz pulses fed in to the AND gate 42 from the divider 2 of Figure 1.

When electric power is applied to the entire timepiece, the outputs from FF 37, 38 and 39 are all "0". Therefore, the output of NOR gate 41 is "1". Before the switch 34 is operated, the output of the anti-chatter circuit 36 is "0". Therefore, the input to NOR gate 44 from the inverter 40 is "1" and the output of said NOR gate is "0". If now the switch 34 is closed, a pulse is fed out from the circuit 36 changing (via inverter 40) the output of NOR gate 44 to "1" and changing the output of FF 37 to "1". This output from FF 37 resets the counters 14, 15 and 16 by the signal applied to them from the output terminal 13A. The next time switch 34 is operated, a second pulse appears at the output of the anti-chatter circuit 36, the output of FF 37 changes to "0" and the output of FF 38 changes to "1". Accordingly the 1 Hz signal fed to one input of AND gate 42 is passed thereby to the counters in the chronograph unit 13 (Figure 1) which have been released from reset by the change in the output of FF 37.

If now the switch 34 is operated a third time, a third pulse appears from the anti-chatter circuit 36, the output of FF 38 changes to "0" and the 1 Hz signal is no longer passed by the AND gate 42. Also said third signal changes the outputs of FF 39 to "1". If now the switch 34 is operated a fourth time, the fourth pulse appearing from the anti-chatter circuit 36 changes the output of FF 37 to "1" because the data terminal D_{37} , that is the output of FF 39, is "1", despite that the output of NOR gate 44 remains at logic "0". This output of FF 37 resets the counters, 14, 15 and 16 (Figure 1) in similar manner to that which occurred the first time the switch was operated. The cycle of operations is now complete and will be repeated over the next four operations of switch 34.

Figure 6 is a circuit diagram of a preferred form for the display selecting circuit 20 of Figure 1. Referring to Figure 6 45 is a manually operable switch which is used for selecting the counts to be displayed, i.e. for selecting whether the counts in the first time counter, or in the second time counter or in the chronograph unit are to be displayed. One terminal of this switch is connected to the higher potential terminal 46 of the power supply (not shown) and the other terminal is connected to the input side of an anti-chatter circuit 47 the output of which is connected to the clock terminals, C_{43} , C_{45} and C_{60} of three flip-

flops 48, 49 and 50 and also to the input of an inverter 51. The output terminal Q_{48} of FF 48 is connected to the data terminal D_{49} of FF 49 and also to an output terminal 20A and to one input of a three-input NOR gate 52. The output terminal Q_{49} of FF 49 is connected to the data terminal D_{50} of FF 50 and to a second input of NOR gate 52 and to a second output terminal 20B. The output terminal Q_{50} of FF 50 is connected to the data input terminal D_{48} of FF 48 and also to the remaining input terminal of NOR gate 52 and to a third output terminal 20C.

The output of NOR gate 52 is connected to one input of a NOR gate 53 the output of which is connected to one input of a NOR gate 54 the other input of which is connected to the output of inverter 51. The output of NOR gate 54 is connected to the remaining input of NOR gate 53 and to the set terminal S_{48} of FF 48.

The operation of the display selecting circuit 20 will now be described with reference to the waveform diagram of Figure 7 in which waveforms appearing at various points in Figure 6 are identified by the references used for those points with an added suffix *a*.

When electric power is applied to the entire timepiece the outputs of the flip-flops 48, 49 and 50 are all "0". Therefore, the output of NOR gate 52 is "1". Before the switch 45 is operated, the output of the anti-chatter circuit 47 is "0", the output side of the inverter 51 is "1" and the output of NOR gate 54 is "0". If, now, the switch 45 is operated, a first pulse will appear from circuit 47 and the output of NOR gate 54 will change to "1". This sets FF 48 and its output becomes "1". This output appears at the first output terminal 20A.

If, now, switch 45 is operated a second time, a second pulse appears from circuit 47 and is applied to the clock input terminal C_{49} of FF 49, the output of FF 49 becomes "1", and the output of FF 48 changes to "0". This output from FF 49 appears at the second output terminal 20B.

On the third operation of switch 45 a third pulse appears from the anti-chatter circuit 47 and is applied to the clock input terminal C_{50} of FF 50, the output of FF 50 becomes "1", and the output of FF 49 changes to "0". The output of FF 50 appears at the third output terminal 20C.

On operating the switch 45 a fourth time, a fourth pulse appears from the anti-chatter circuit 47, the output of FF 48 changes to "1" because of the signal applied to its data input terminal D_{48} , i.e. the "1" output from FF 50, despite that the output of NOR gate 54 is "0". As will be seen the output of NOR gate 54 is not operative to cause any action if the output of any one of the flip-flops 48 to 50 is "1". The action of the flip-flops 48 to 50 is like that of a ring counter and a "1"

signal appears successively at the output terminals 20A to 20C on successive operations of the switch 45.

Figure 8 is a circuit diagram of a preferred form of the selecting gate circuit 17 (Figure 1). The selecting gate circuits 18 and 19 are similar.

Referring to Figure 8, terminals 20A, 20B and 20C are, electrically, the same terminals as those to which those references are applied in Figure 6. Terminal 17A is connected, through an inverter 55, to the gate electrodes on the respective P channel sides of seven transmission gates (hereinafter referred to as "TG") 56, 57, 58, 59, 60, 61 and 62. The terminal 20A is also connected directly to the gate electrodes on the respective N channel sides of TGs 56 to 62. In the same way, the input terminal 20B is connected, through an inverter 63, to the gate electrodes on the respective P channel sides of seven TGs 64, 65, 66, 67, 68, 69 and 70. The input terminal 20B is also connected directly to the respective gate electrodes on the N channel sides of TGs 64 to 70. Input terminal 20C is connected, through an inverter 71, to the respective gate electrodes on the P channel sides of seven TGs 72, 73, 74, 75, 76, 77, and 78. The input terminal 20C is also connected directly to the respective gate electrodes on the N channel sides of TGs 72 to 78. The respective 7-bit outputs of the 60-seconds counter 4 (the first of the counters in the first time counter 3 of Figure 1) are connected to the respective inputs of TGs 56 to 62. The respective 7-bit outputs of the seconds counter 8 (the first of the counters in the secondary counter 7 of Figure 1) are connected to each of the respective inputs of the TGs 64 to 70. The respective 7-bit outputs of the seconds counter 14 (the first of the counters in the chronograph unit 12 of Figure 1) are connected to the respective inputs of the TGs 72 to 78. The outputs of the TGs 56, 64 and 72 are connected together and to the output terminal 17D; the outputs of the TGs 57, 65 and 73 are connected together and to the output terminal 17E; the outputs of the TGs 58, 66 and 74 are connected together and to the output terminal 17F; the outputs of the TGs 59, 67 and 75 are connected together and to the output terminal 17G; the outputs of TGs 60, 68 and 76 are connected together and to the output terminal 17H; the outputs of the TGs 61, 69 and 77 are connected together and to the output terminal 17I; and the outputs of the TGs 62, 70 and 78 are connected together and to the output terminal 17J. If a "1" signal is applied to the input terminal 20A, TGs 56 to 62 become "ON" and the count contents of the seconds counter 4 are fed to the output terminals 17D to 17J: if a "1" signal is applied to the input terminal 20B, TGs 64 to 70 become "ON" and the count contents of the seconds counter 8 are

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fed to the output terminals 17D to 17J; or if a "1" signal is applied to the input terminal 20C, TGs 72 to 78 become "ON" and the count contents of the seconds counter 14 are fed to the output terminals 17D to 17J. A "1" signal is fed successively to the input terminals 20A to 20C in response to successive operations of the switch 45 of the display selecting circuit (Figure 6) and therefore each such successive operation will cause the selecting gate circuit of Figure 8 to select a successively different one of the counters 4, 8 and 14 for passing its BCD coded count output via terminals 17D to 17J, to the decoder-driver 21 (Figure 1). The selecting gate circuit 18 is similar to that shown in Figure 8 and selects one of the counters 5, 9 or 15 and the selecting gate 19 for selecting one of the hours counters 6, 10 or 16 is also similar except, of course, that it has 18 transmission gates (six in each of three sets instead of seven in each set) because the number of output bits in each 24 hours counter is six.

The time correcting and adjusting means 11, which may take any convenient form known per se, and which provides for independent and separate adjustment of the first time counter 3 and of the second time counter 7 may be used to adjust one of these two time counters to count one time (e.g. GMT) and the other to count time as kept in some other place, e.g. Japanese Standard Time or Eastern Standard Time in the U.S.A. Either of the two times kept by these two counters can be quickly and easily displayed whenever desired by a very simple operation of the display selecting switch 45 which can also be used to select the chronograph display. When chronograph display is selected equally simple operation of the chronograph switch 34 is all that is required to obtain chronograph operation (start-count-stop) and it will be noted that chronograph time measurement can be effected up to a comparatively long time—24 hours—which is often useful, e.g. when it is required to time a motor car race. Thus the invention provides a relatively simple timepiece able to make three independent time measurements and to display at will the measured time obtained by any of them.

Since, with the illustrated embodiment of the invention, all three hours counters are 24-hours counters there is no need for or provision of means, other than the hours counts themselves, for distinguishing between AM and PM.

Attention is directed to the specification accompanying our co-pending Applications Nos. 41306/76, Serial No. 1,526,468, 42969/76, Serial No. 1,532,863, 46170/76, Serial No. 1,527,939, 46802/76 Serial No. 1,534,557 and 47704/76 Serial No. 1,531,769 which claim related subject matter.

Having regard to the provisions of Sec-

tion 9 of the Patents Act, attention is directed to the claims of Patent No. 1,355,161.

WHAT WE CLAIM IS:—

1. An electronic timepiece comprising a time standard oscillator, at least first, secondary and additional time counting means for counting time signals derived from said oscillator, means for controlling said additional time counting means to operate as chronograph time counting means, a common display, and means, operable at will and comprising a plurality of selecting gate circuits each controllable to select, as its output, one of a plurality of inputs, one from each of the time counting means for selecting the count in any one of said time counting means for display by said common display.

2. A timepiece as claimed in claim 1 wherein each of said time counting means comprises a seconds counter, a minutes counter and a 24 hours counter.

3. A timepiece as claimed in claim 2 wherein each selecting gate circuit comprises a plurality of sets of transmission gates each set being connected to receive BCD bit outputs from the respective counters, each in one of the time counting means, and means for selectively rendering said sets conductive, one at a time, to transmit the input signals thereto to output terminals.

4. A timepiece as claimed in claim 2 or 3 wherein control of the selecting gate circuits is effected by a display selecting control circuit including a manually operable display selecting switch and having a plurality of output terminals, at which a control signal successively appears in response to successive operations of said switch.

5. A timepiece as claimed in any of the preceding claims wherein chronograph operation of the counters in the additional time keeping means is controlled by a chronograph control circuit in turn controlled by a manually operable chronograph switch successive operations of which reset said counters and effect the starting and stopping of counting therein.

6. A timepiece as claimed in any of the preceding claims and comprising separate independently operable means for correcting and adjusting the time counting means other than the aforesaid additional time counting means.

7. A timepiece as claimed in any of the preceding claims wherein the common display is a numeric liquid crystal display.

8. A timepiece as claimed in any of the preceding claims wherein each of the time counting means includes a 24 hours counter substantially as herein described with reference to Figures 2 and 3 of the accompanying drawings.

9. A timepiece as claimed in any of the preceding claims and comprising a chronograph control circuit substantially as herein

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fed to the output terminals 17D to 17J; or if a "1" signal is applied to the input terminal 20C, TGs 72 to 78 become "ON" and the count contents of the seconds counter 14 are fed to the output terminals 17D to 17J. A "1" signal is fed successively to the input terminals 20A to 20C in response to successive operations of the switch 45 of the display selecting circuit (Figure 6) and therefore each such successive operation will cause the selecting gate circuit of Figure 8 to select a successively different one of the counters 4, 8 and 14 for passing its BCD coded count output via terminals 17D to 17J, to the decoder-driver 21 (Figure 1). The selecting gate circuit 18 is similar to that shown in Figure 8 and selects one of the counters 5, 9 or 15 and the selecting gate 19 for selecting one of the hours counters 6, 10 or 16 is also similar except, of course, that it has 18 transmission gates (six in each of three sets instead of seven in each set) because the number of output bits in each 24 hours counter is six.

The time correcting and adjusting means 11, which may take any convenient form known per se, and which provides for independent and separate adjustment of the first time counter 3 and of the second time counter 7 may be used to adjust one of these two time counters to count one time (e.g. GMT) and the other to count time as kept in some other place, e.g. Japanese Standard Time or Eastern Standard Time in the U.S.A. Either of the two times kept by these two counters can be quickly and easily displayed whenever desired by a very simple operation of the display selecting switch 45 which can also be used to select the chronograph display. When chronograph display is selected equally simple operation of the chronograph switch 34 is all that is required to obtain chronograph operation (start-count-stop) and it will be noted that chronograph time measurement can be effected up to a comparatively long time—24 hours—which is often useful, e.g. when it is required to time a motor car race. Thus the invention provides a relatively simple timepiece able to make three independent time measurements and to display at will the measured time obtained by any of them.

Since, with the illustrated embodiment of the invention, all three hours counters are 24-hours counters there is no need for or provision of means, other than the hours counts themselves, for distinguishing between AM and PM.

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2. A timepiece as claimed in claim 1 wherein each of said time counting means comprises a seconds counter, a minutes counter and a 24 hours counter.

3. A timepiece as claimed in claim 2 wherein each selecting gate circuit comprises a plurality of sets of transmission gates each set being connected to receive BCD bit outputs from the respective counters, each in one of the time counting means, and means for selectively rendering said sets conductive, one at a time, to transmit the input signals thereto to output terminals.

4. A timepiece as claimed in claim 2 or 3 wherein control of the selecting gate circuits is effected by a display selecting control circuit including a manually operable display selecting switch and having a plurality of output terminals, at which a control signal successively appears in response to successive operations of said switch.

5. A timepiece as claimed in any of the preceding claims wherein chronograph operation of the counters in the additional time keeping means is controlled by a chronograph control circuit in turn controlled by a manually operable chronograph switch successive operations of which reset said counters and effect the starting and stopping of counting therein.

6. A timepiece as claimed in any of the preceding claims and comprising separate independently operable means for correcting and adjusting the time counting means other than the aforesaid additional time counting means.

7. A timepiece as claimed in any of the preceding claims wherein the common display is a numeric liquid crystal display.

8. A timepiece as claimed in any of the preceding claims wherein each of the time counting means includes a 24 hours counter substantially as herein described with reference to Figures 2 and 3 of the accompanying drawings.

9. A timepiece as claimed in any of the preceding claims and comprising a chronograph control circuit substantially as herein



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described with reference to Figures 4 and 5 of the accompanying drawings.

10. A timepiece as claimed in any of the preceding claims and comprising a display selecting control circuit substantially as herein described with reference to Figures 6 and 7 of the accompanying drawings.

11. A timepiece as claimed in any of the preceding claims and comprising selecting gate circuits substantially as herein described with reference to Figure 8 of the accompanying drawings.

12. Electronic timepieces as claimed in any of the preceding claims and substantially as herein described and illustrated in Figure 1 of the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1978
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.