ABSTRACT

NOVEL PROCESS TO ACHIEVE UNIFORM GROOVE DEPTH IN A SILICON SUBSTRATE

A process for forming a groove in a semiconductor substrate, to be used to fabricate grooved gate, MOSFET devices, has been developed. The process features the use of an insulator mask, used as an etch mask for definition of the groove feature in the semiconductor substrate. A selective, anisotropic RIE procedure, using an etchant with a specific etch rate ratio of silicon, (semiconductor substrate), to silicon oxide, (insulator mask), is used to establish the desired groove depth, in the semiconductor substrate. The combination of a specific thickness of insulator shape, and a specific etch rate ratio for the selective, anisotropic RIE procedure, allows the desired depth of the groove to be established when the insulator shape is completely removed from the top surface of the semiconductor substrate. The groove depth established at this point of the RIE procedure, will not change during an overetch cycle, as a result of etching the now exposed, top surface of the semiconductor surface, at the same rate as exposed semiconductor, located at the bottom of the groove.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)