(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 December 2004 (29.12.2004)

PCT

(10) International Publication Number
WO 2004/114396 A1

(51) International Patent Classification[7]: H01L 21/768

(21) International Application Number:
PCT/EP2004/051131

(22) International Filing Date: 16 June 2004 (16.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/604,056 24 June 2003 (24.06.2003) US

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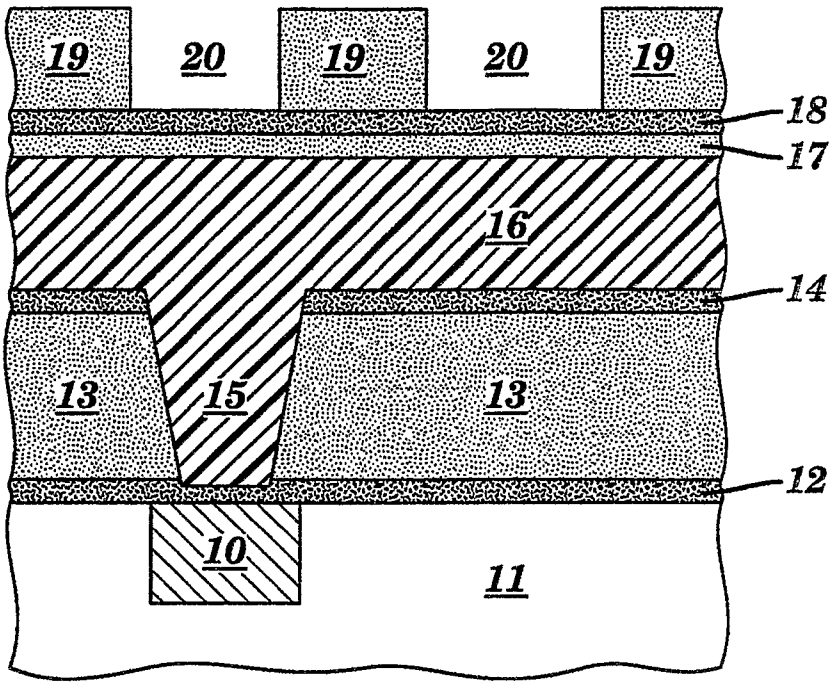
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

[Continued on next page]

(54) Title: INTERCONNECT STRUCTURES IN INTEGRATED CIRCUIT DEVICES



(57) Abstract: This invention relates to the manufacture of dual damascene interconnect structures in integrated circuit devices. Specifically, a method is disclosed for forming a single or dual damascene structure in a low-k dielectric thin film utilizing a planarizing material and a diffusion barrier material. In a preferred dual damascene embodiment of this method, the vias are formed first in the dielectric material (13), then the planarizing material (16) is deposited in the vias and on the dielectric material, and the barrier material (17) is deposited on the planarizing material. The trenches are then formed lithographically in the imaging material (19), etched through the barrier material into the. planarizing material, and the trench pattern is transferred to the dielectric material. During and following the course of these etch steps, the imaging, barrier and planarizing materials are removed. The resultant dual damascene structure may then be metallized. With this method, the problem of photoresist poisoning by the interlevel dielectric material is alleviated.

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GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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