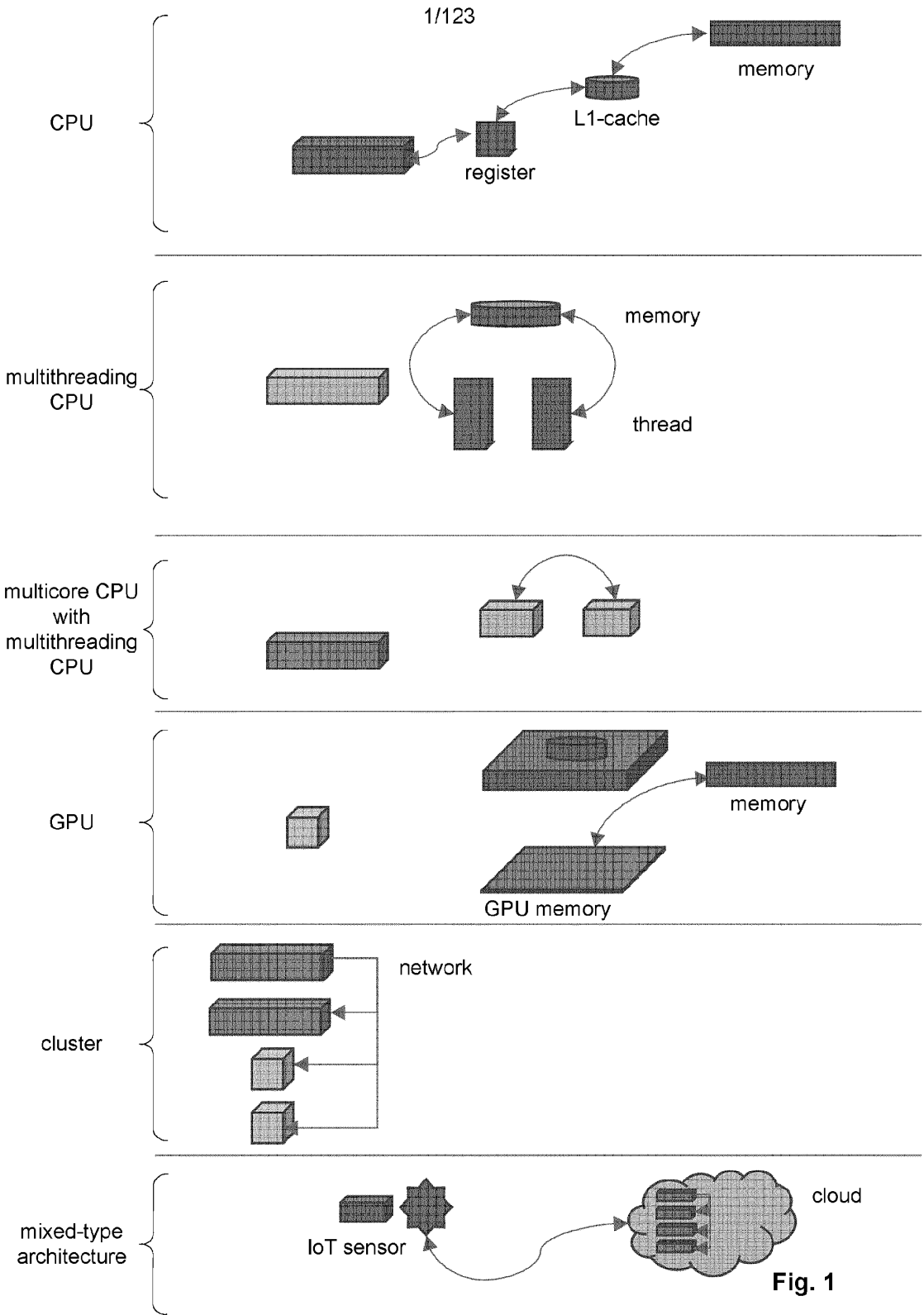




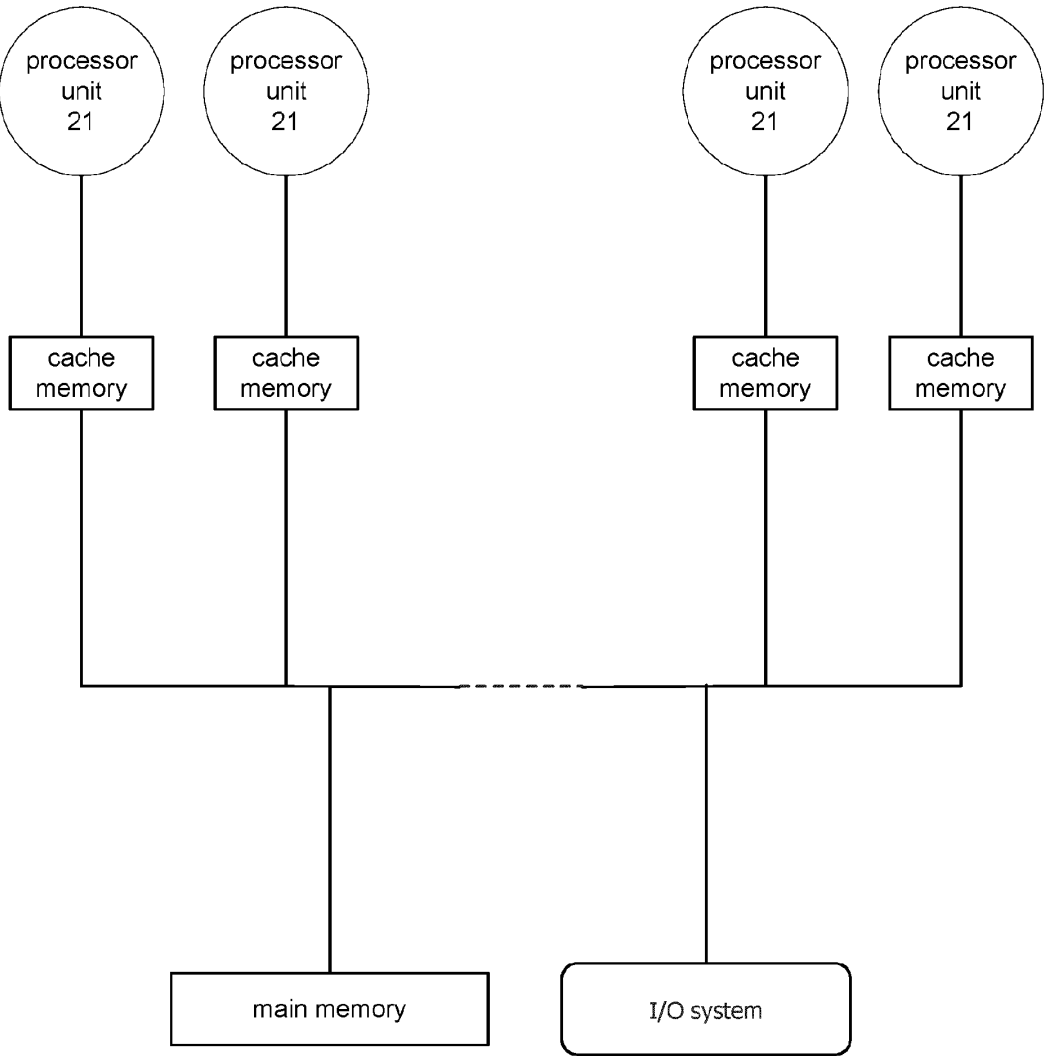


Fig. 2

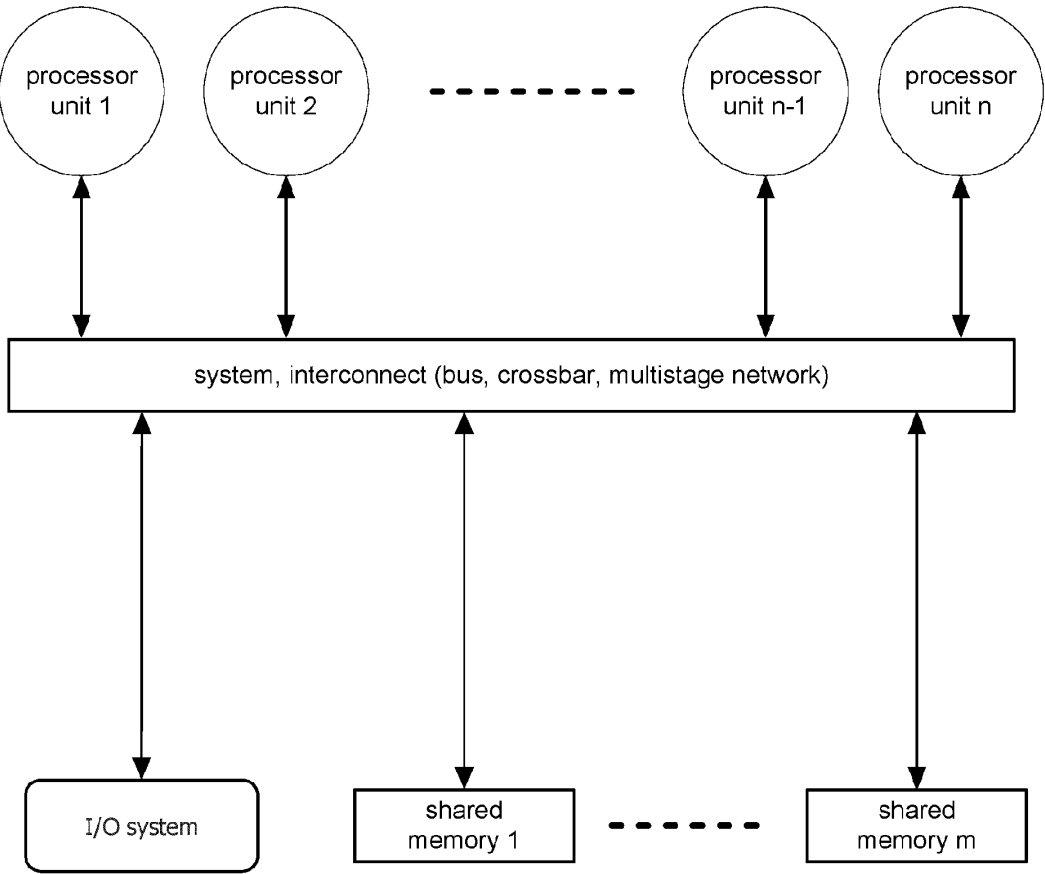


Fig. 3

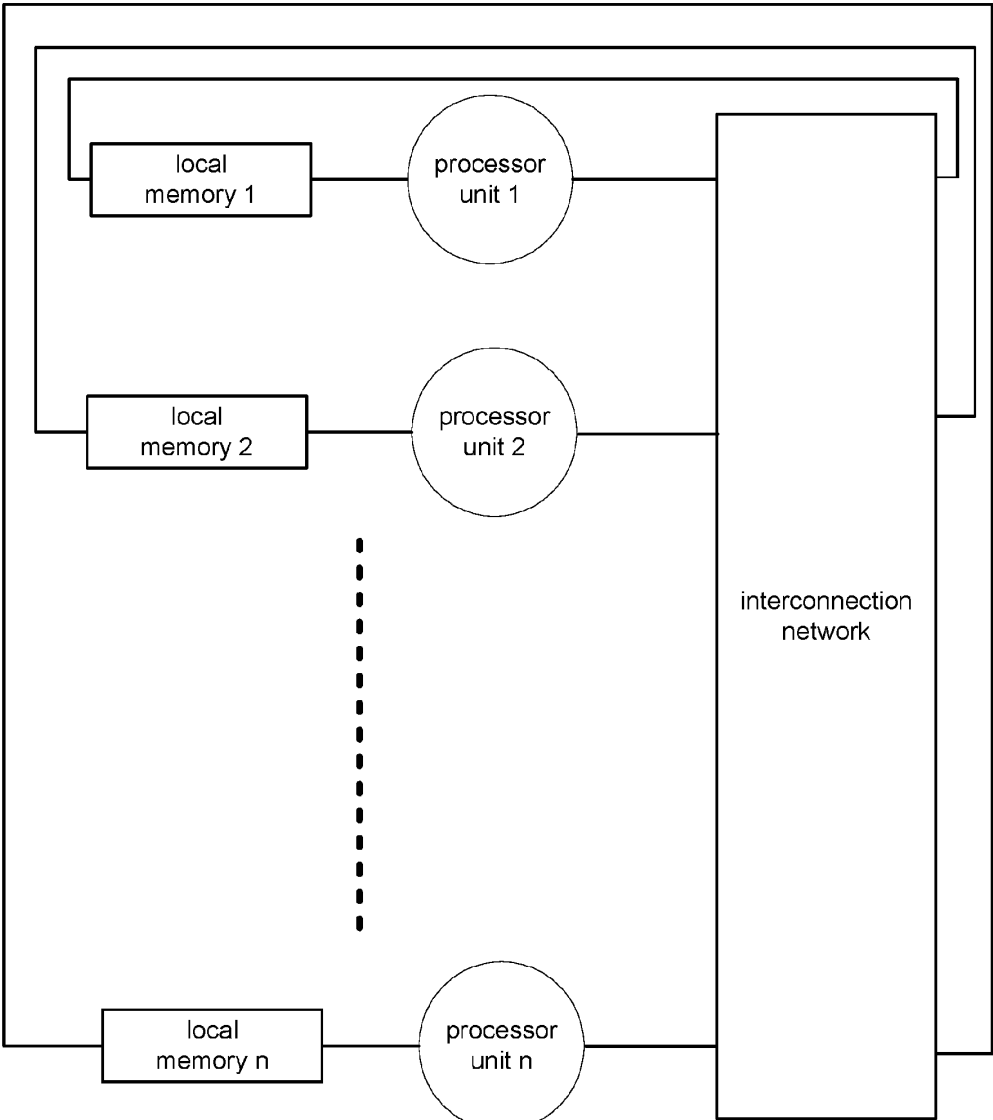


Fig. 4

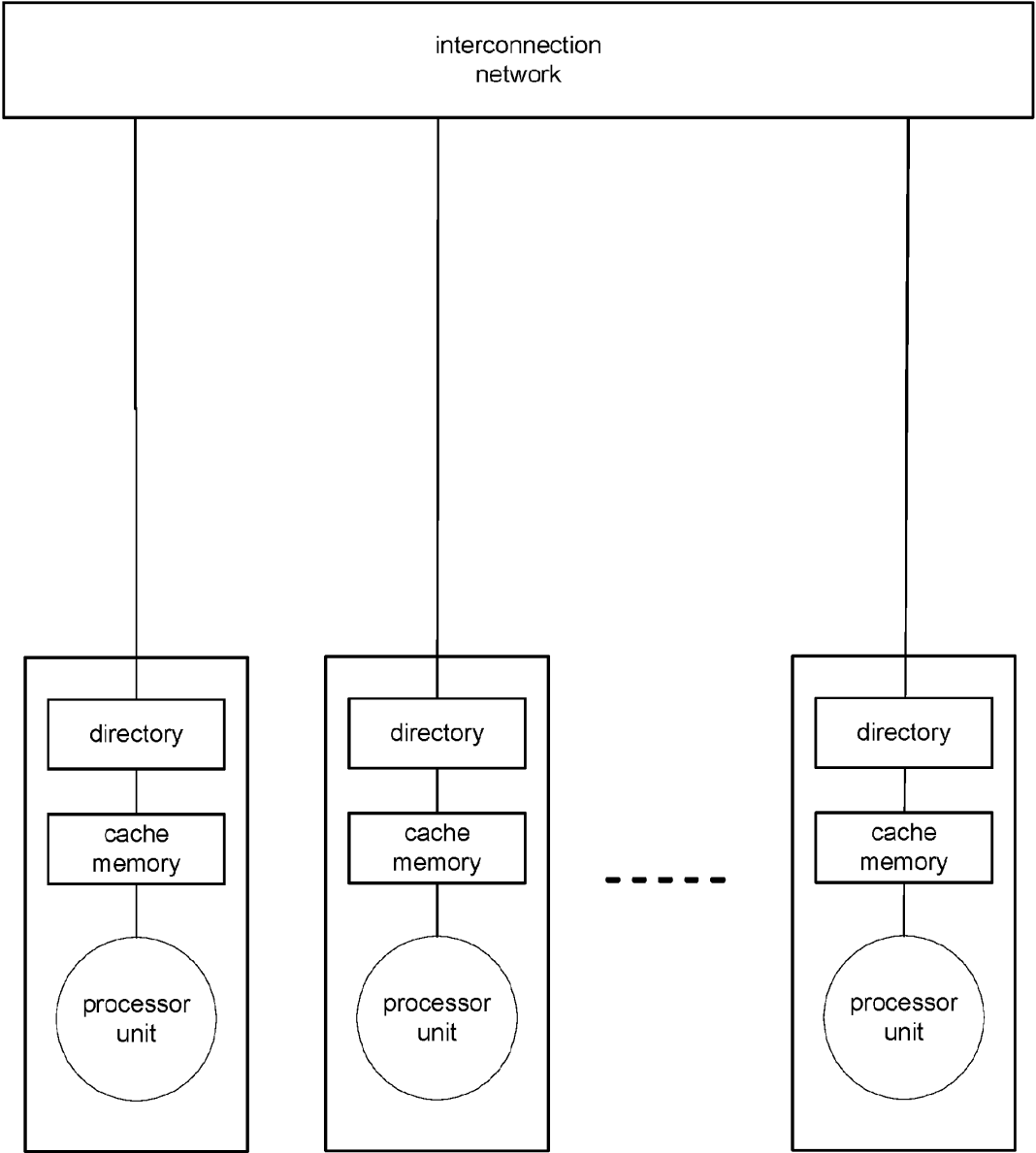


Fig. 5

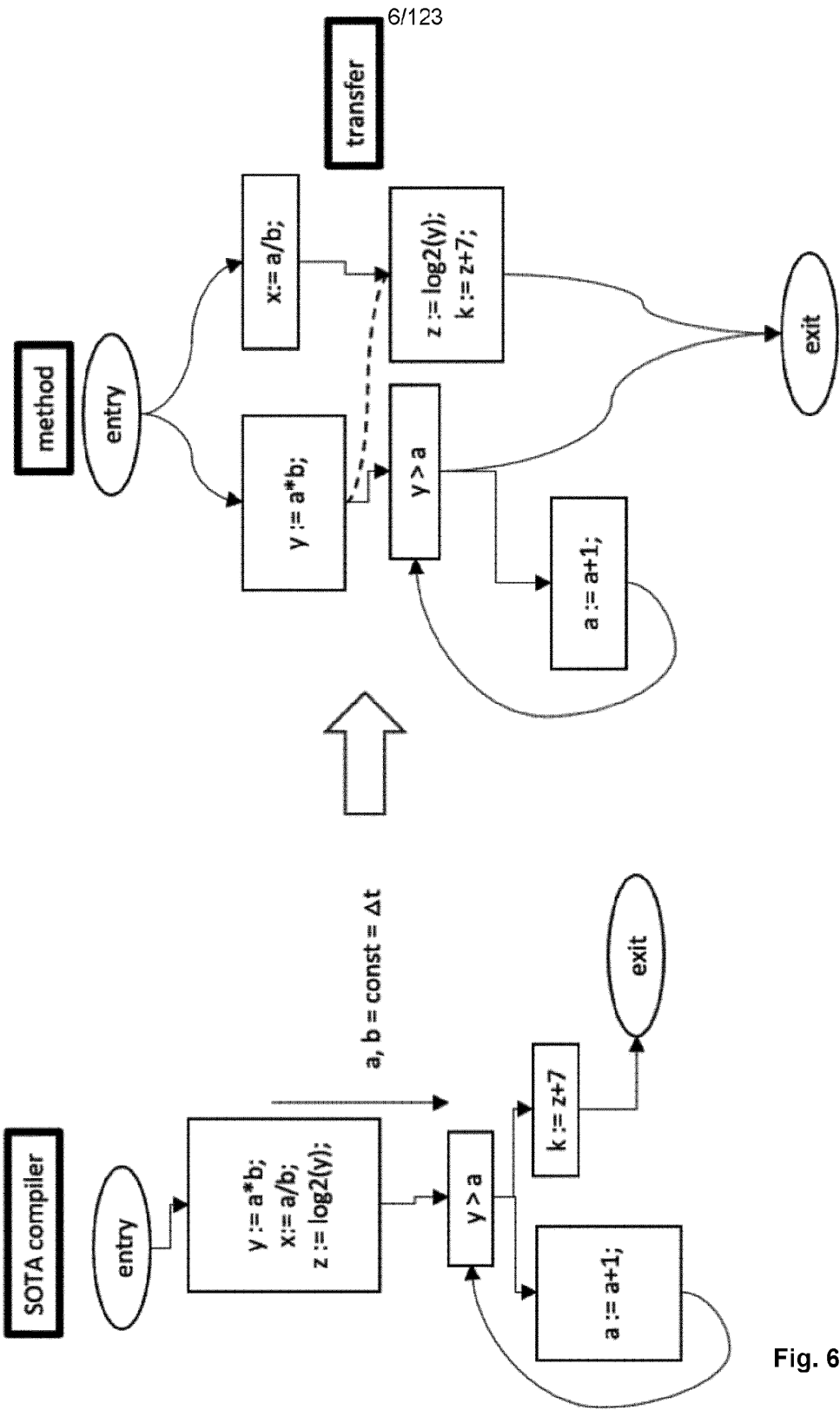


Fig. 6

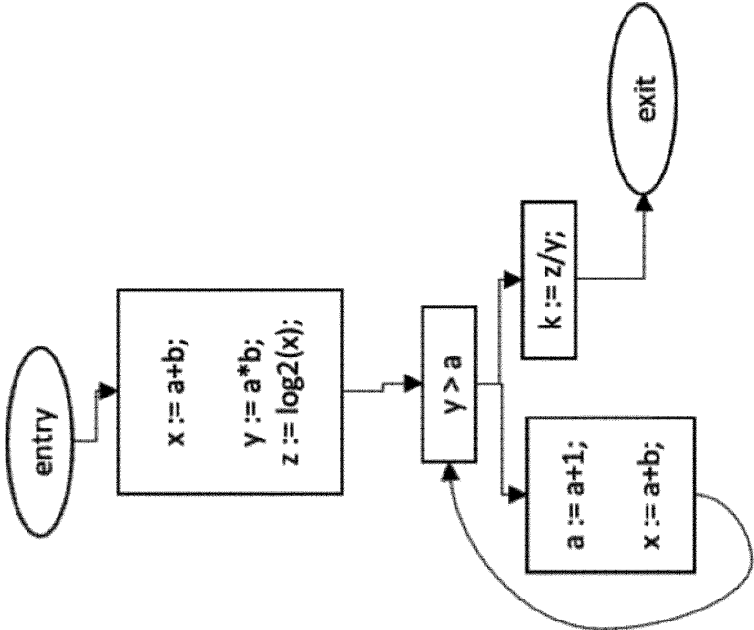
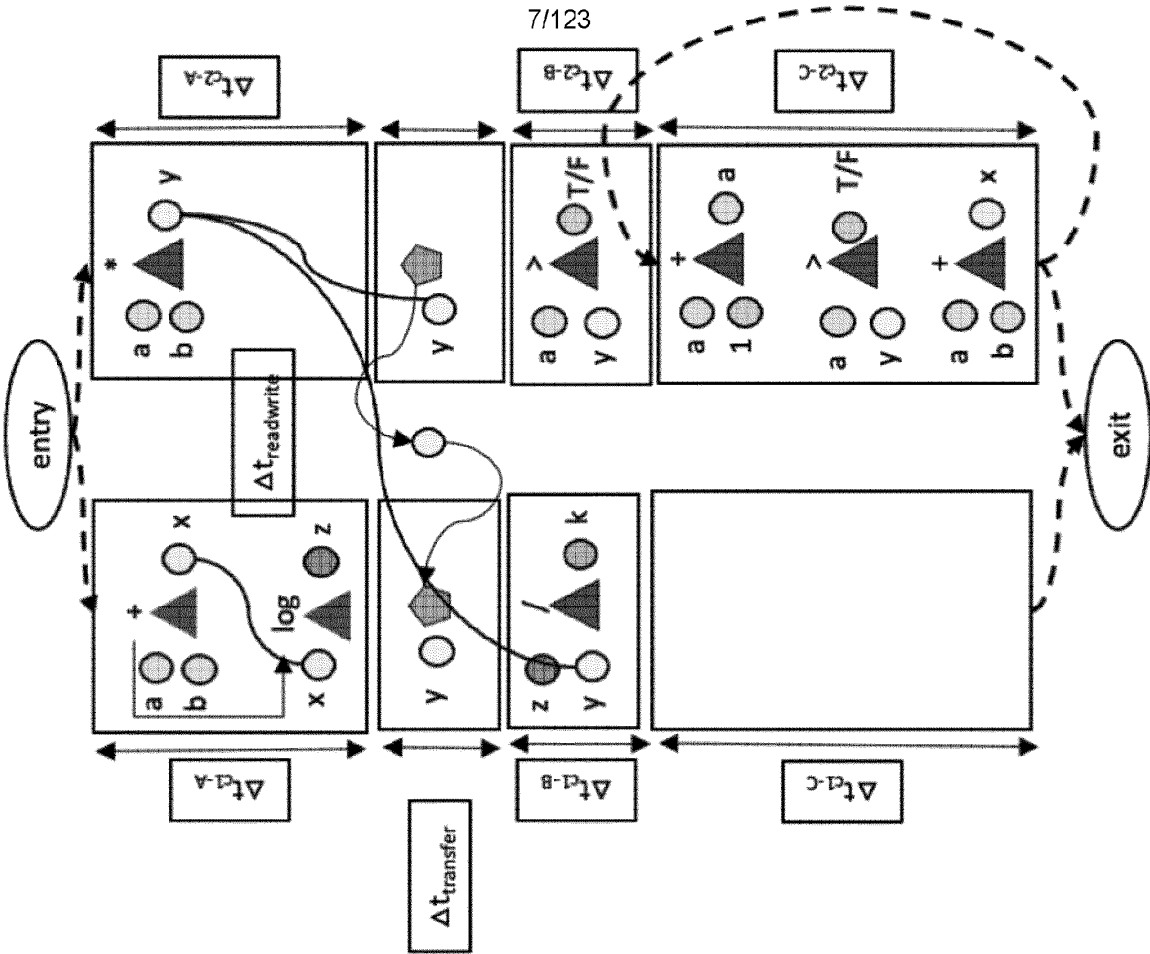


Fig. 7

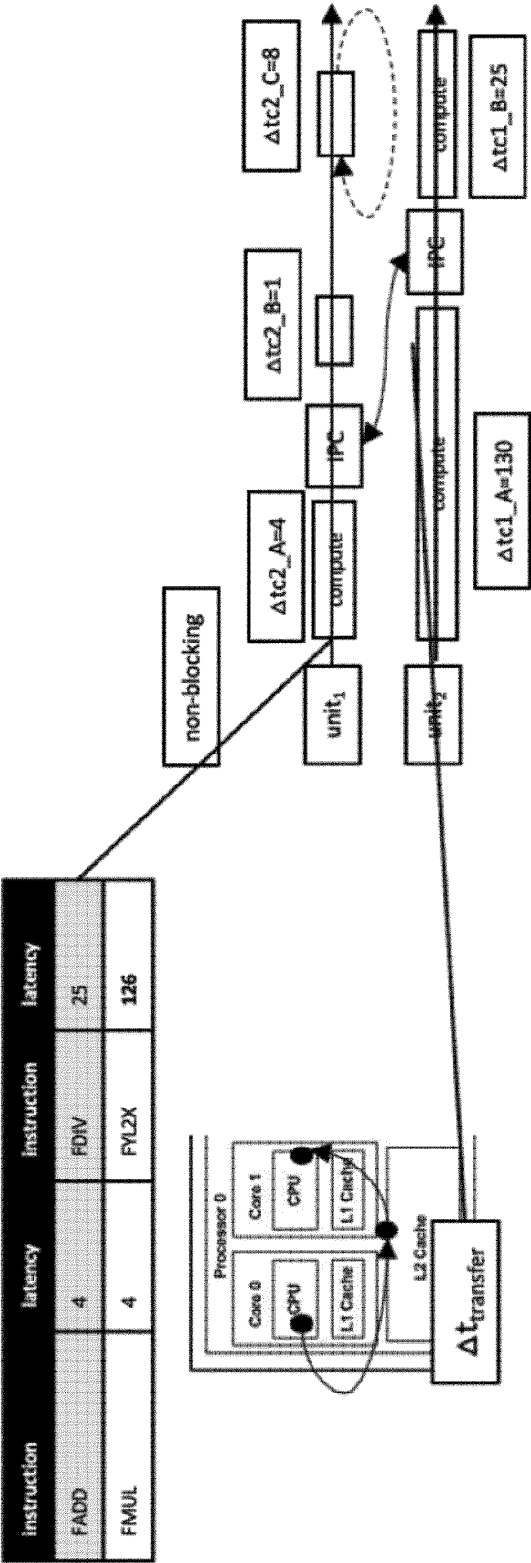


Fig. 8

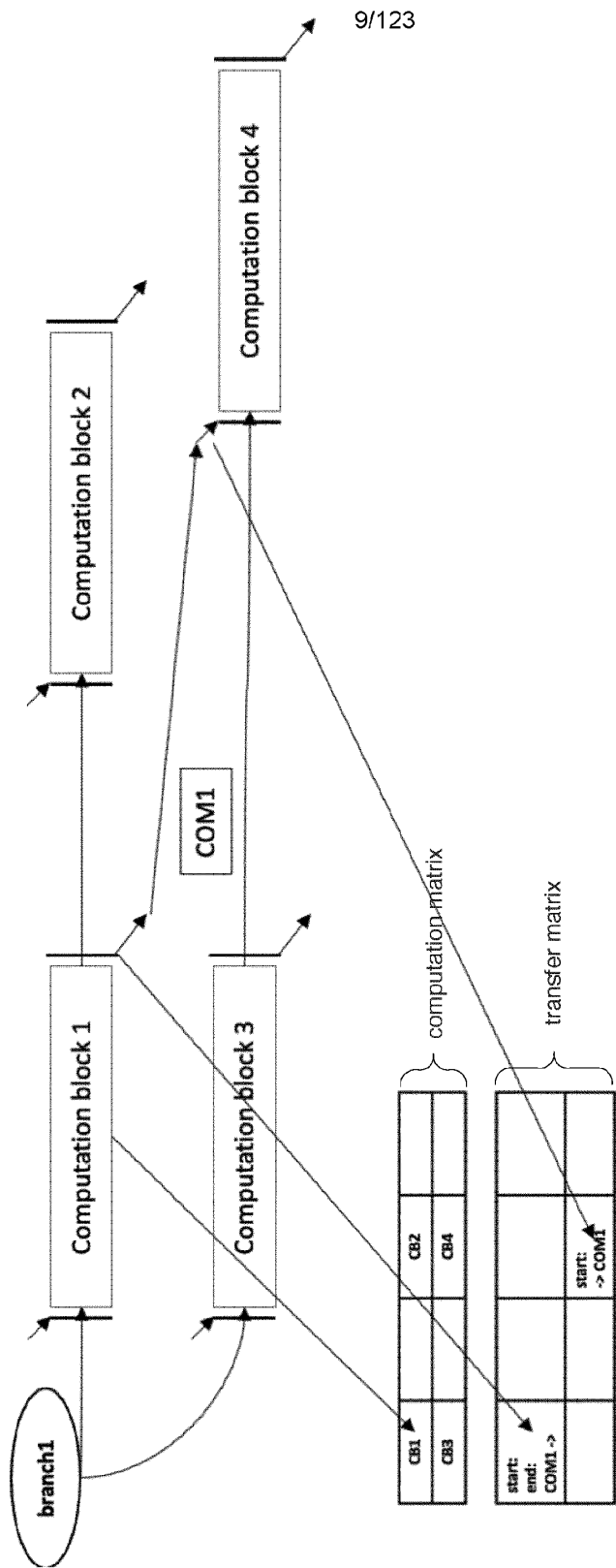


Fig. 9

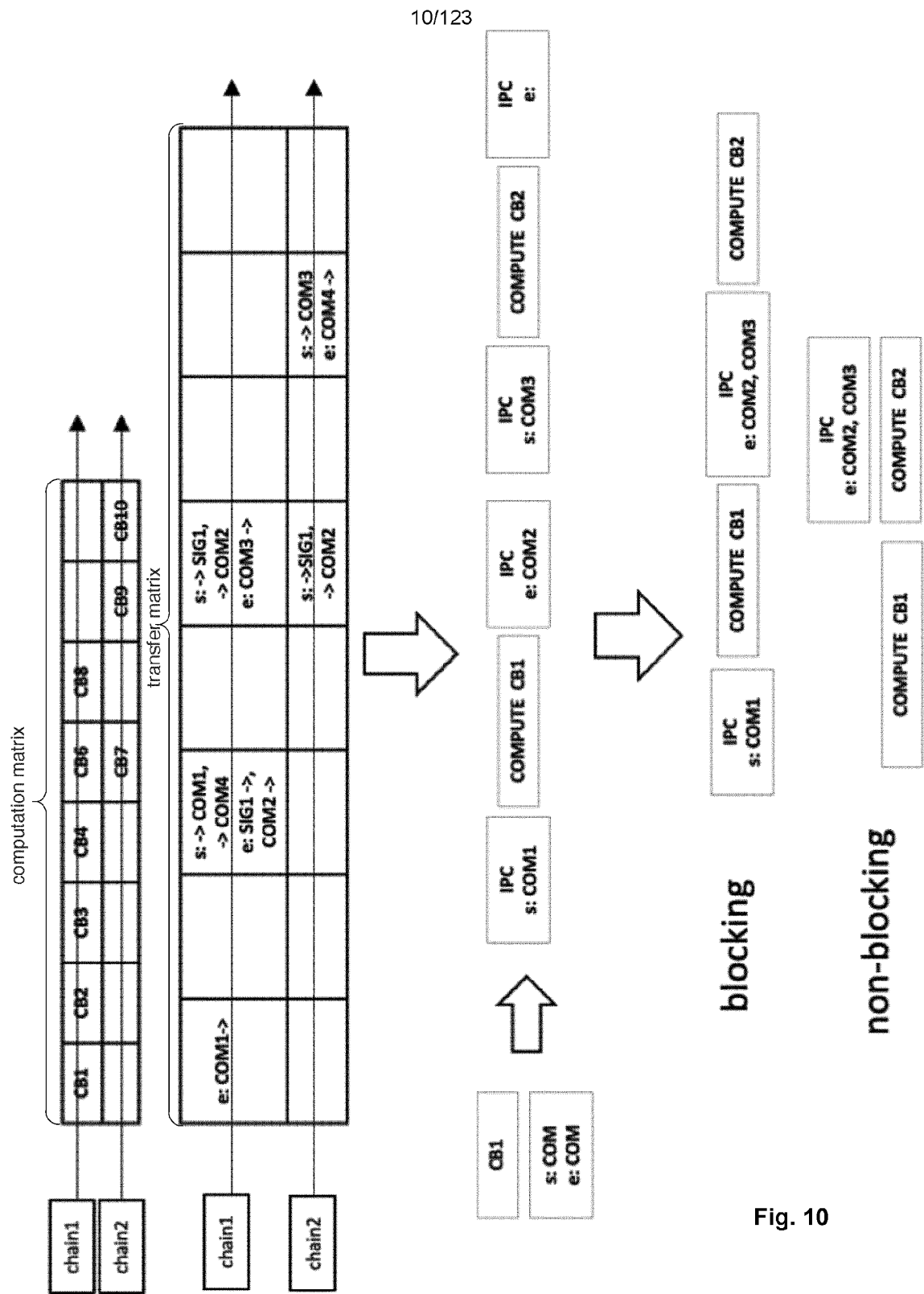


Fig. 10

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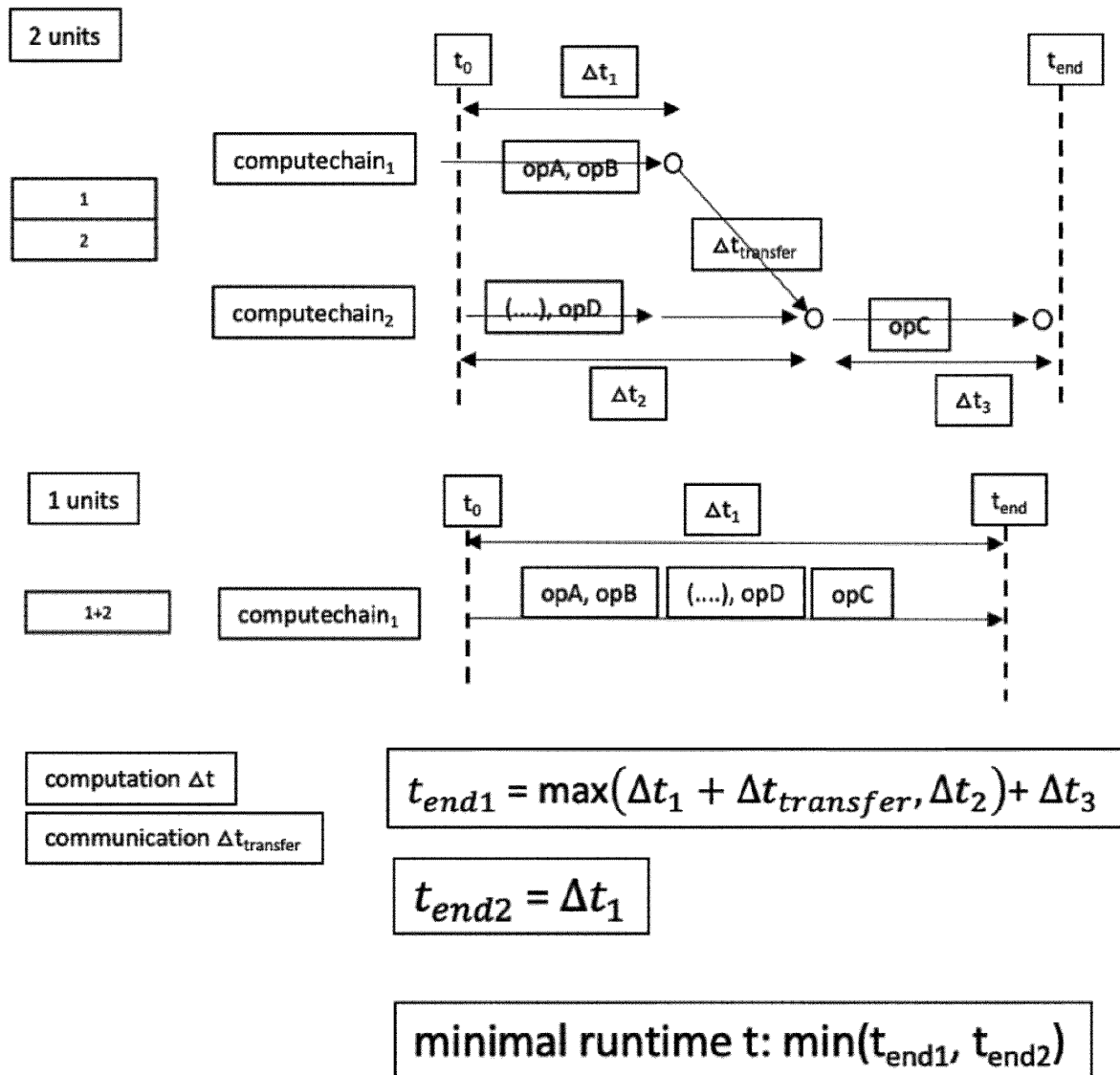


Fig. 11

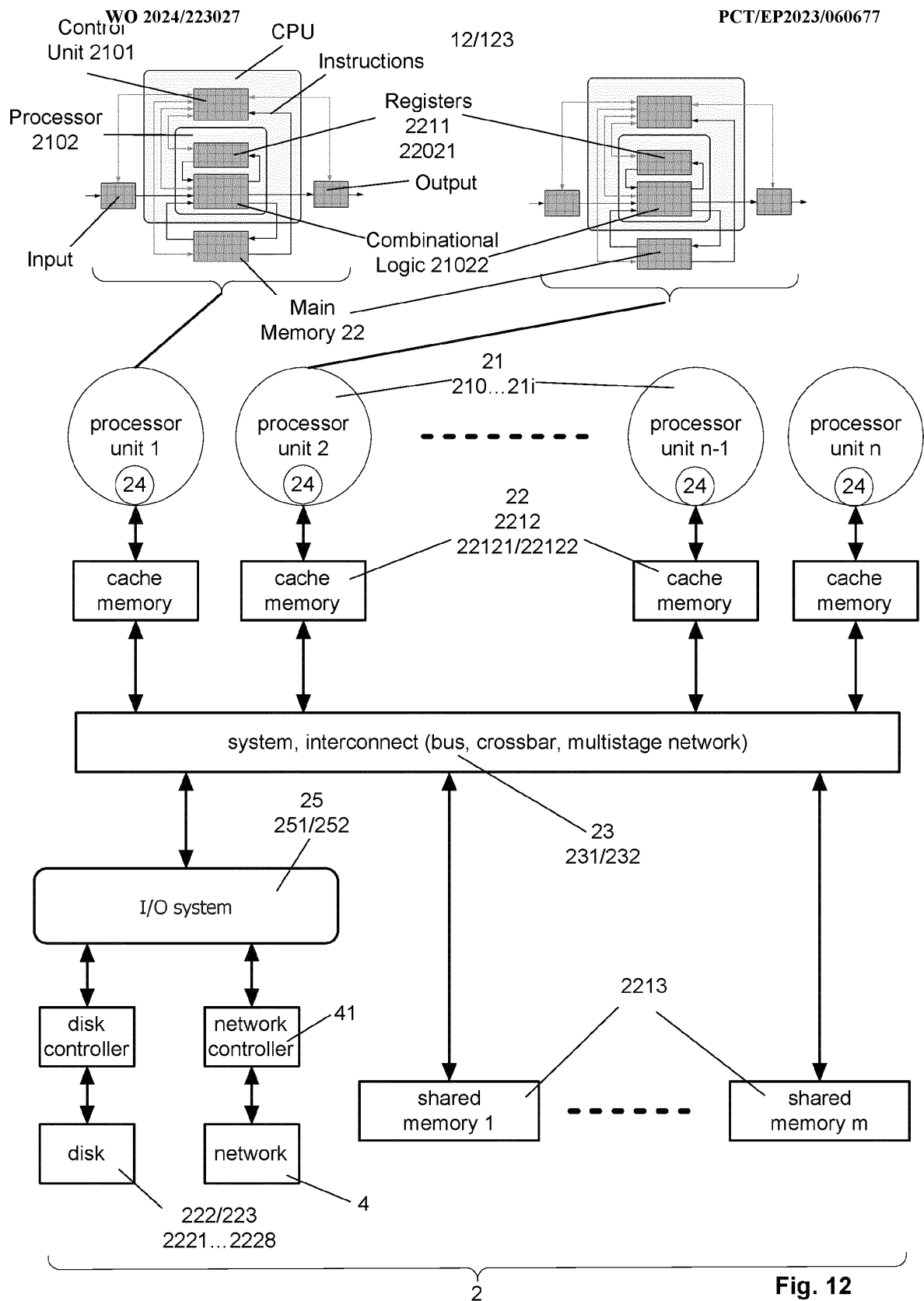


Fig. 12

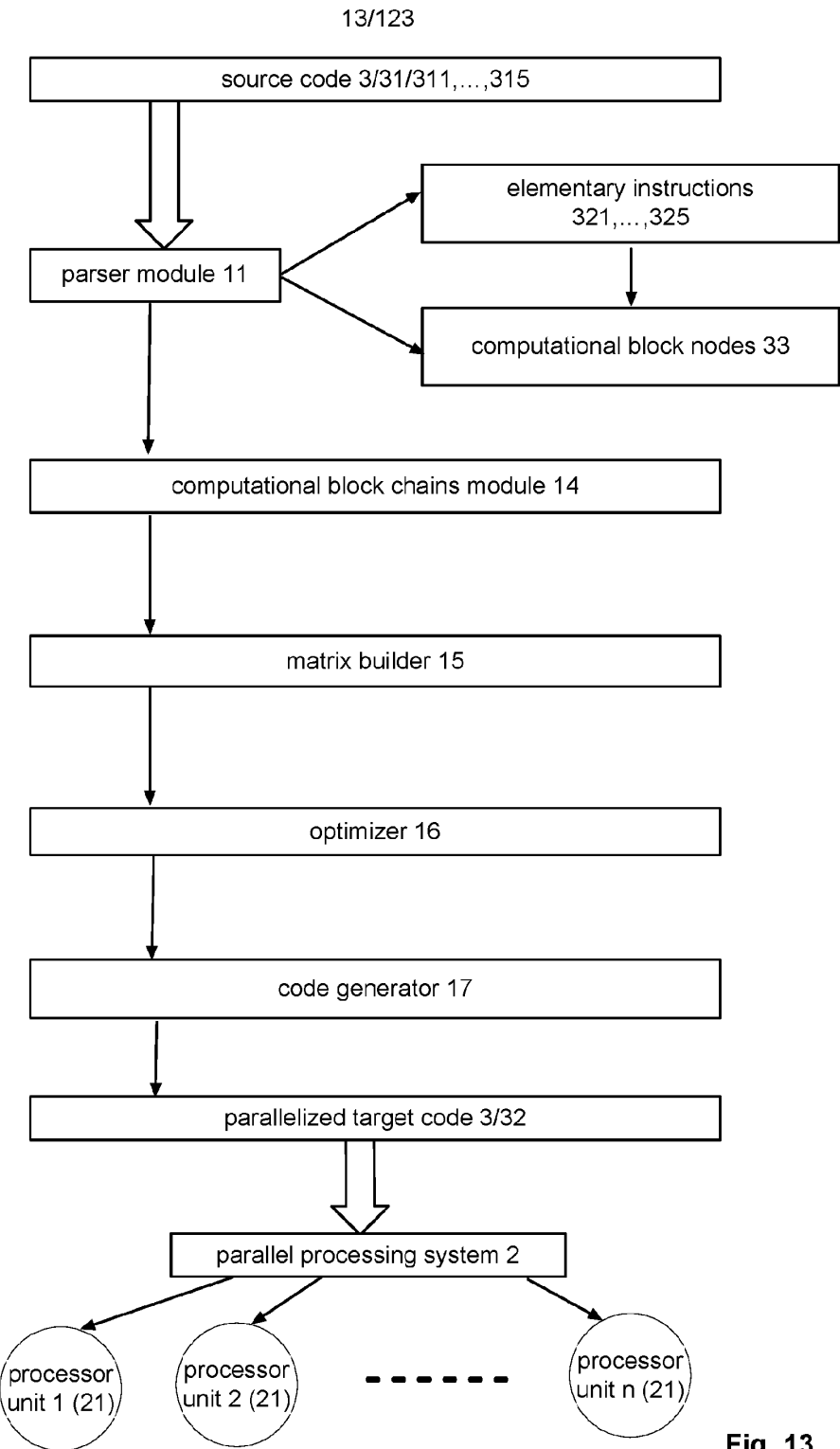


Fig. 13

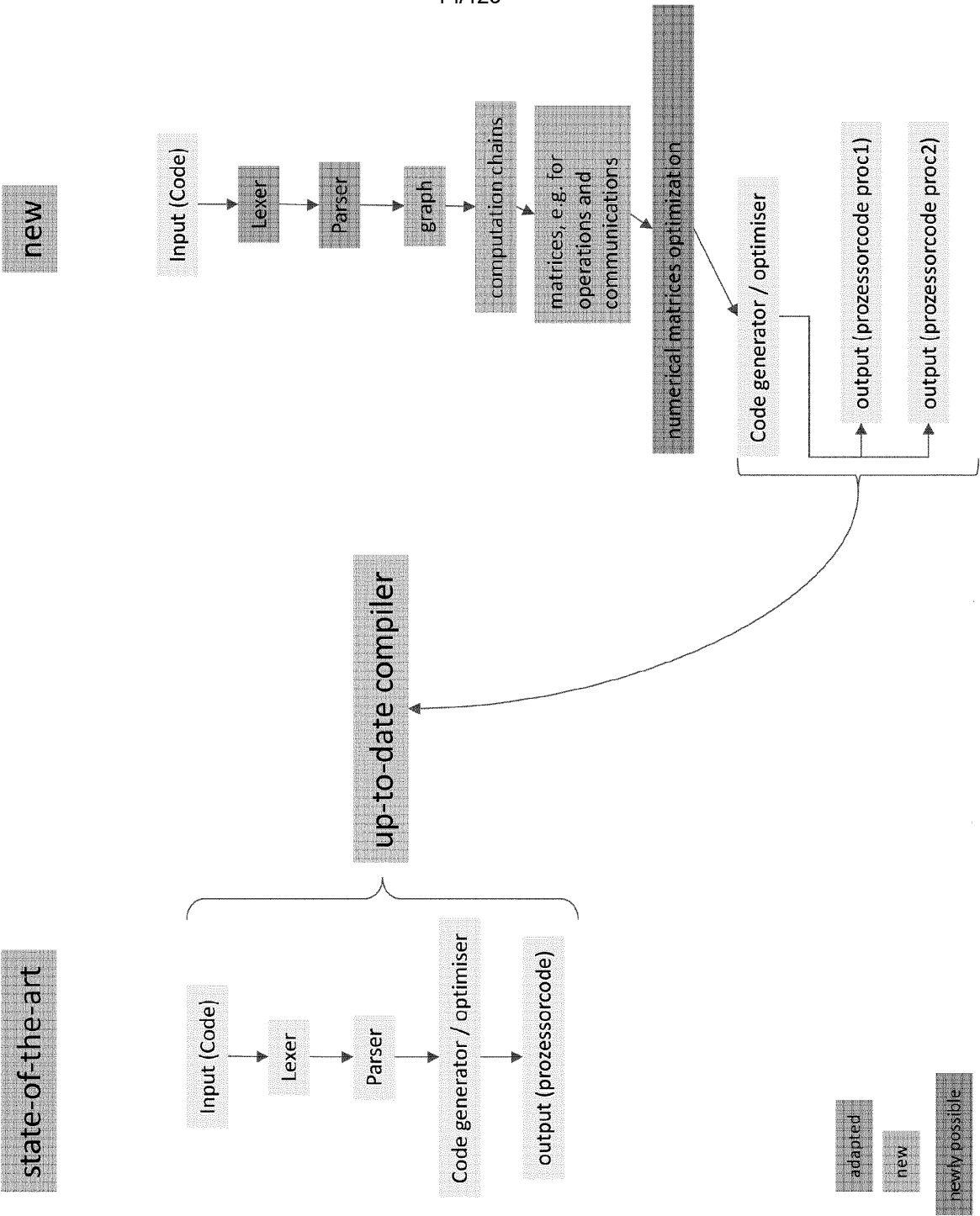


Fig. 14

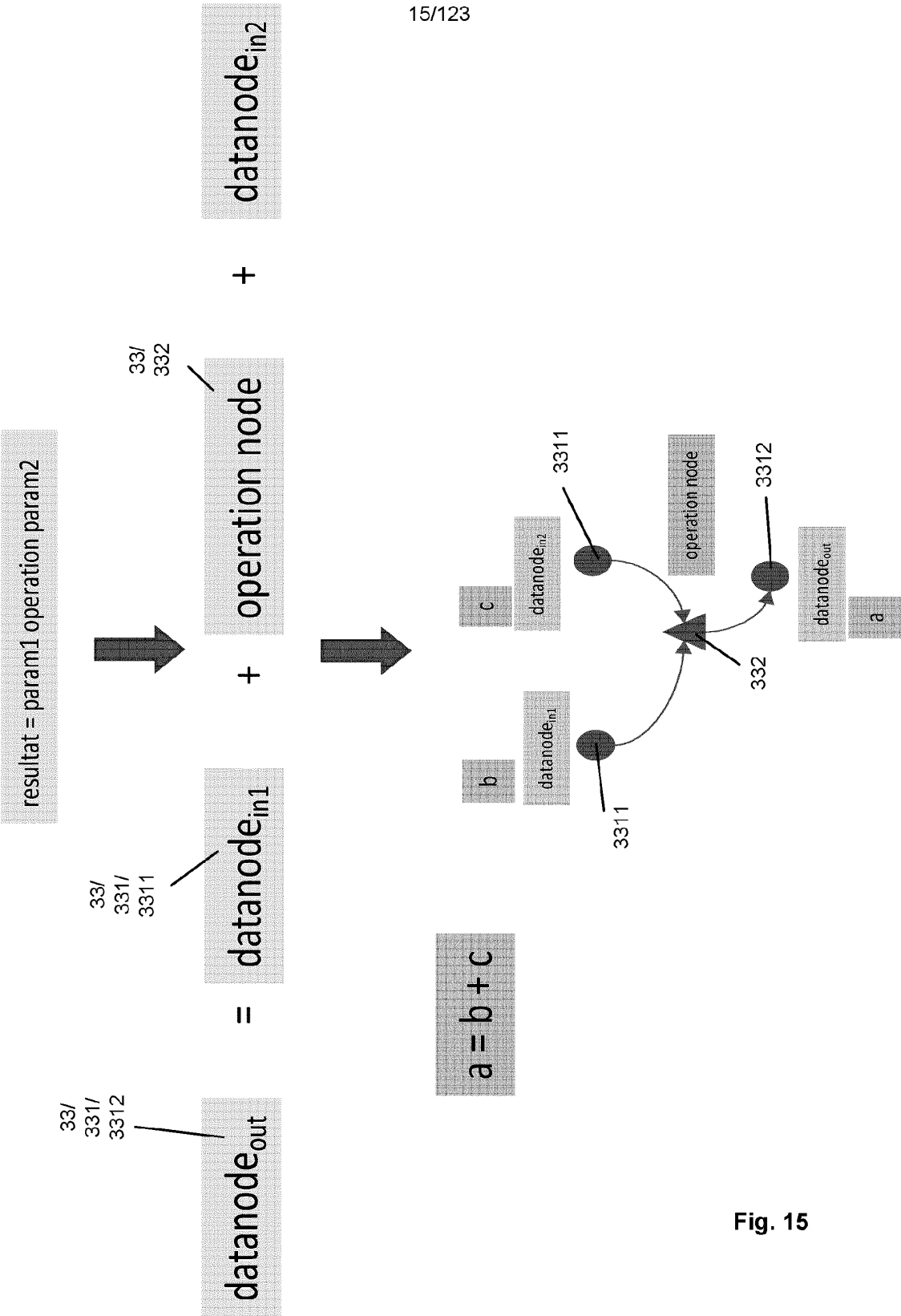


Fig. 15

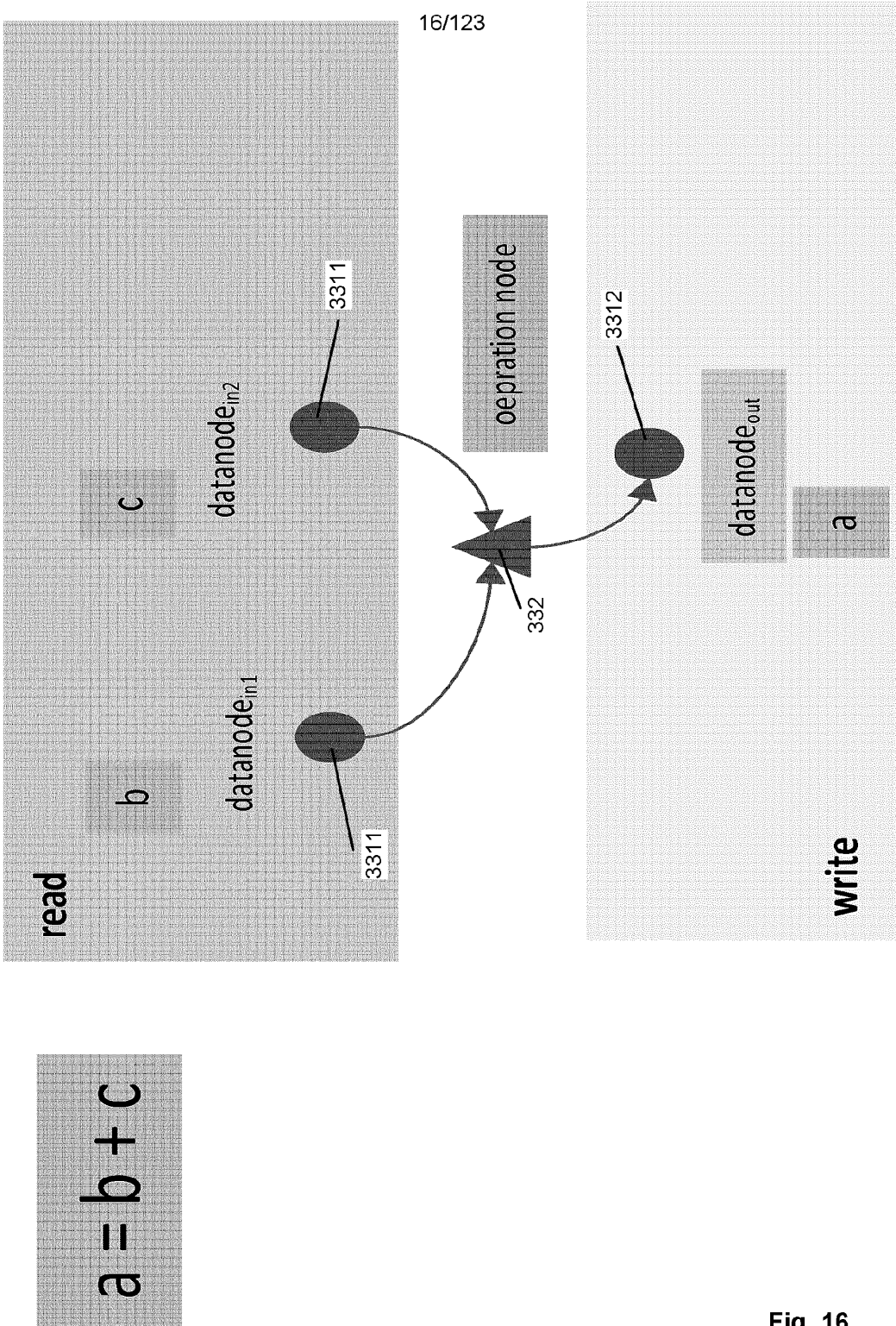


Fig. 16

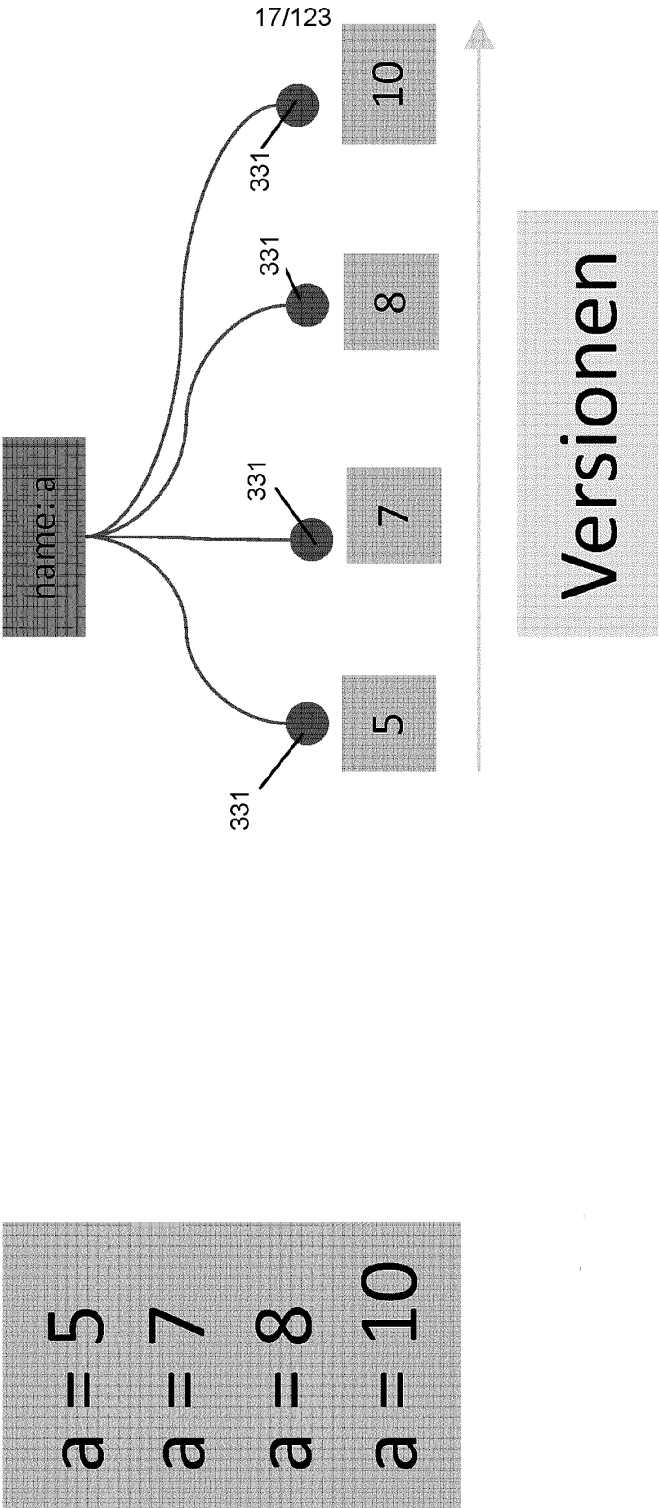


Fig. 17

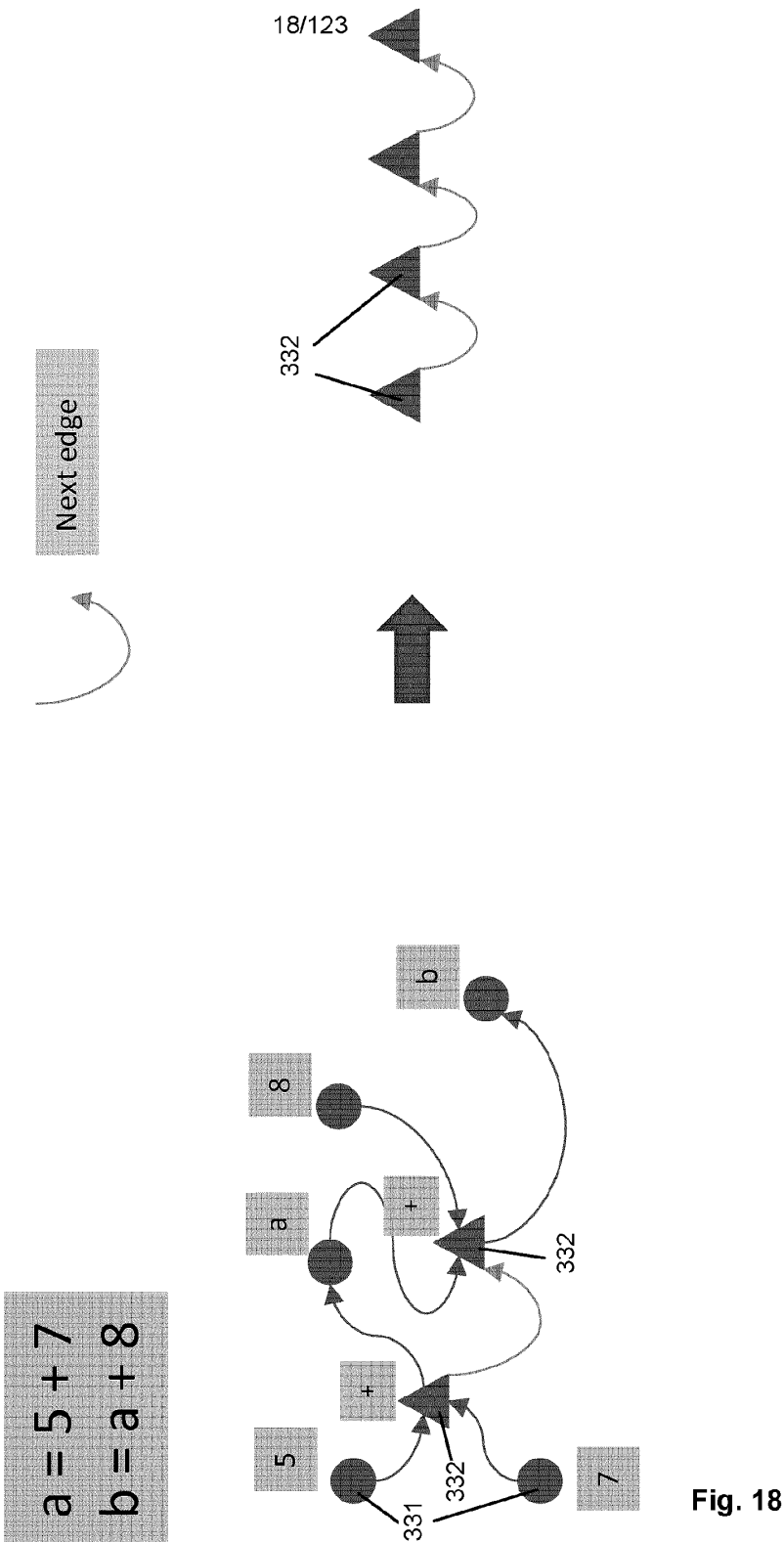


Fig. 18

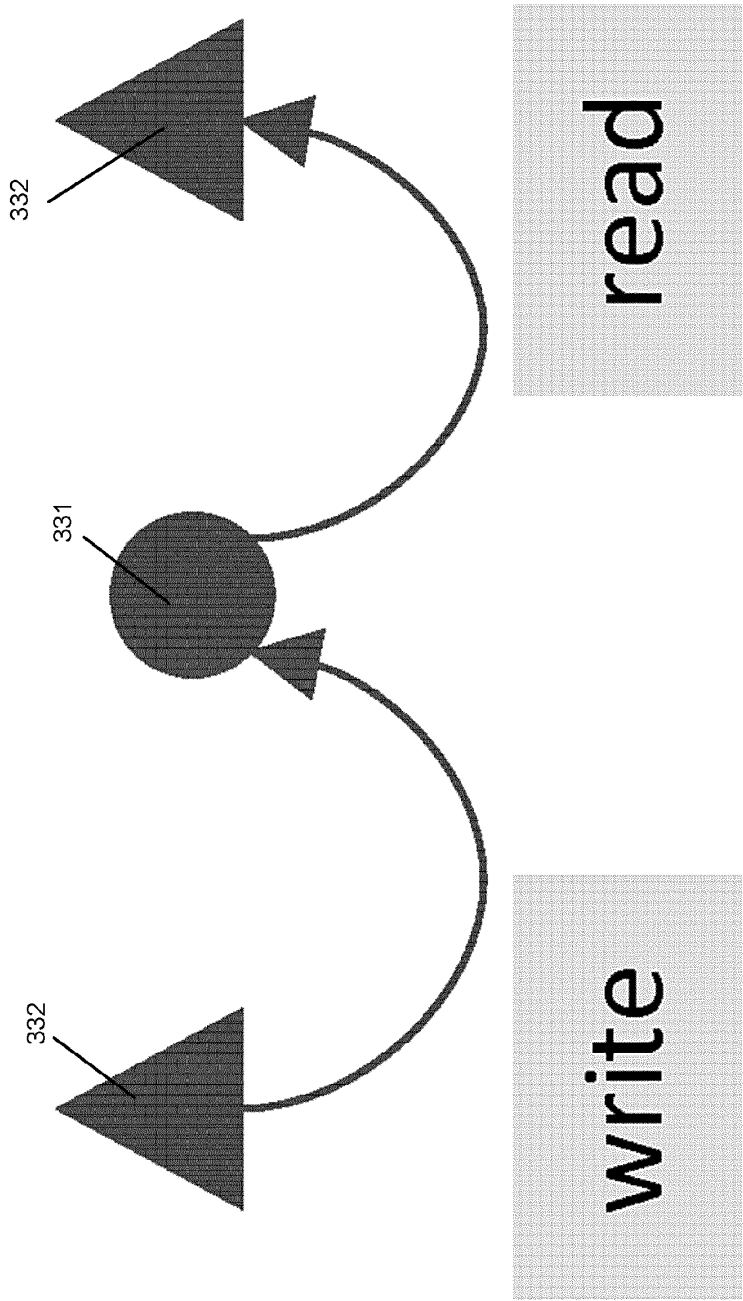
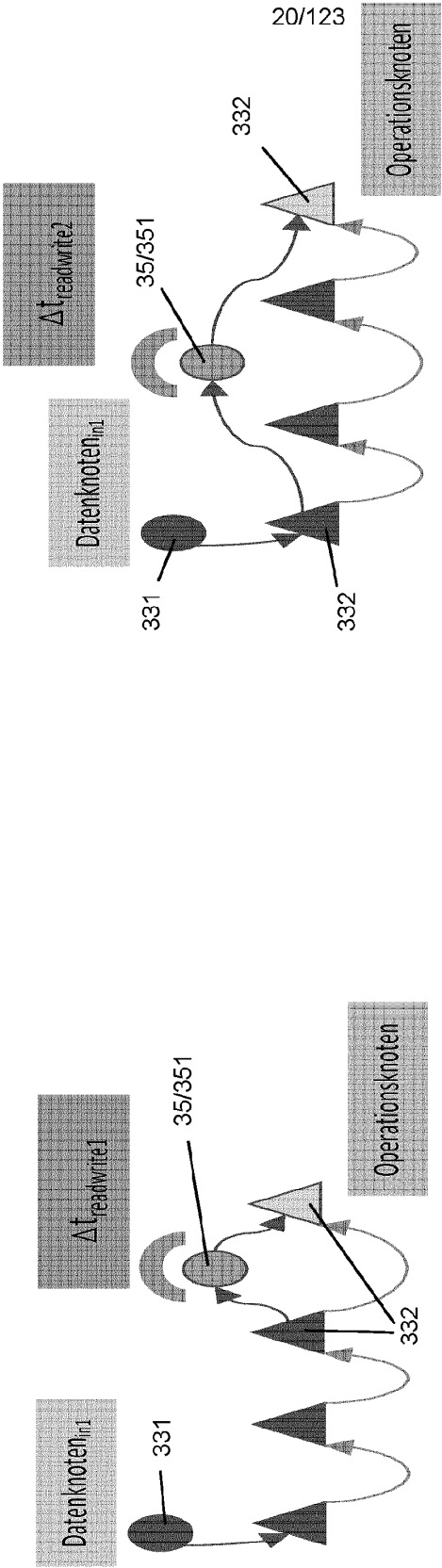


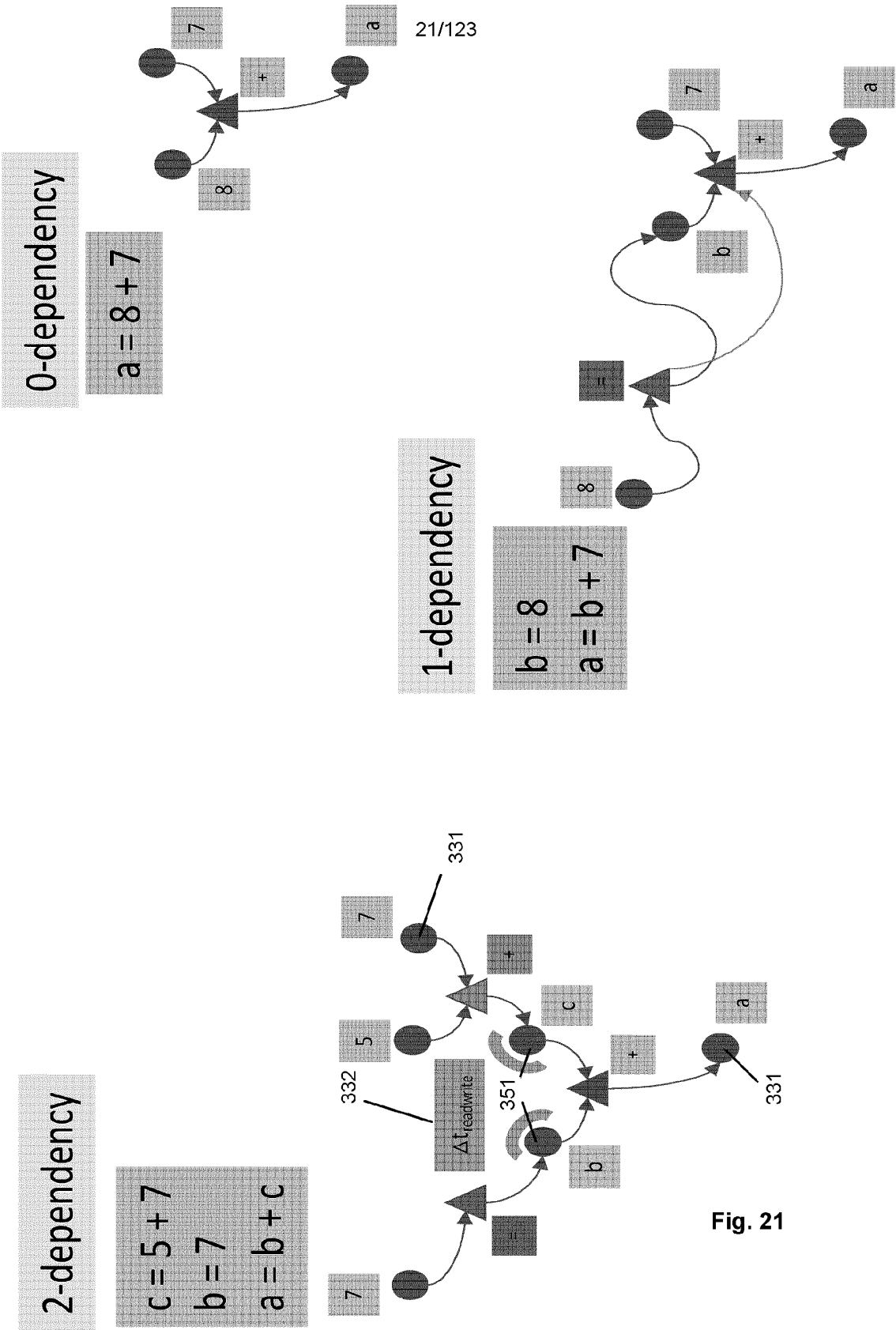
Fig. 19



$\Delta t_{readwrite}$ as a indicator what can be done with this data node

- $\Delta t_{readwrite}$ sehr klein: same cache_line or nearby
- $\Delta t_{readwrite}$ „mittel gross“: on same #cpu unit, use prefetch
- $\Delta t_{readwrite}$ „genug gross“: possible to transfer over network

Fig. 20



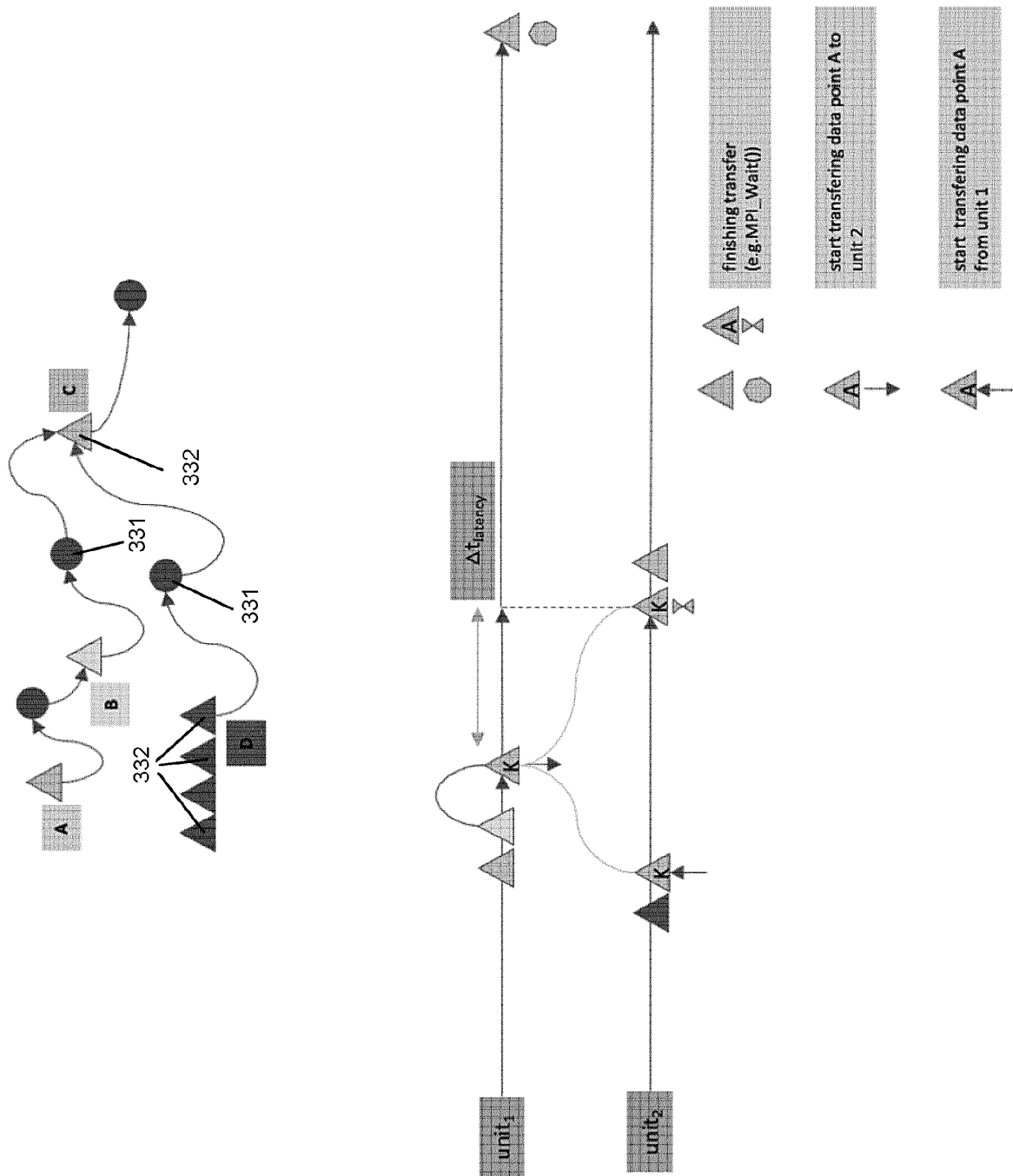


Fig. 22

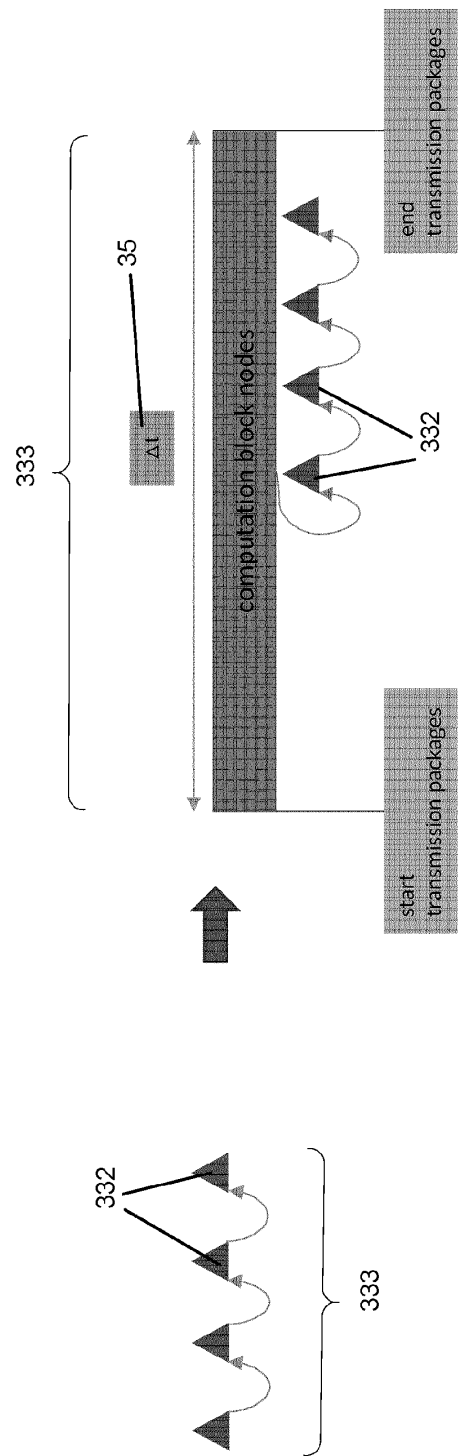


Fig. 23

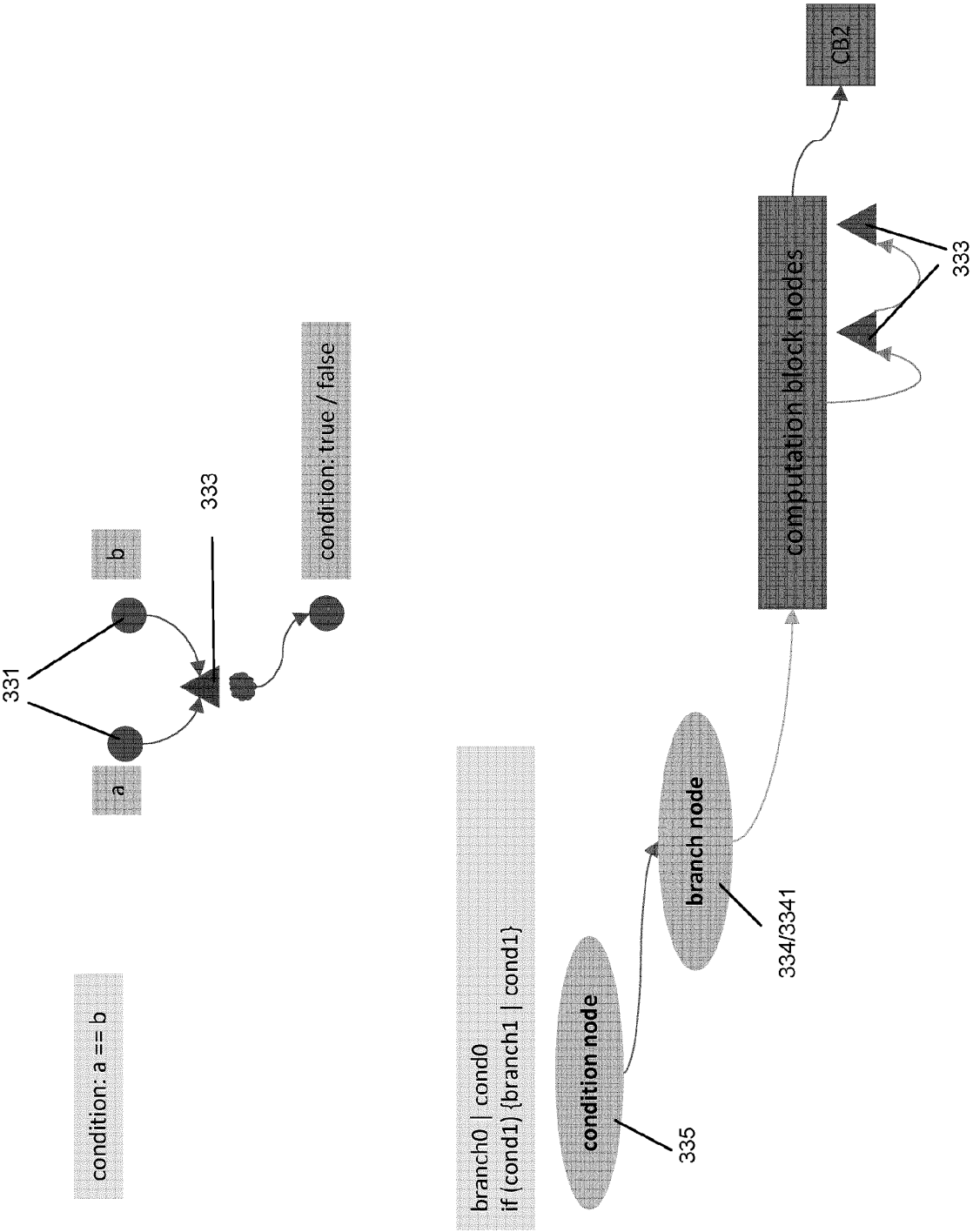


Fig. 24

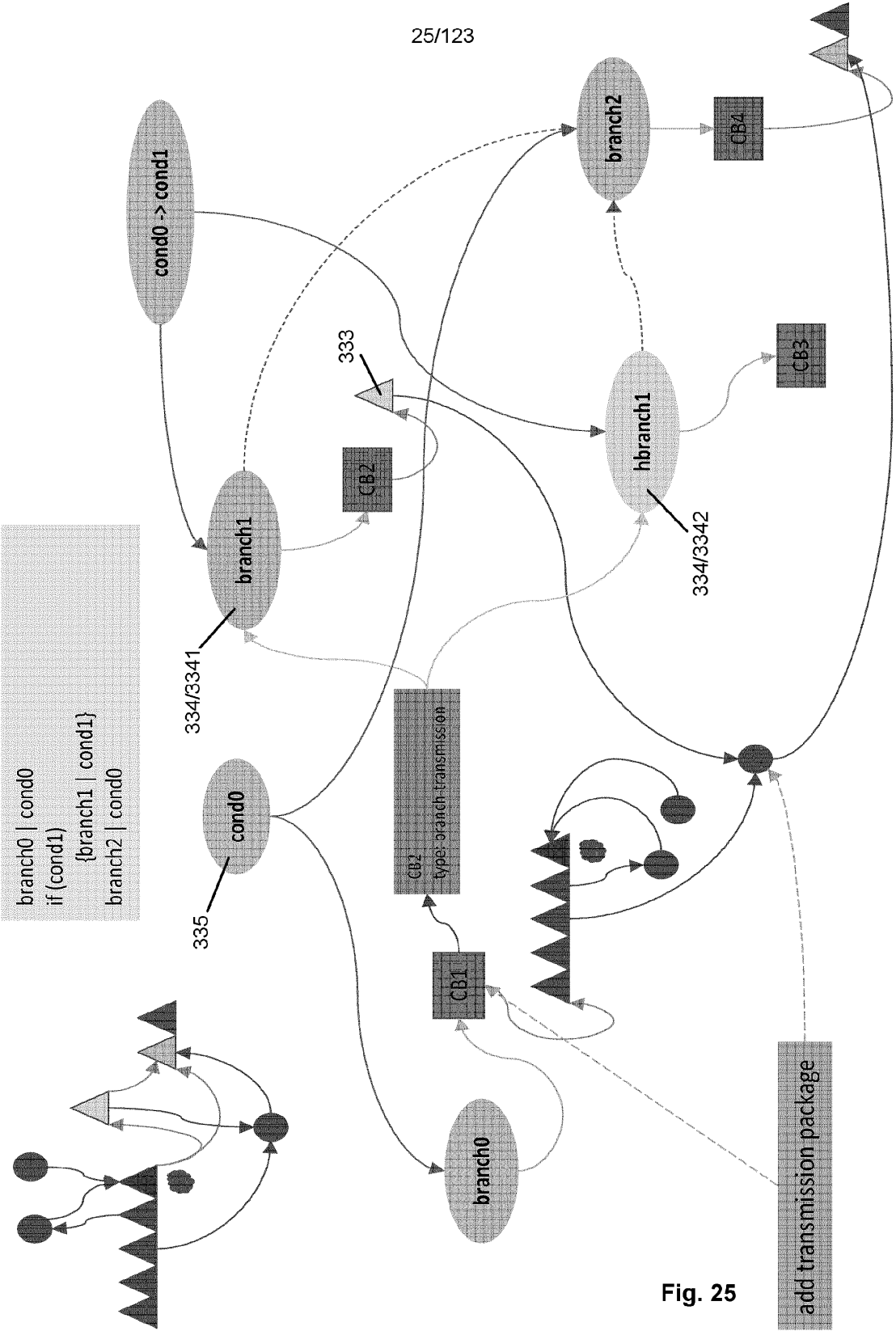


Fig. 25

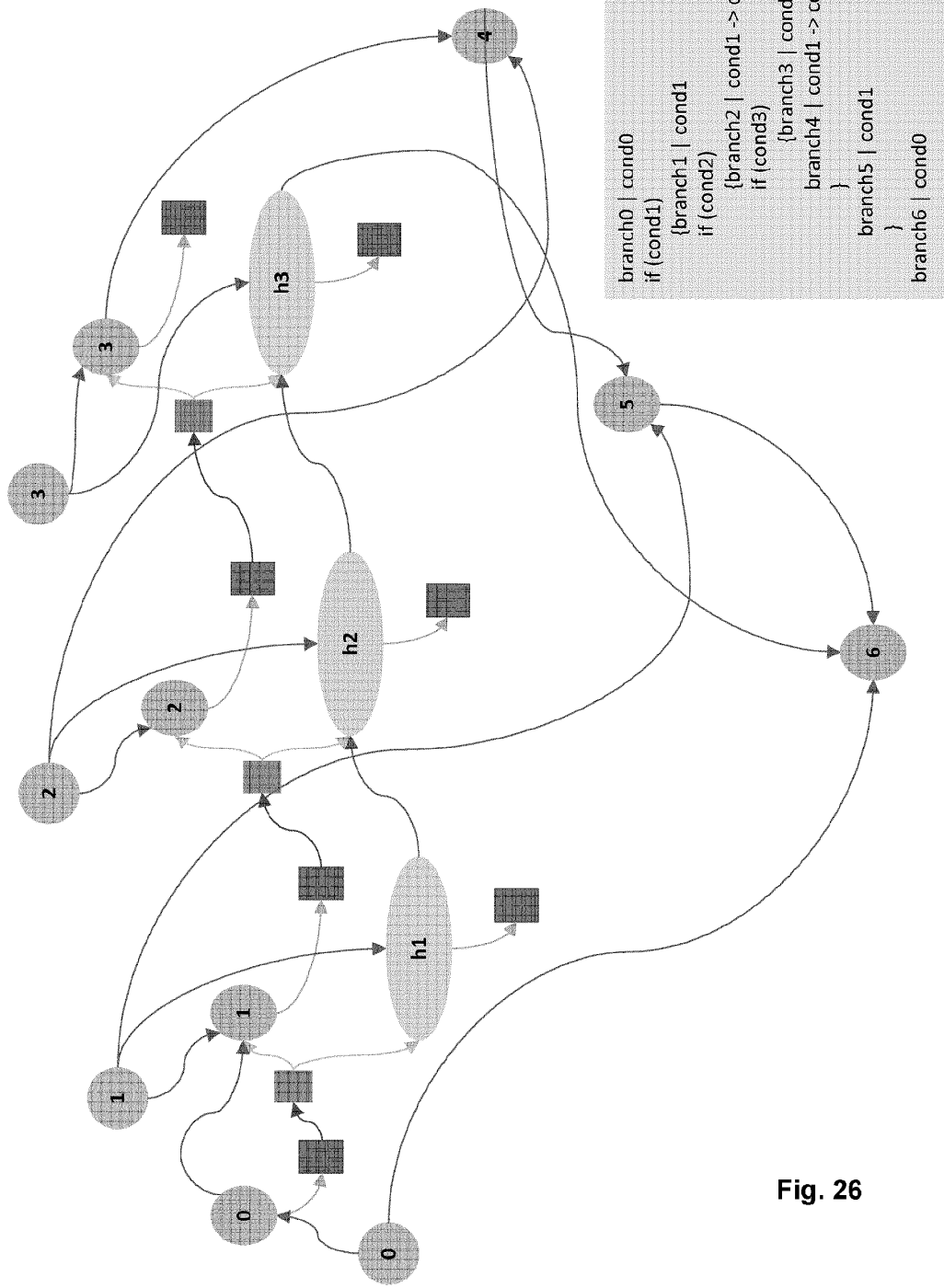


Fig. 26

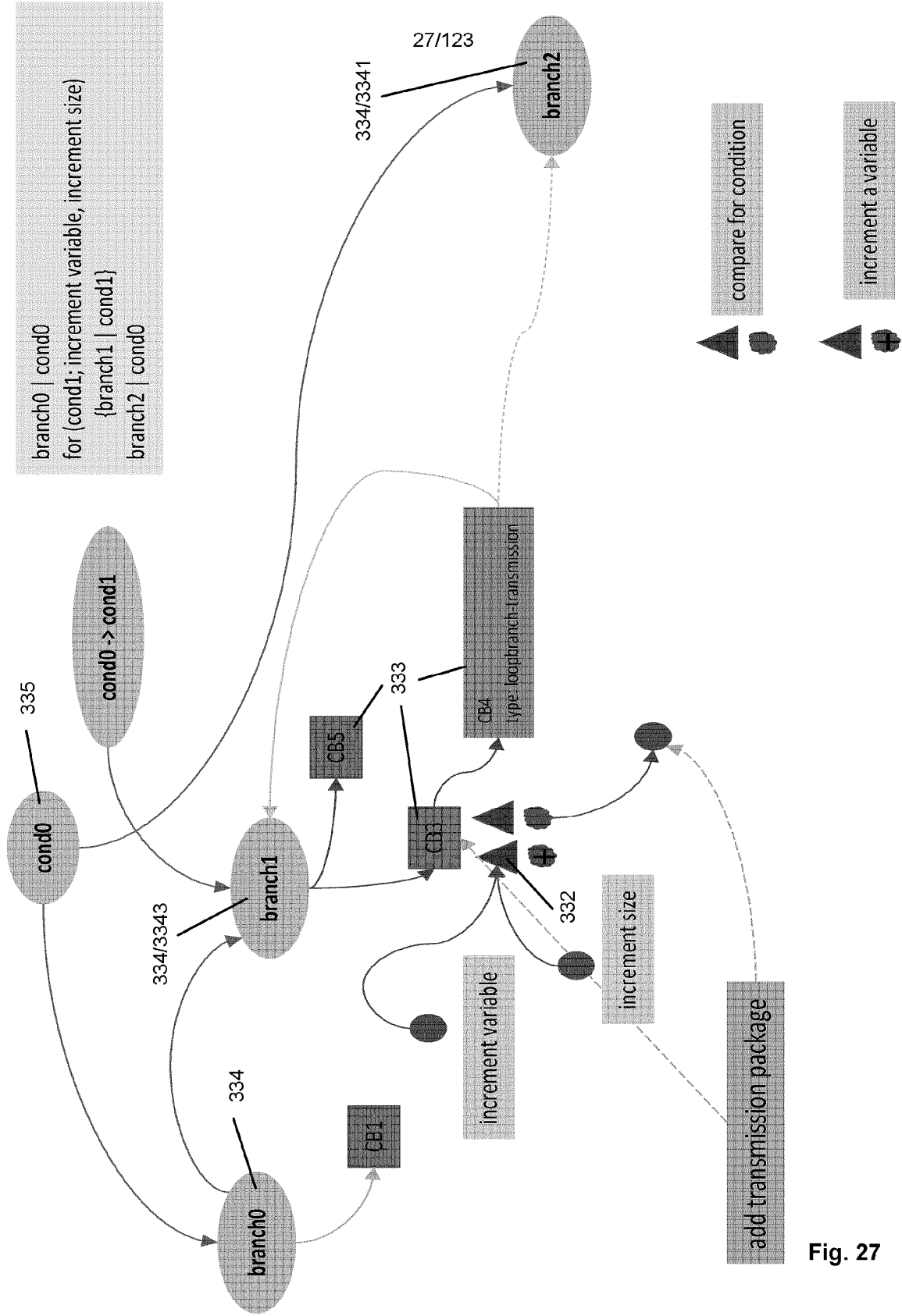


Fig. 27

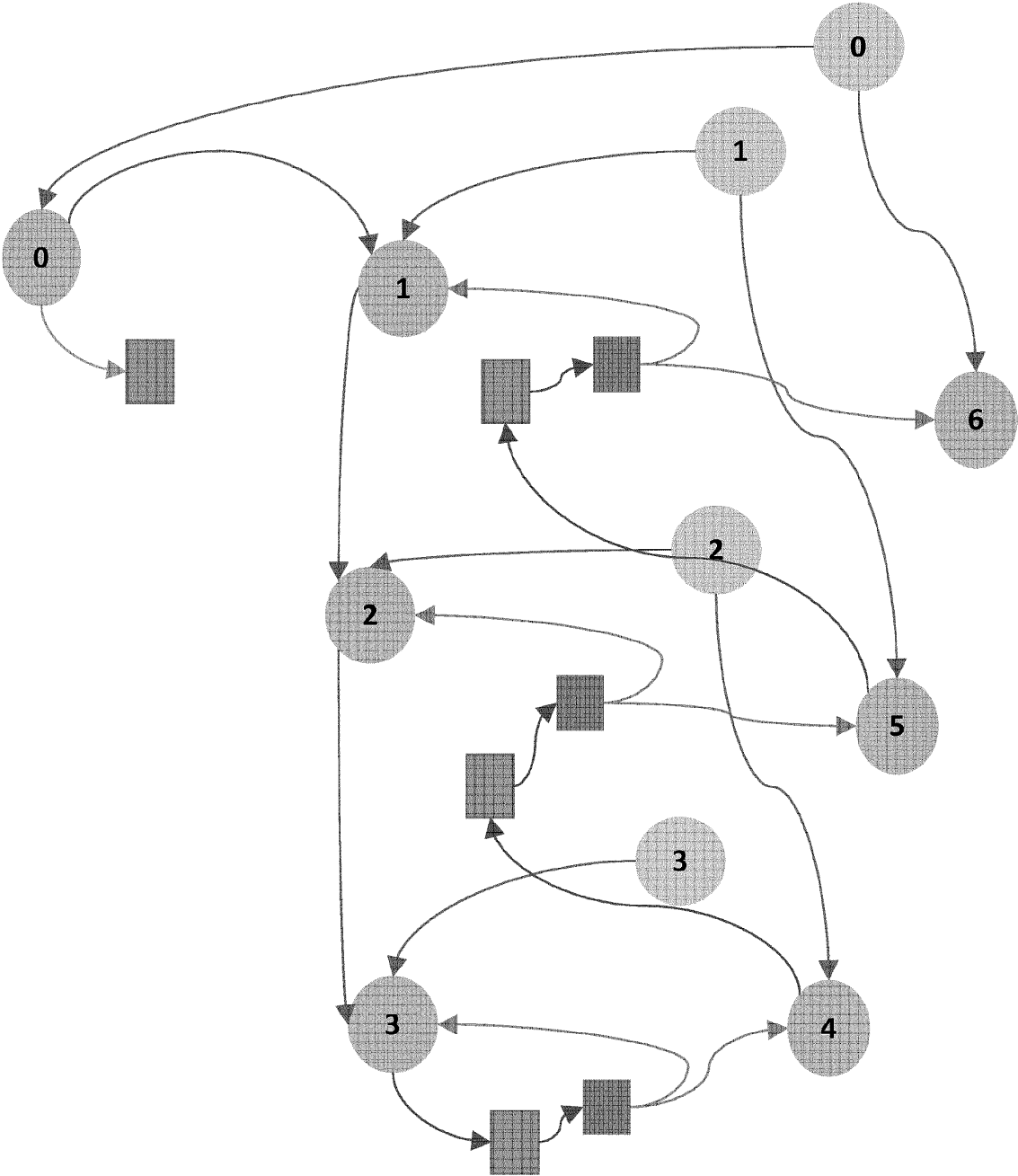
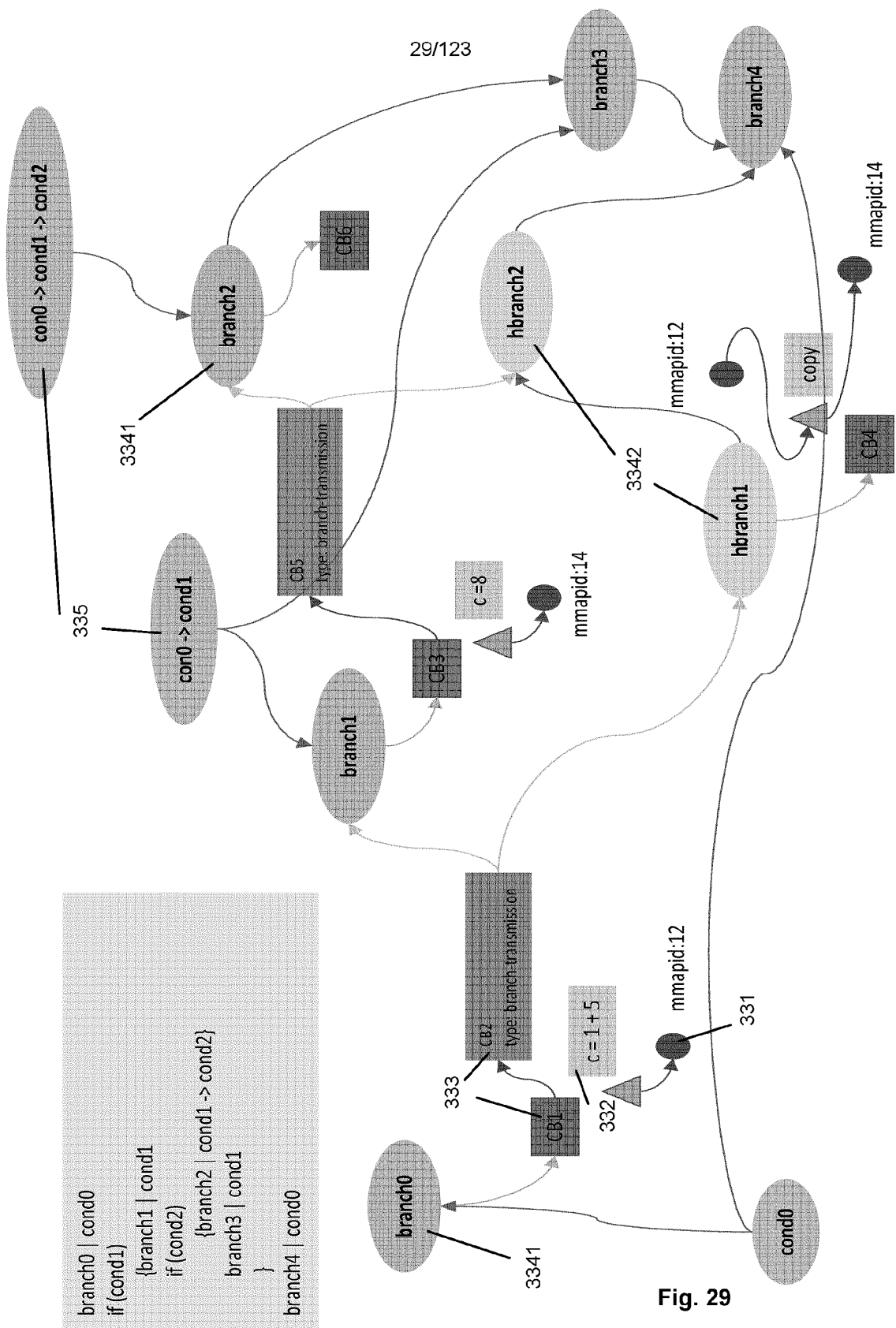


Fig. 28



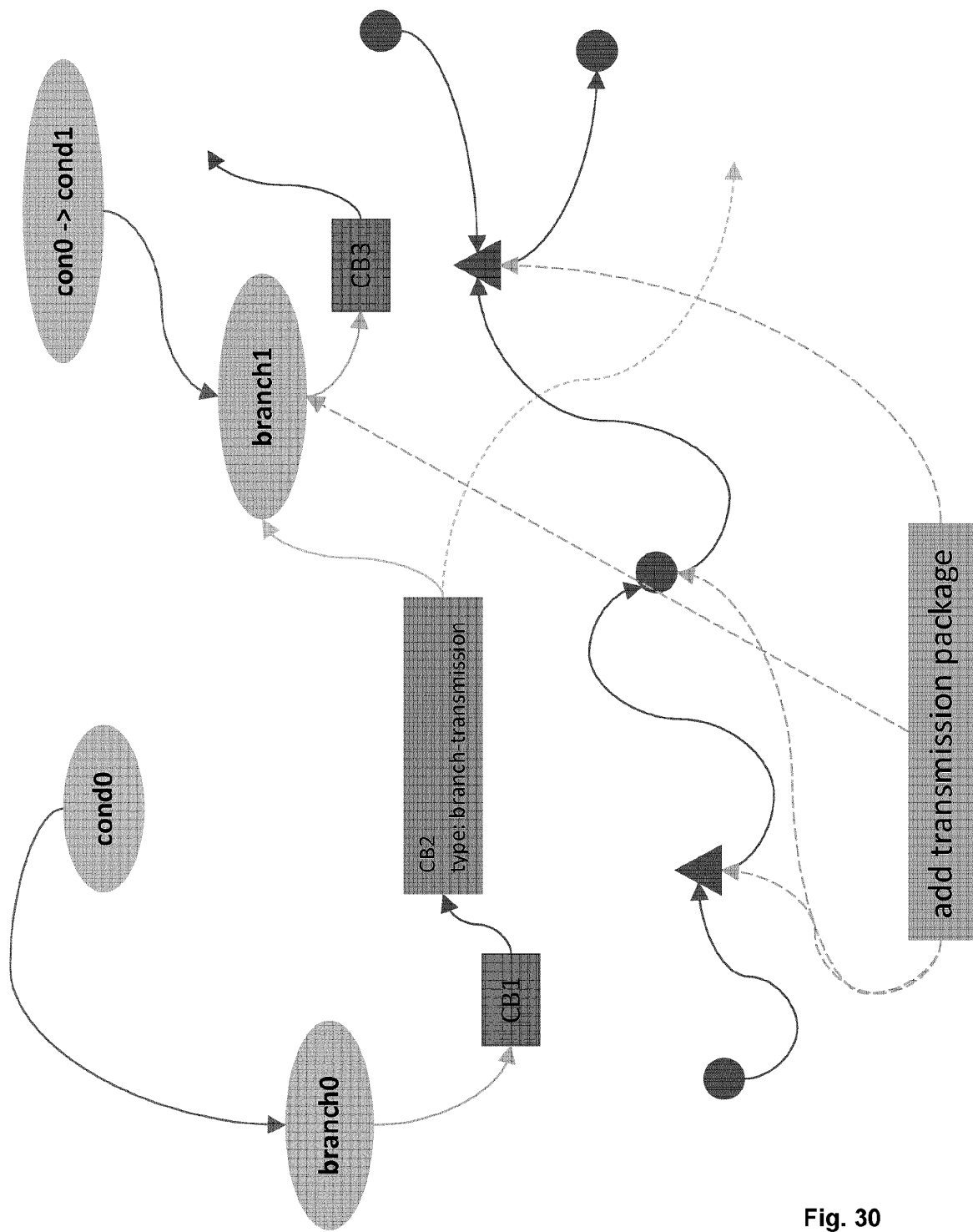


Fig. 30

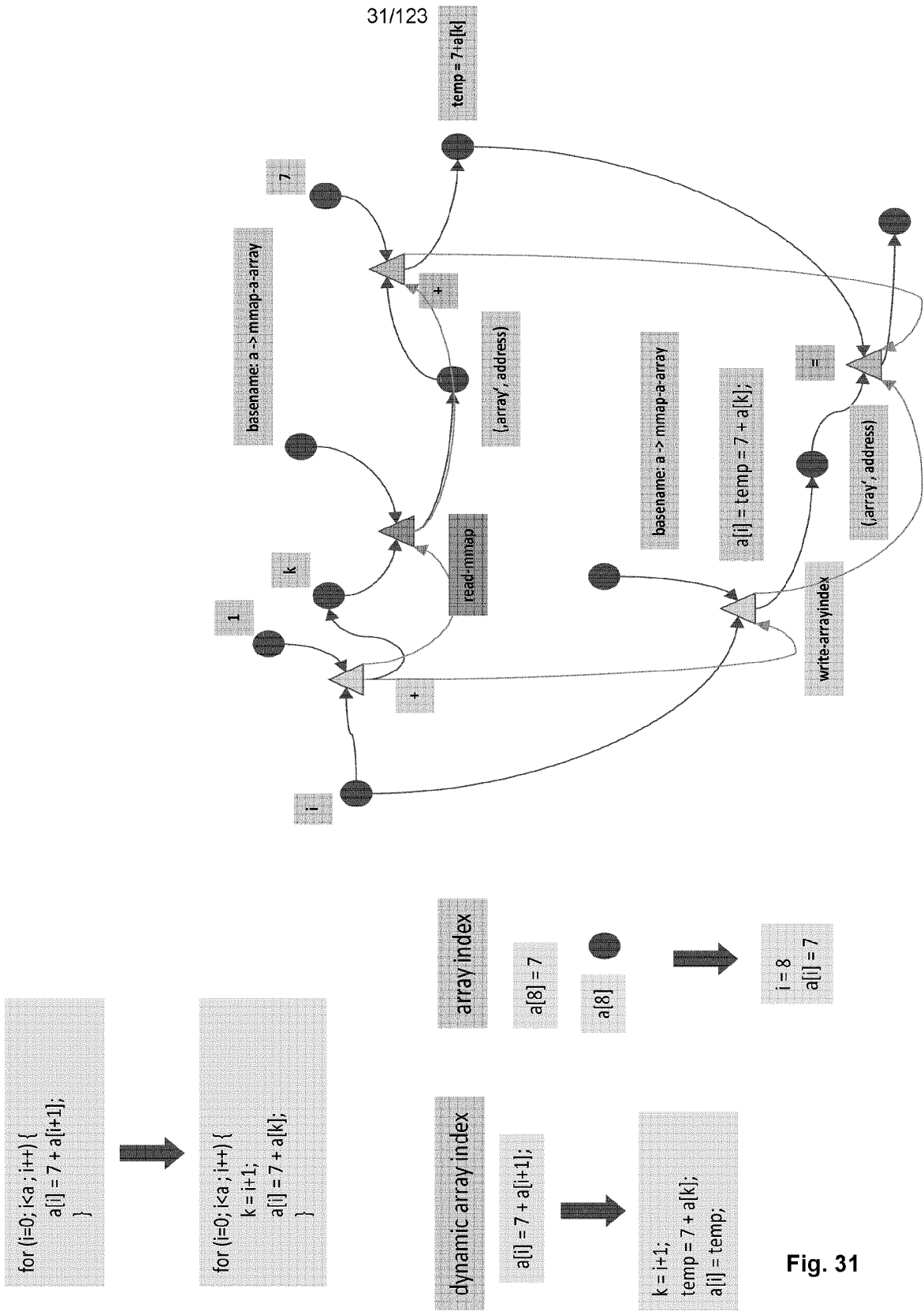


Fig. 31

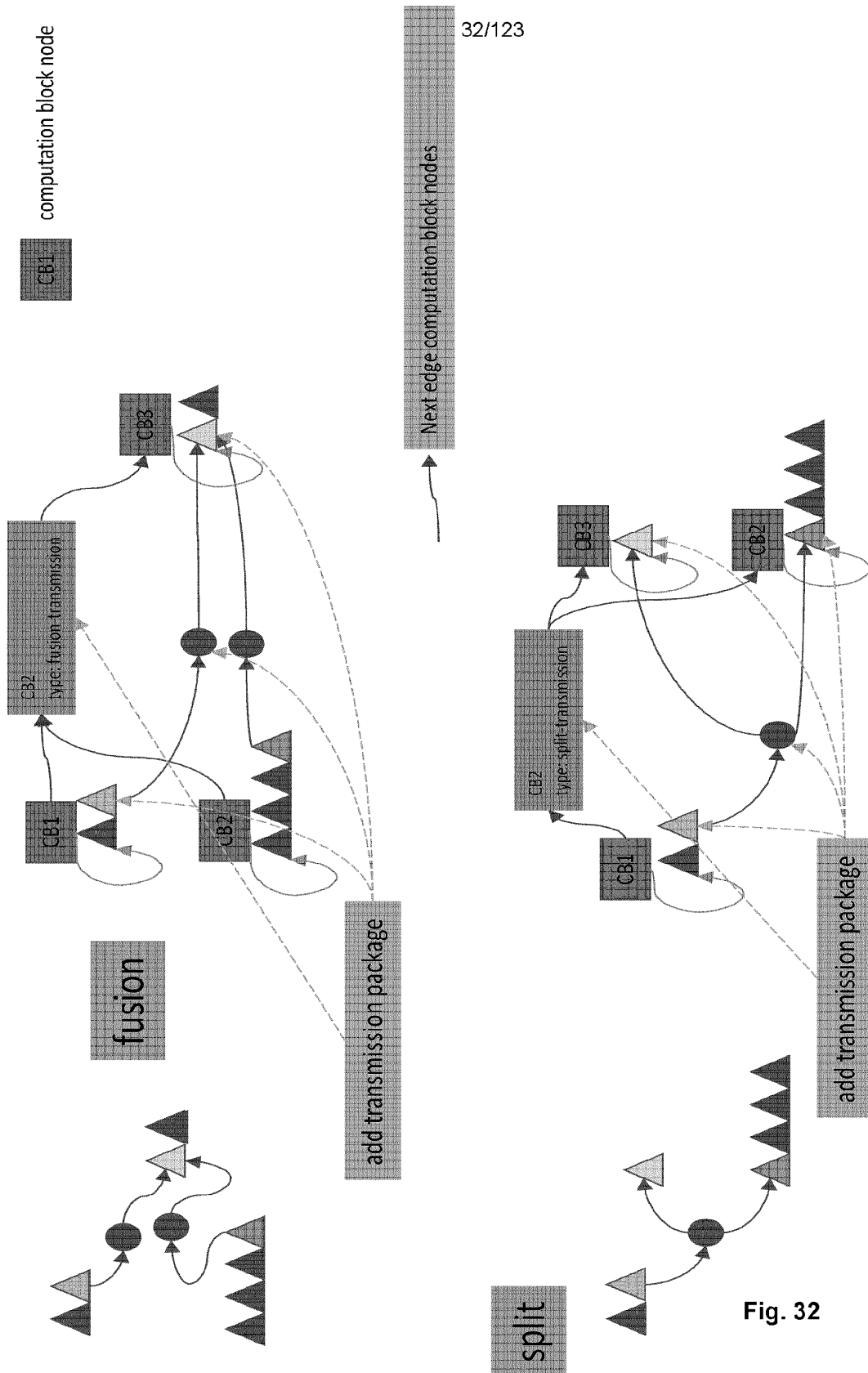


Fig. 32

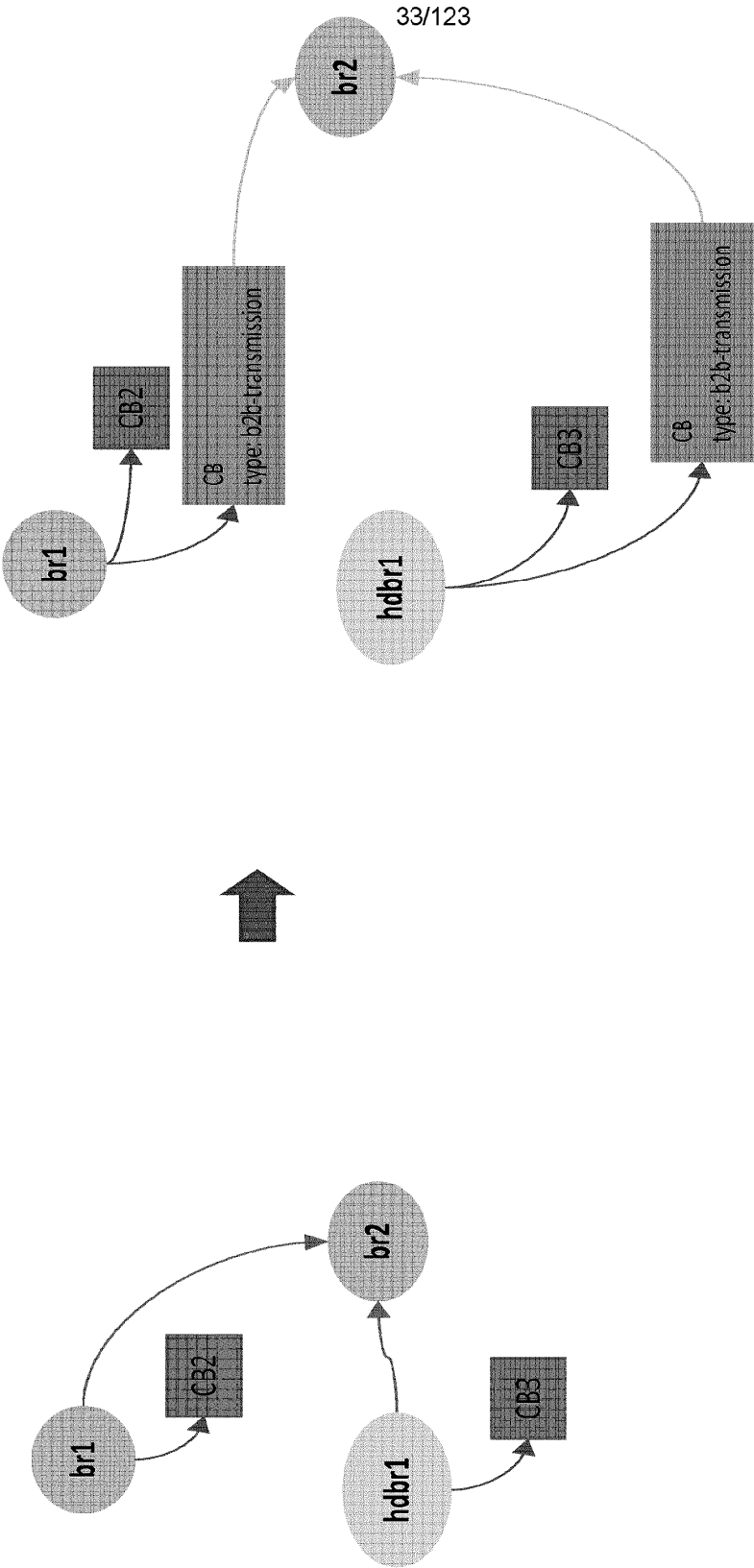


Fig. 33

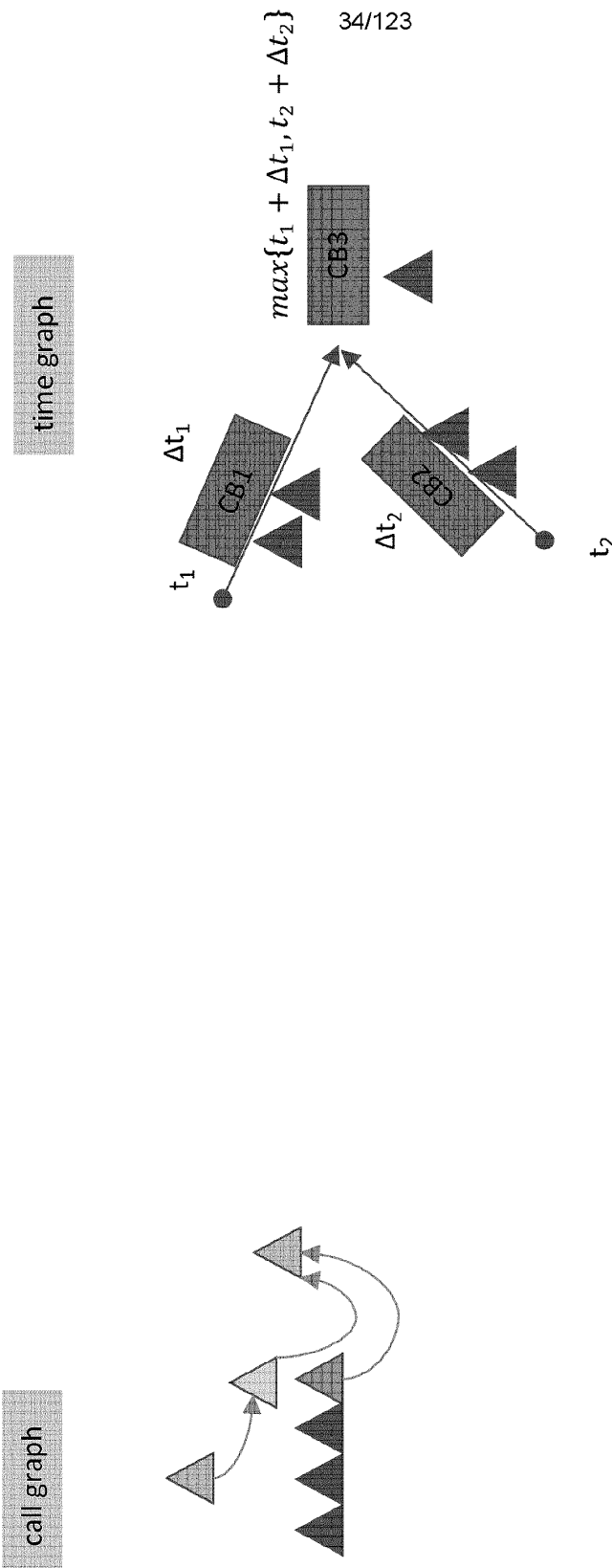
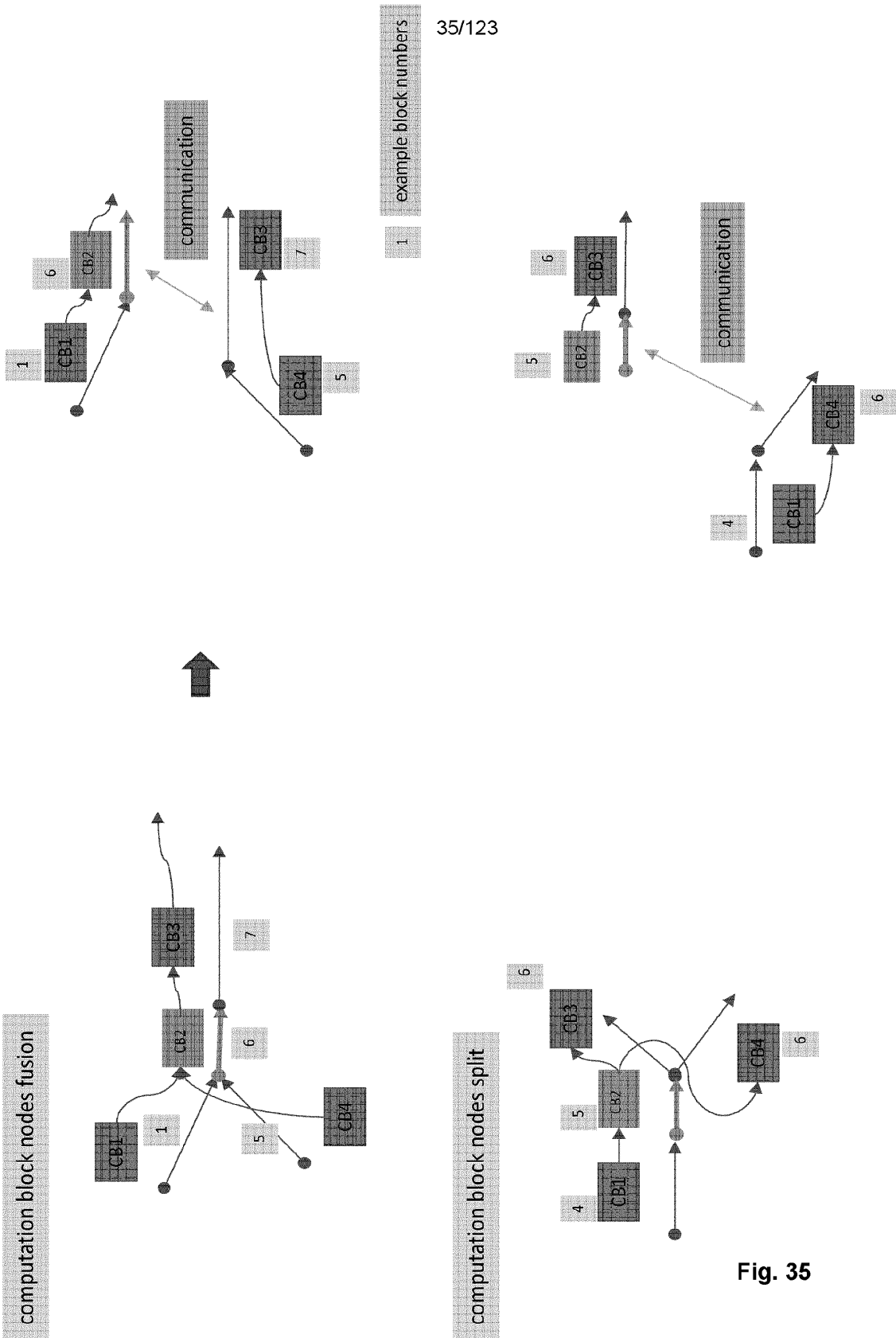


Fig. 34



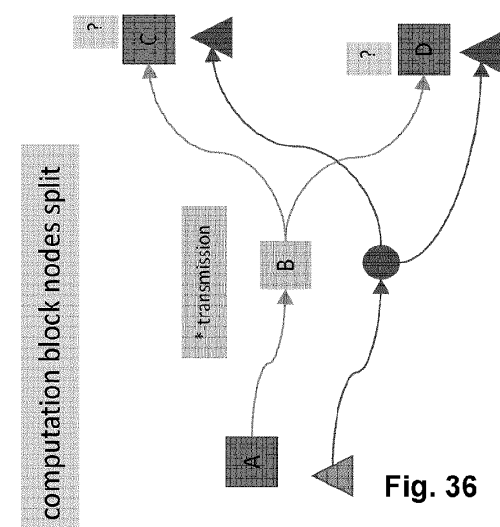
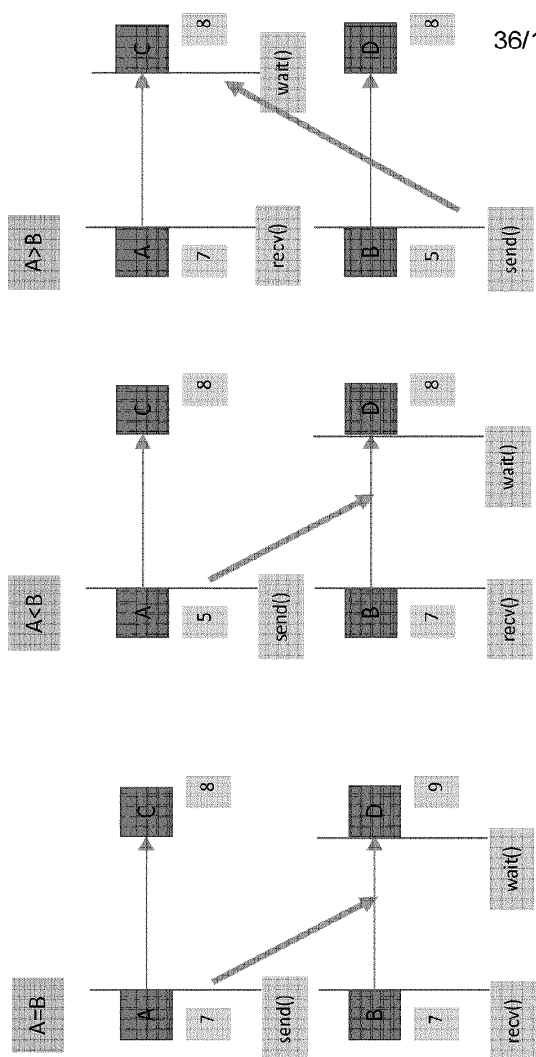
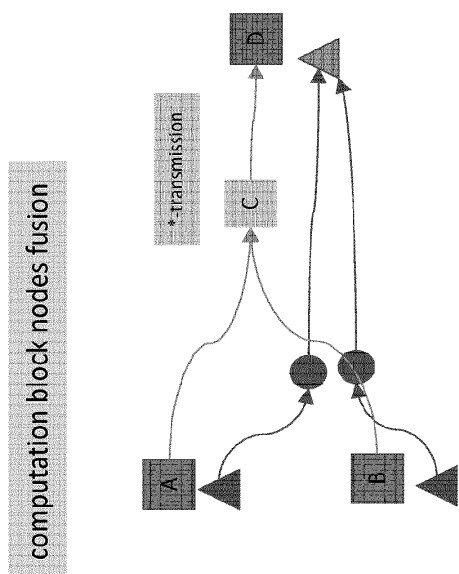
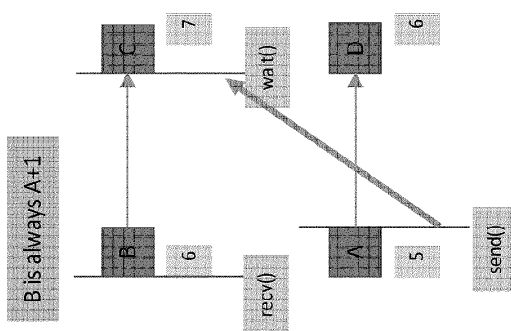
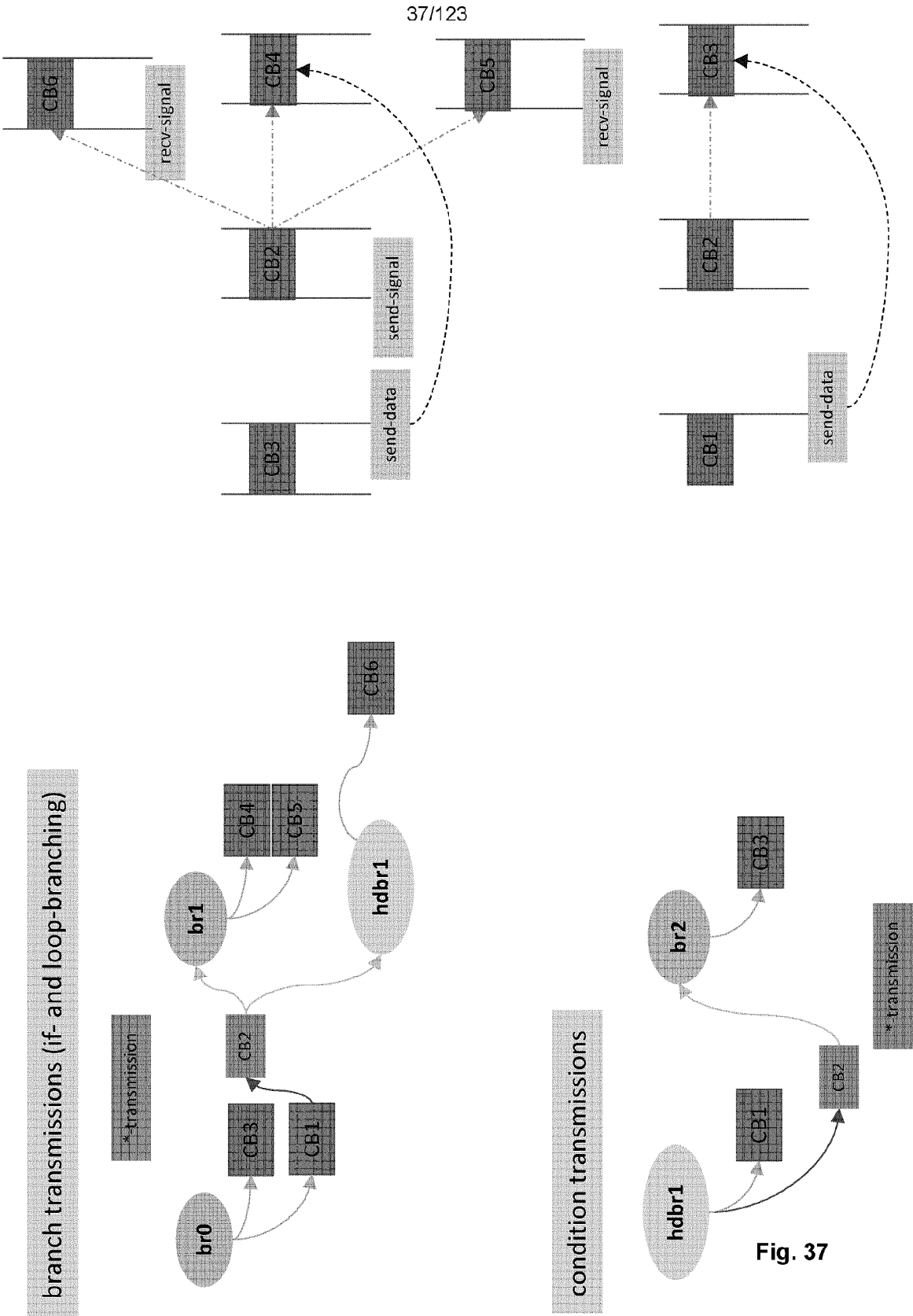
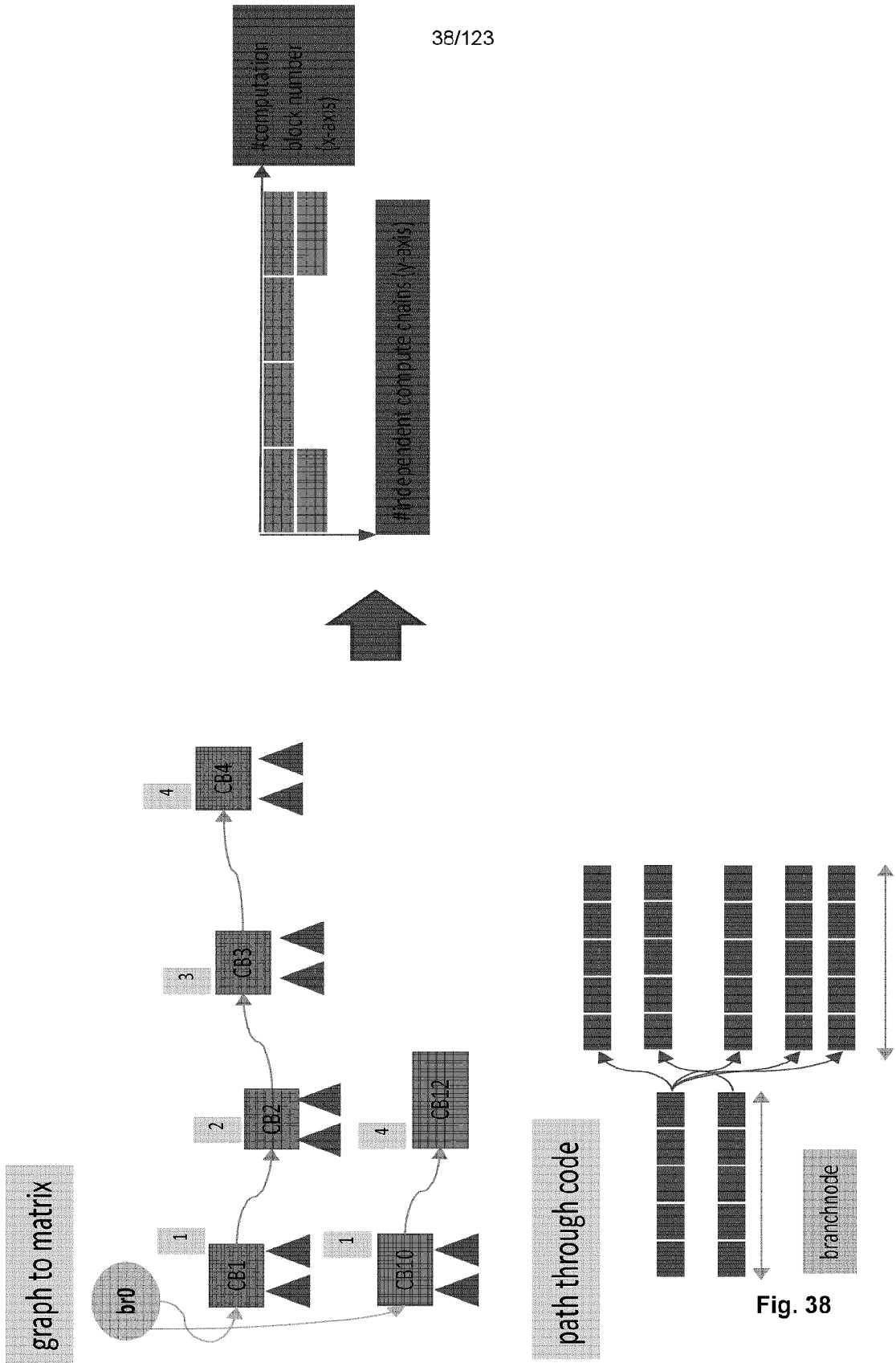


Fig. 36







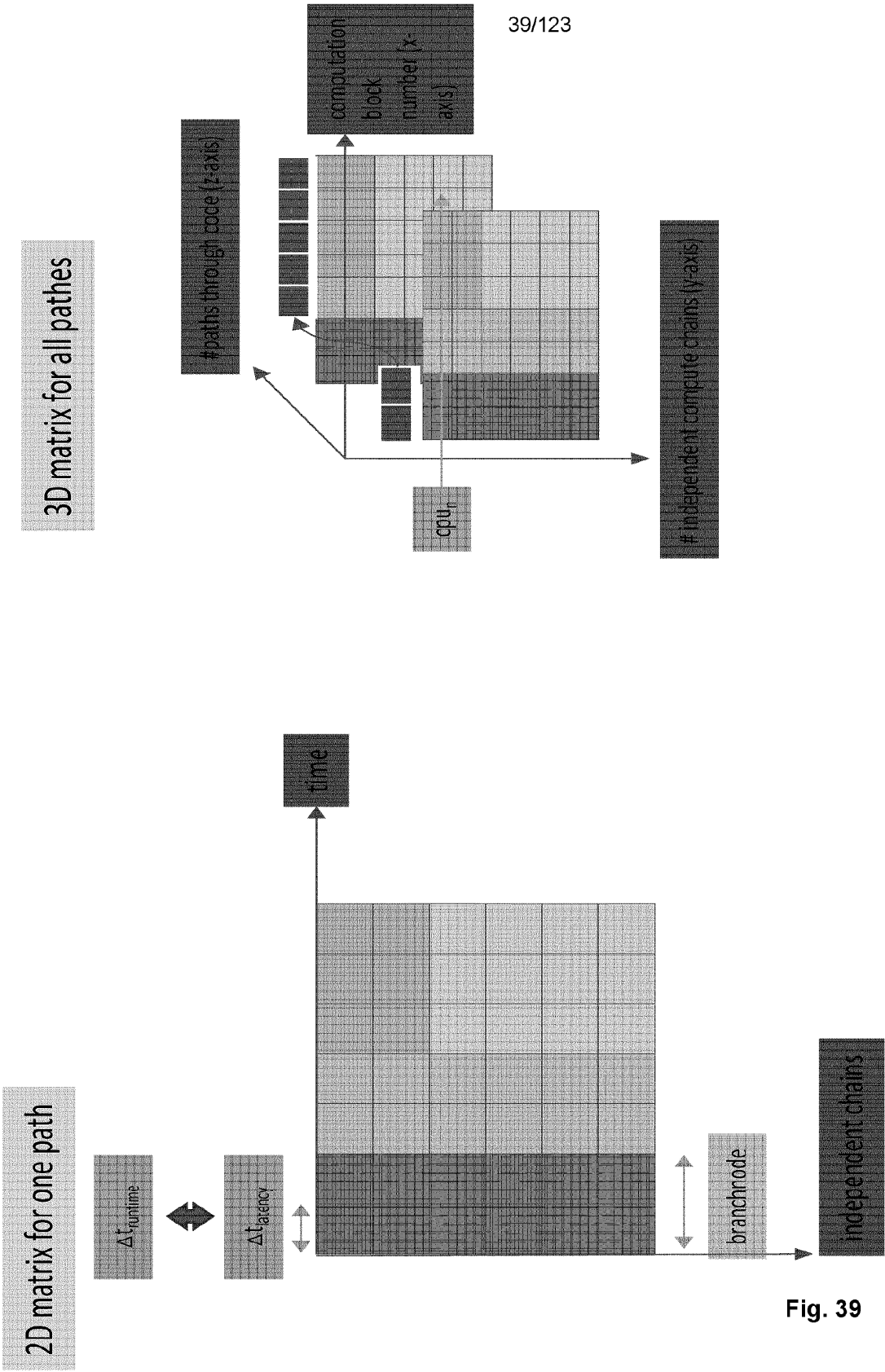


Fig. 39

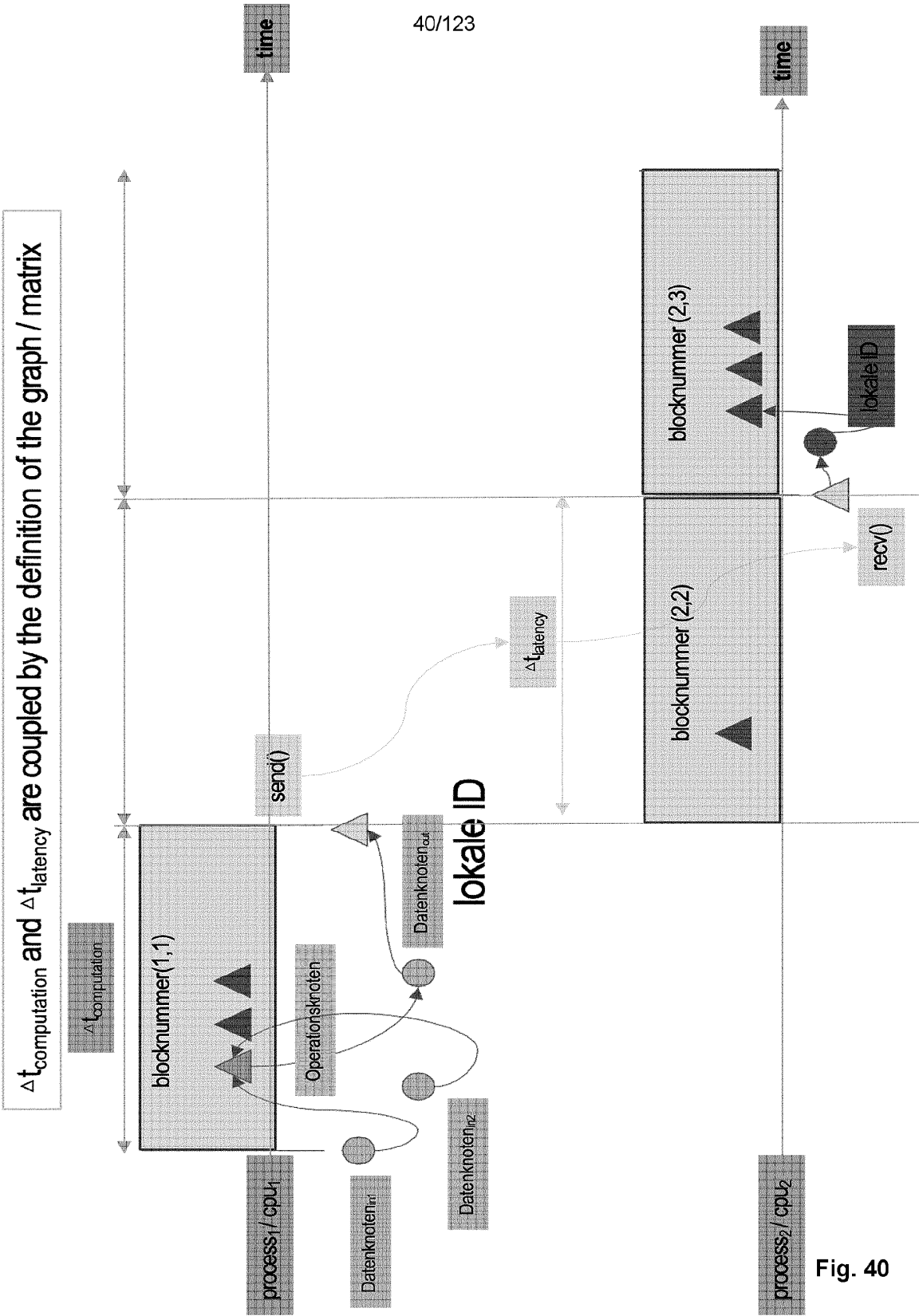


Fig. 40

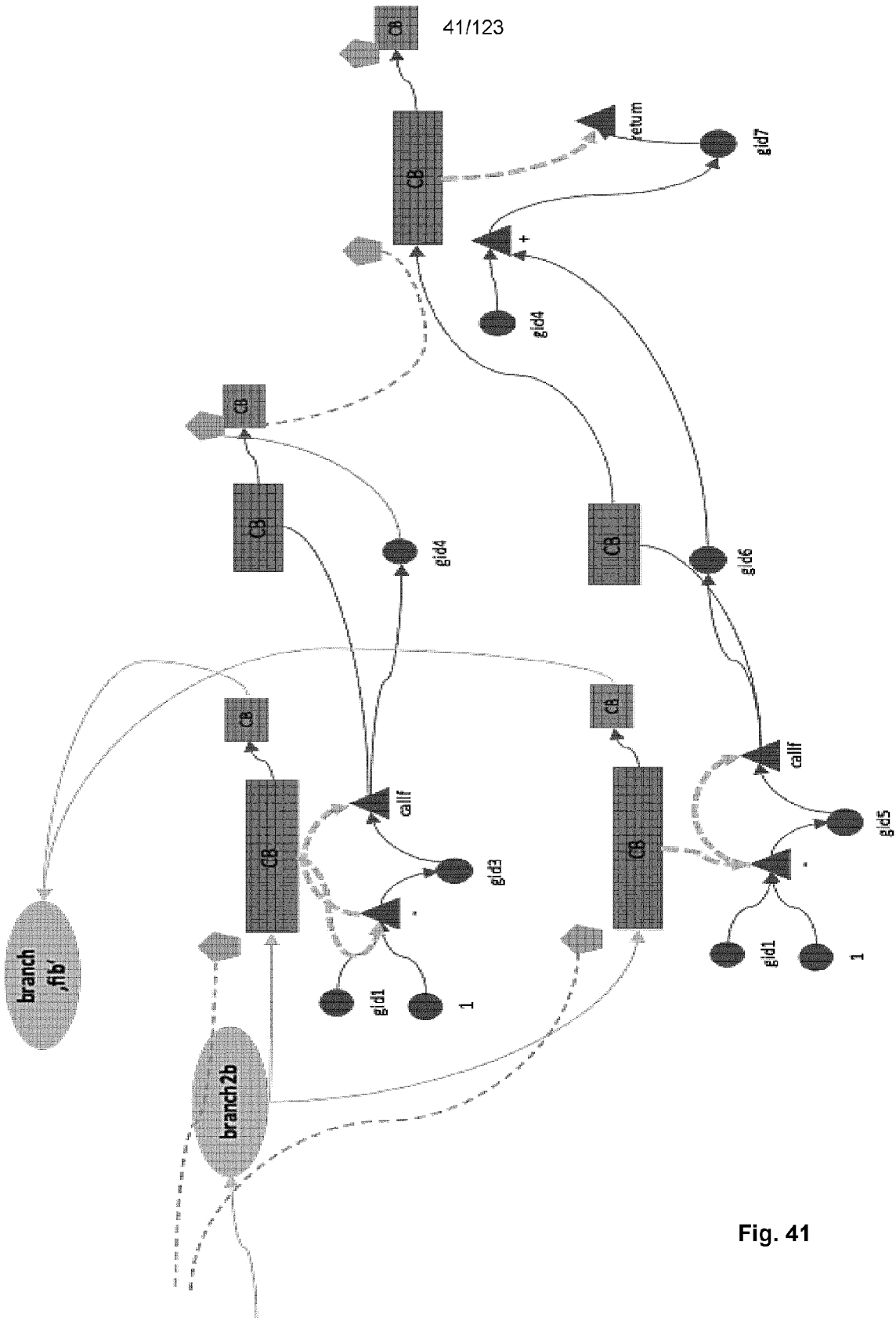


Fig. 41

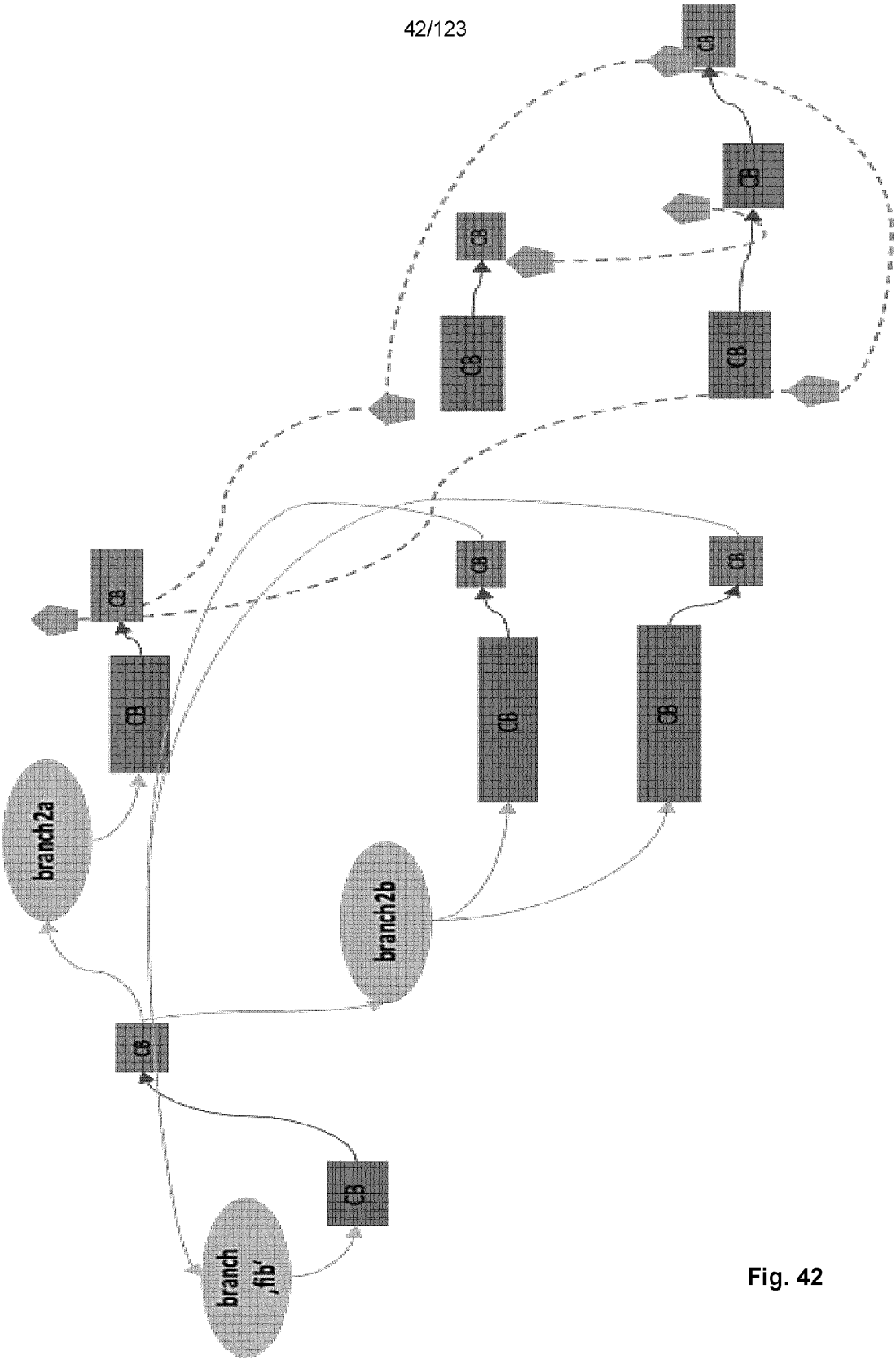


Fig. 42

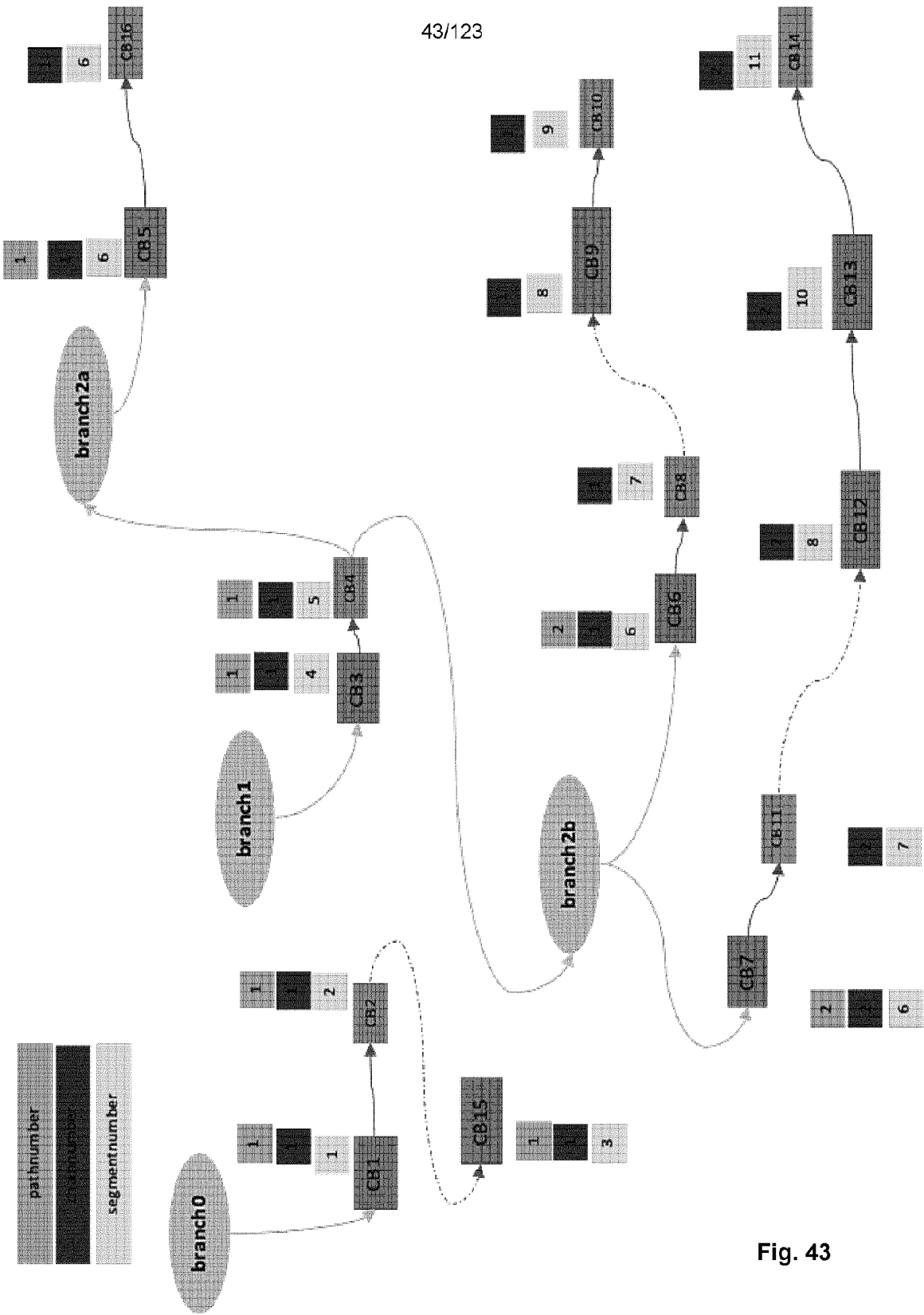
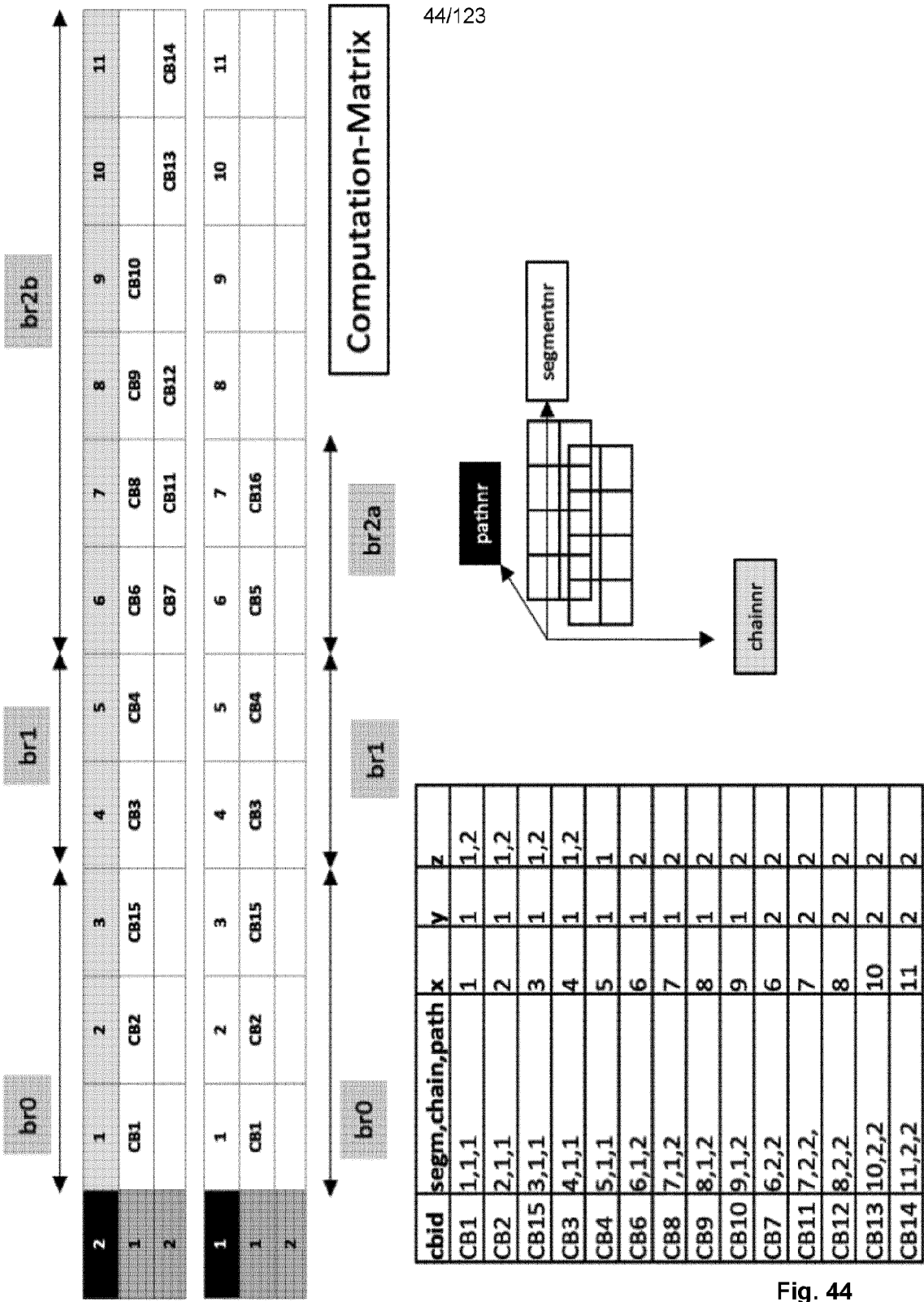


Fig. 43



Transfer-Matrix

	2	1	1	2	3	4	5	6	7	8	9	10	11
1		e: COM1->			s: ->COM10	e: SIG1-> COM2-> s: ->COM1 ->COM4 ->COM5		s: ->SIG1 ->COM2 e: COM4->		s: ->COM8	s: COM6->		
2								s: ->SIG1 ->COM2 e: COM5->		s: ->COM9		s: ->COM6	s: COM7->

	1	2	3	4	5	6	7	8	9	10	11
1											
1	e: COM1->		s: ->COM10	e: SIG1-> COM2-> s: ->COM1 ->COM4 ->COM5		s: ->SIG1 ->COM2 e: COM3->					
2											

Fig. 45

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	source cbid	start	target cbid	end	variable	direction
COM1	CB1 - (1,1,1)	CB3 - (4,1,1)			gid8, addr CB15	forward
SIG1	CB3 - (4,1,1)	CB5 - (6,1,1), CB6 - (6,1,2), CB7 - (6,2,2)			gid2	forward
COM2	CB3 - (4,1,1)	CB5 - (6,1,1), CB6 - (6,1,2), CB7 - (6,2,2)			gid1	forward
COM3	CB5 - (6,1,1)	CB15 / CB9 / CB12			gid1	
COM4	CB6 - (6,1,2)	CB3 - (4,1,1)			gid3, addr CB9	backward
COM5	CB7 - (6,2,2)	CB3 - (4,1,1)			gid5, addr CB12	backward
COM6	CB9 - (9,1,2)	CB10 - (10,2,2)			gid4	forward
COM7	CB13 - (10,2,2)	CB15 / CB9 / CB12			gid7	
COM8	LL	CB9 - (8,1,2)			gid4	
COM9	LL	CB12 - (8,2,2)			gid6	
COM10	LL	CB15 - (3,1,1)			gid9	

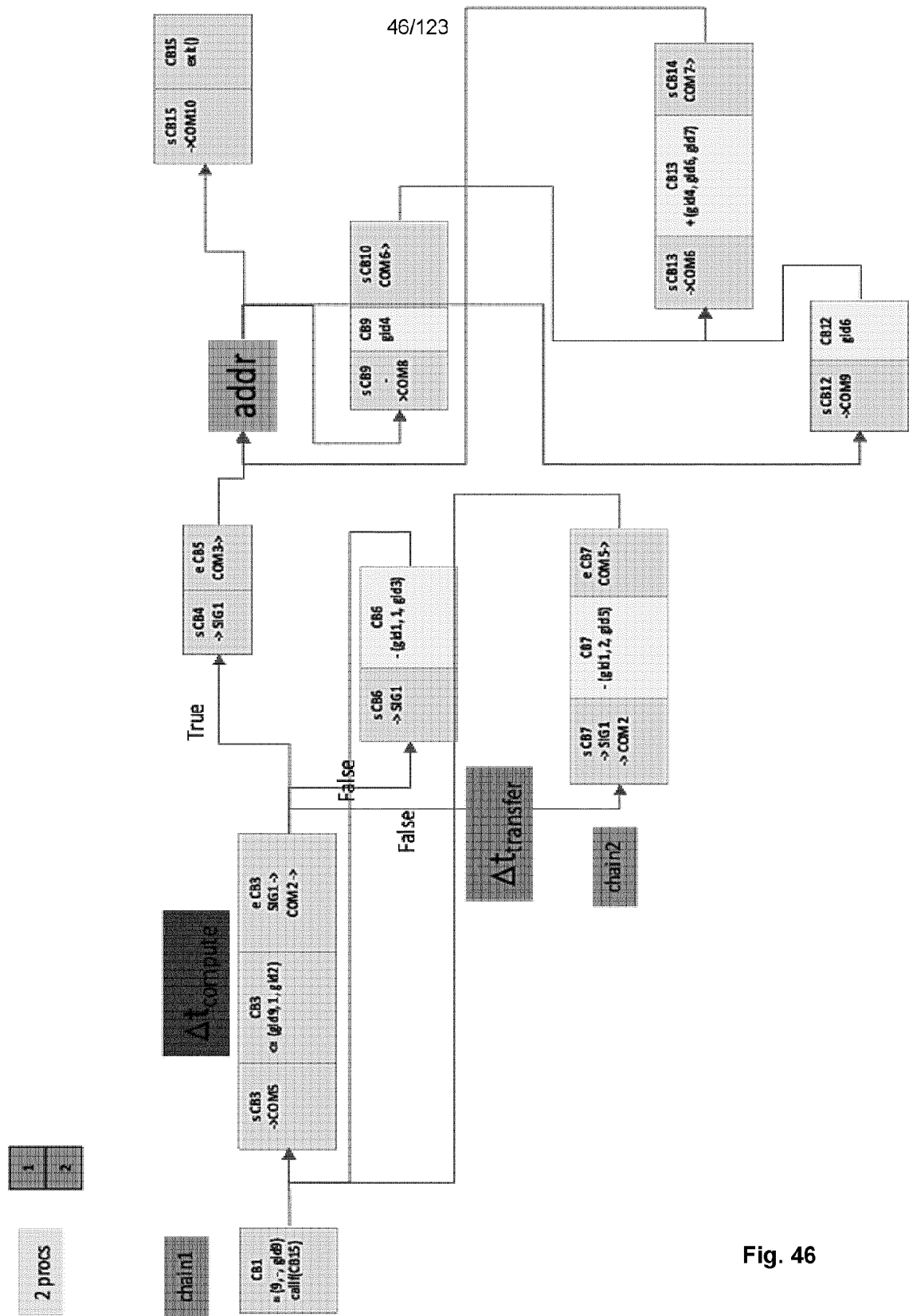
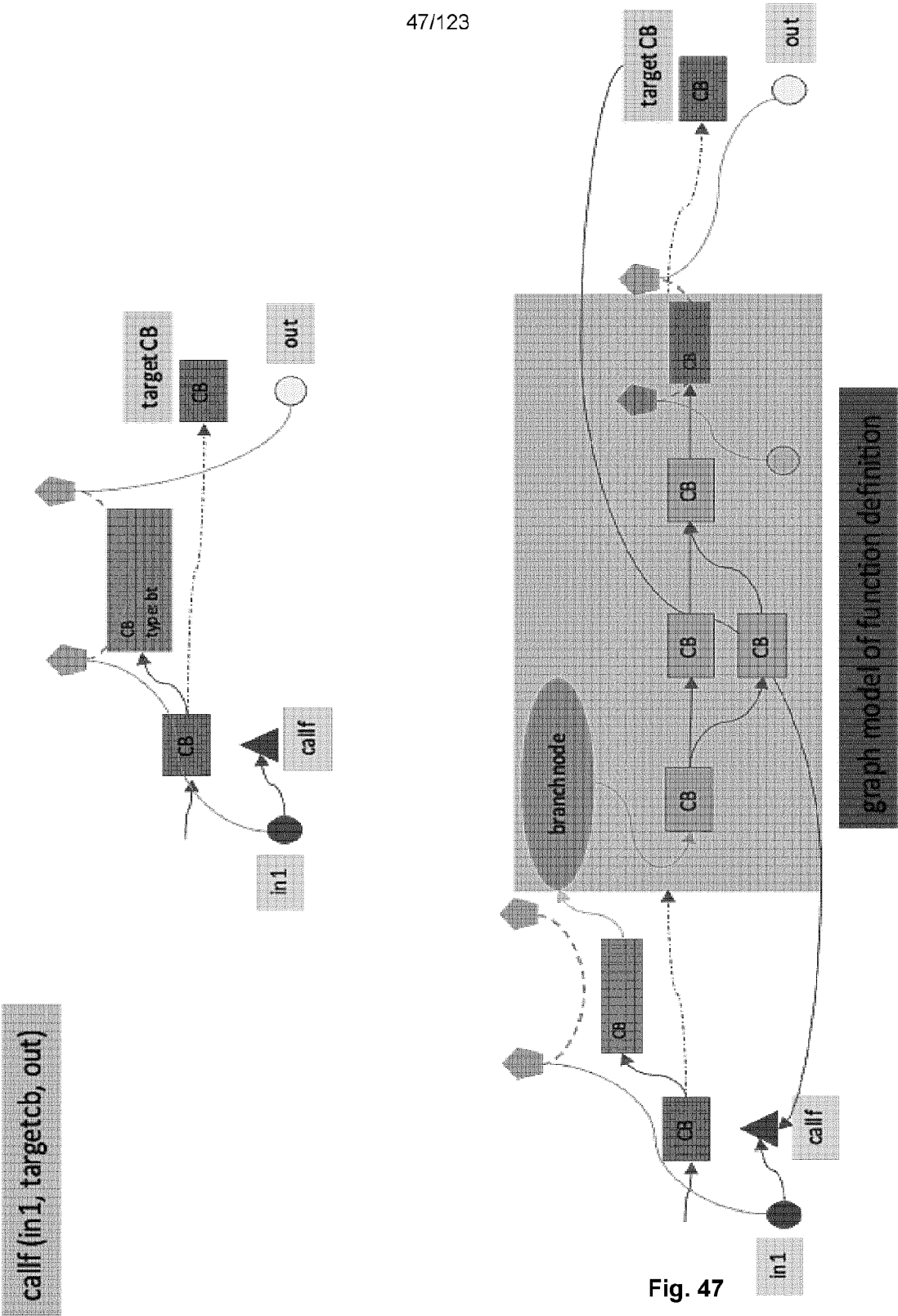


Fig. 46



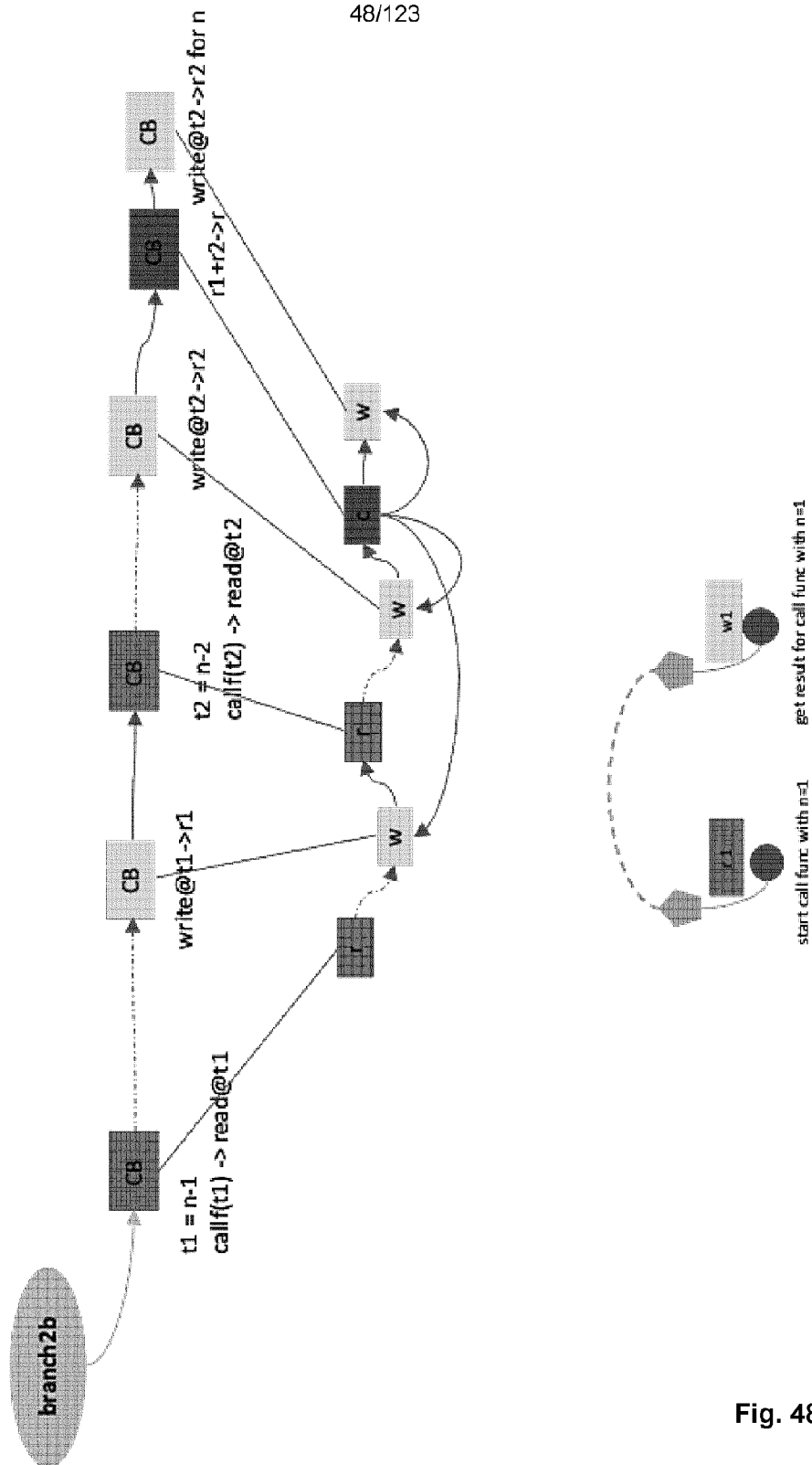


Fig. 48

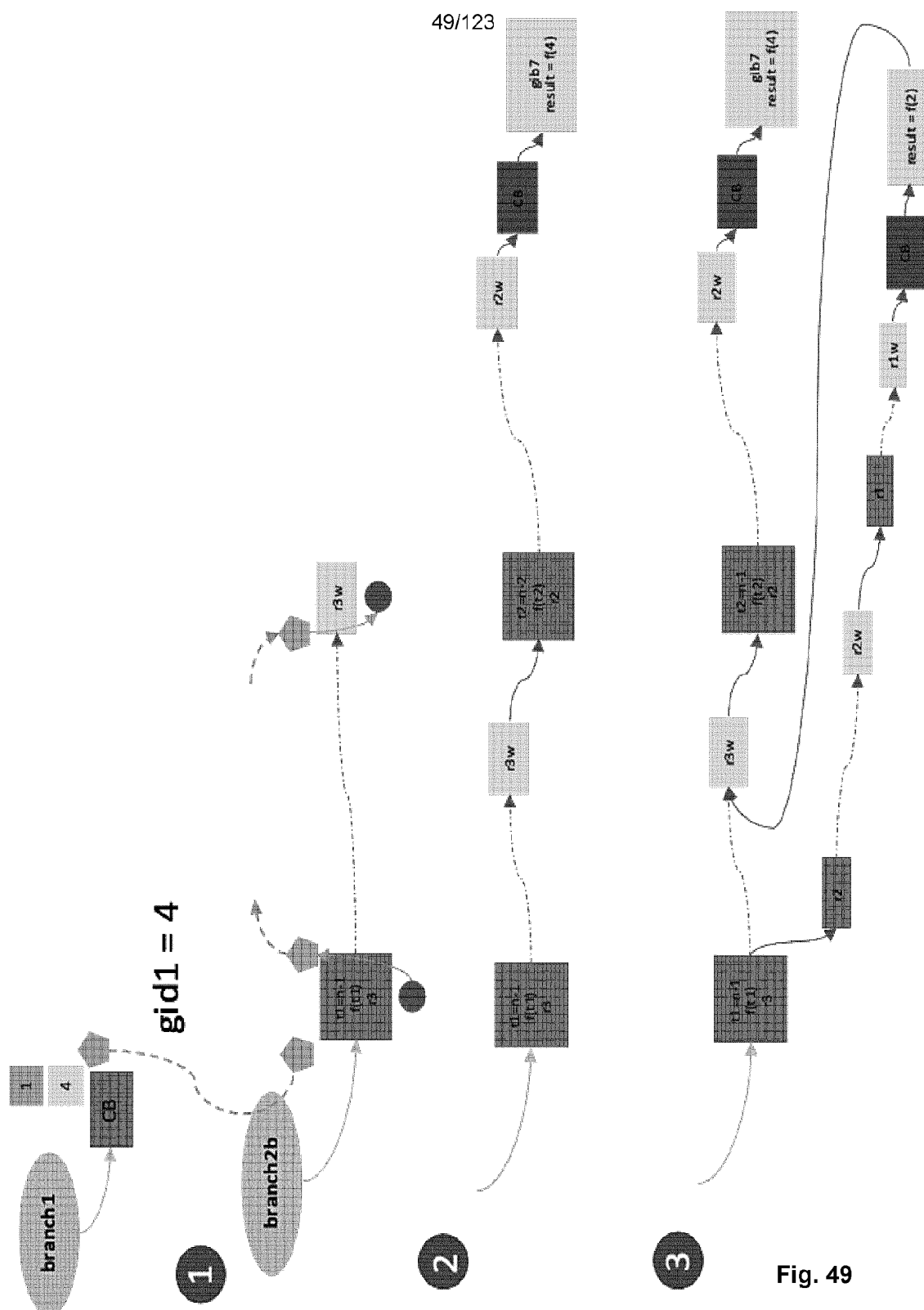


Fig. 49

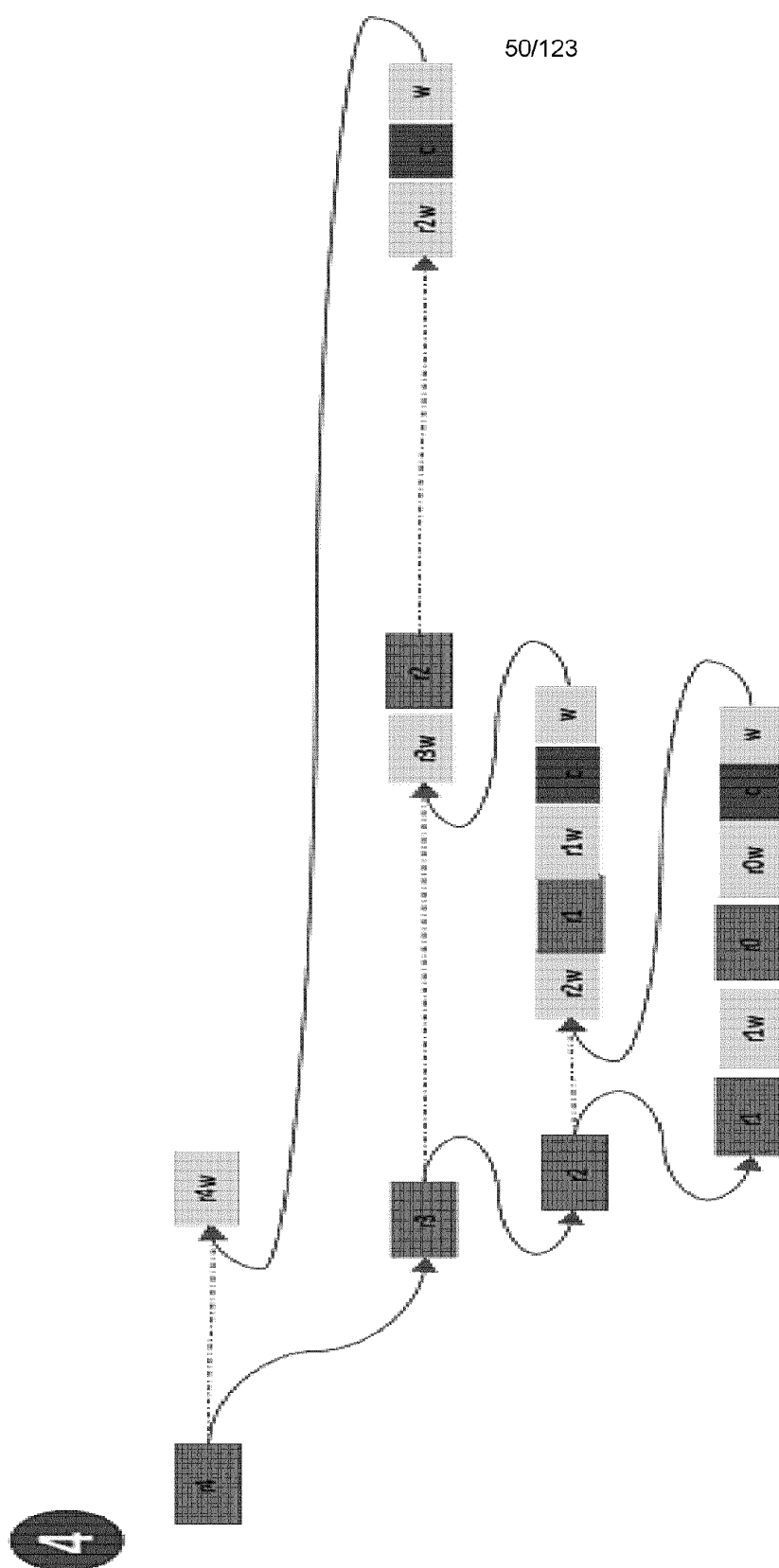


Fig. 50

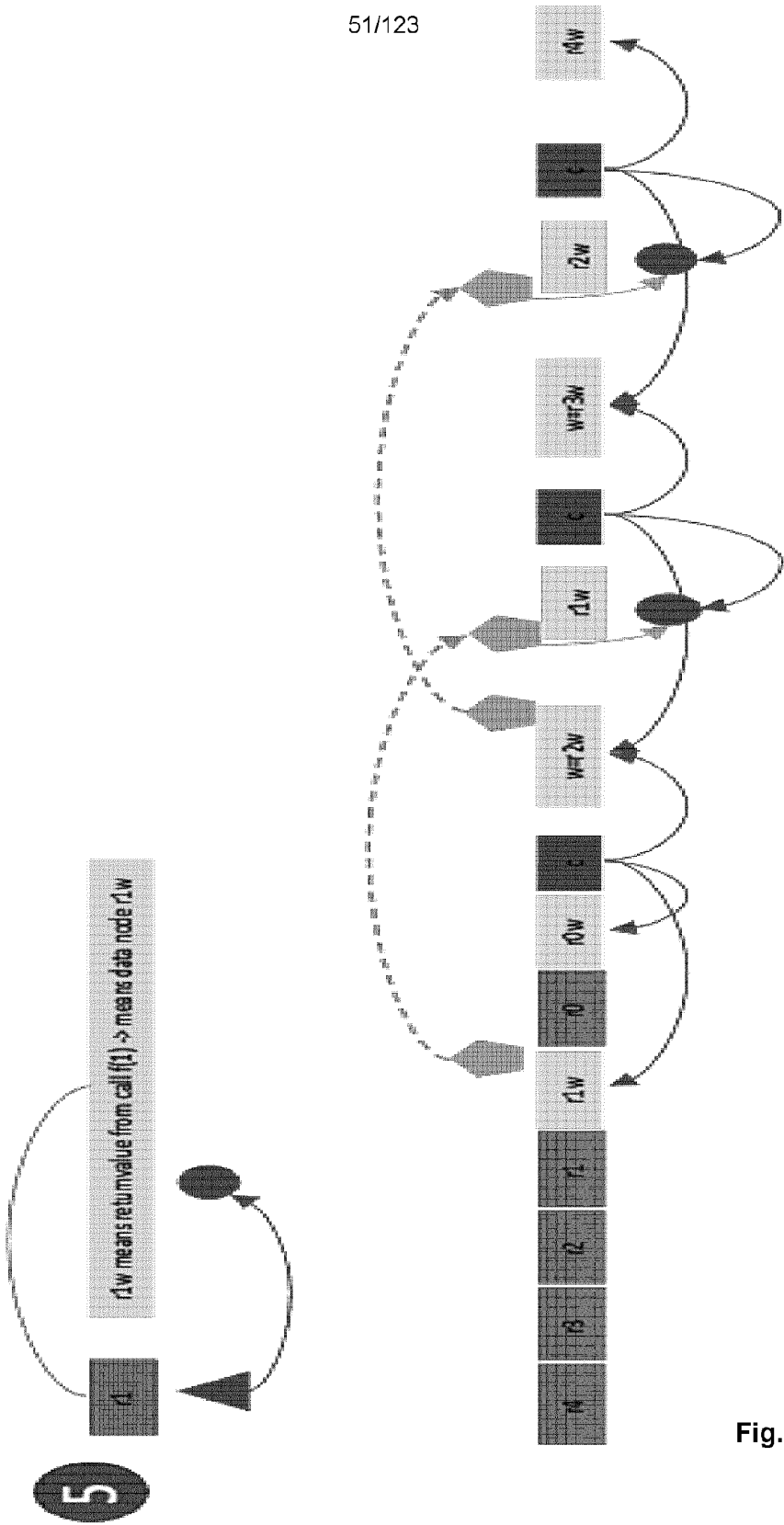


Fig. 51

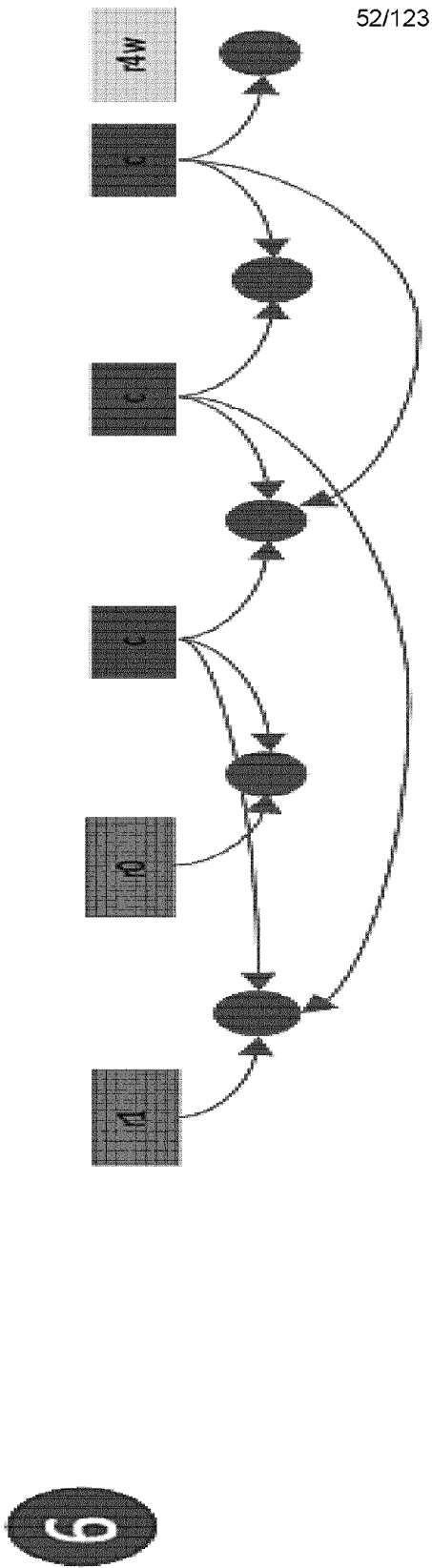


Fig. 52

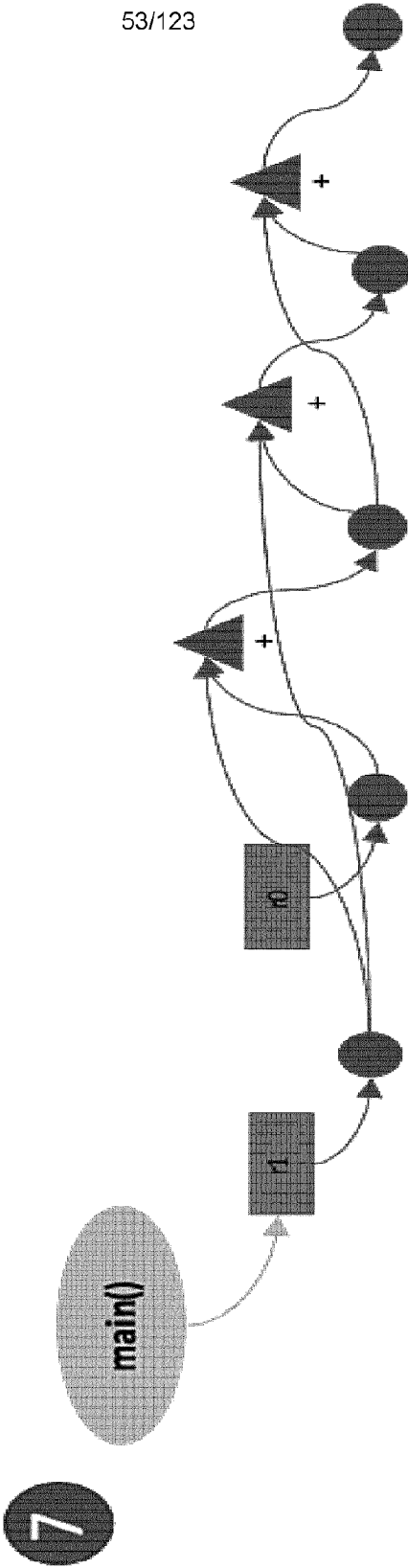


Fig. 53

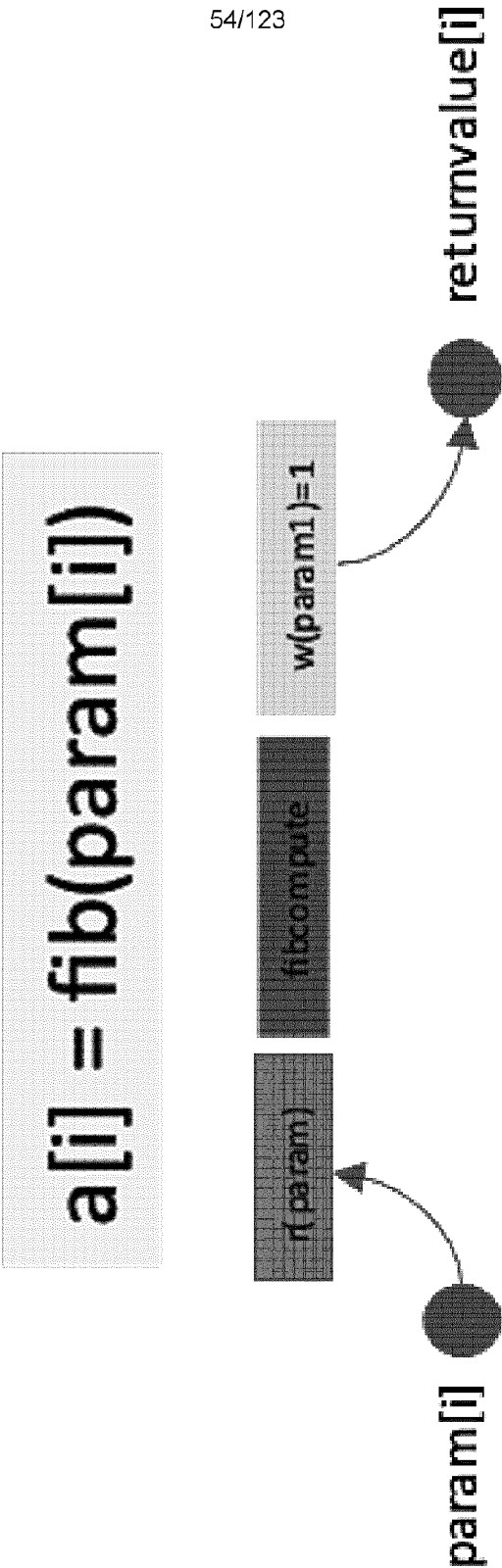


Fig. 54

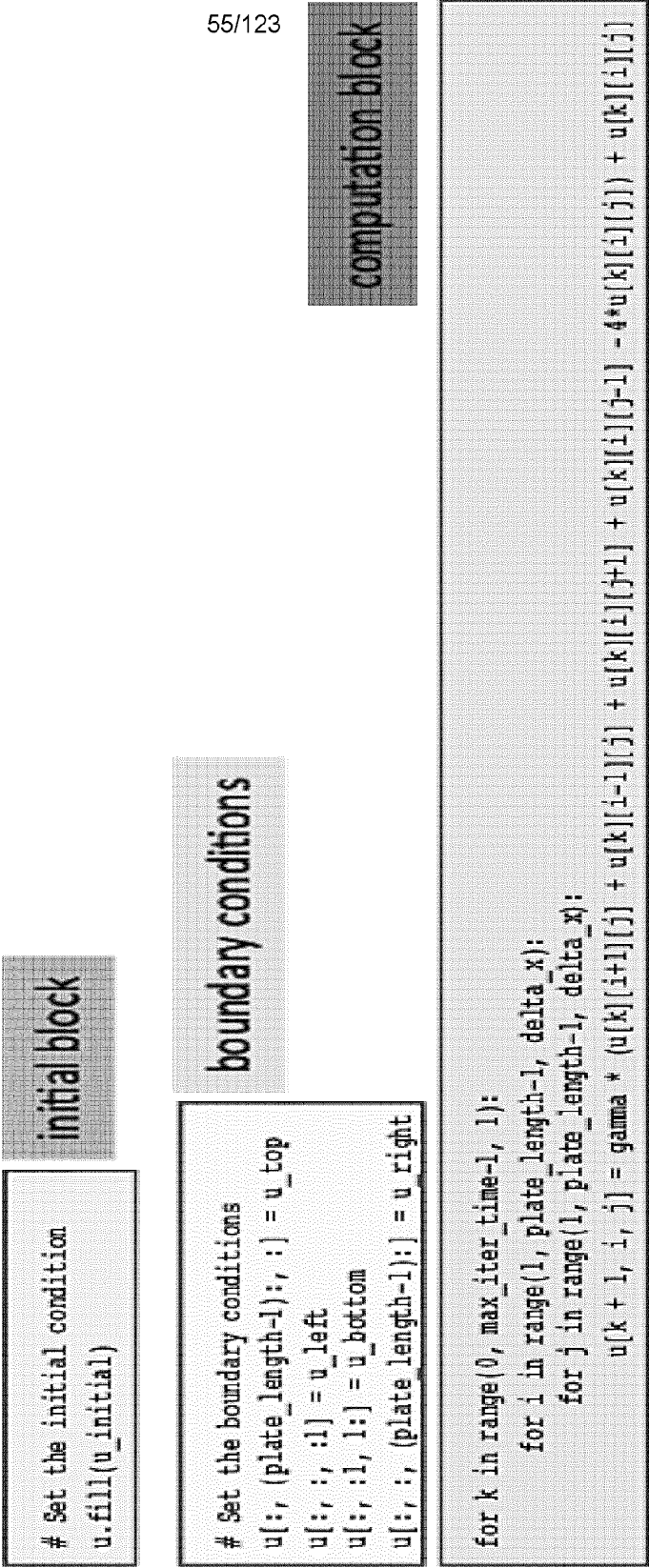


Fig. 55

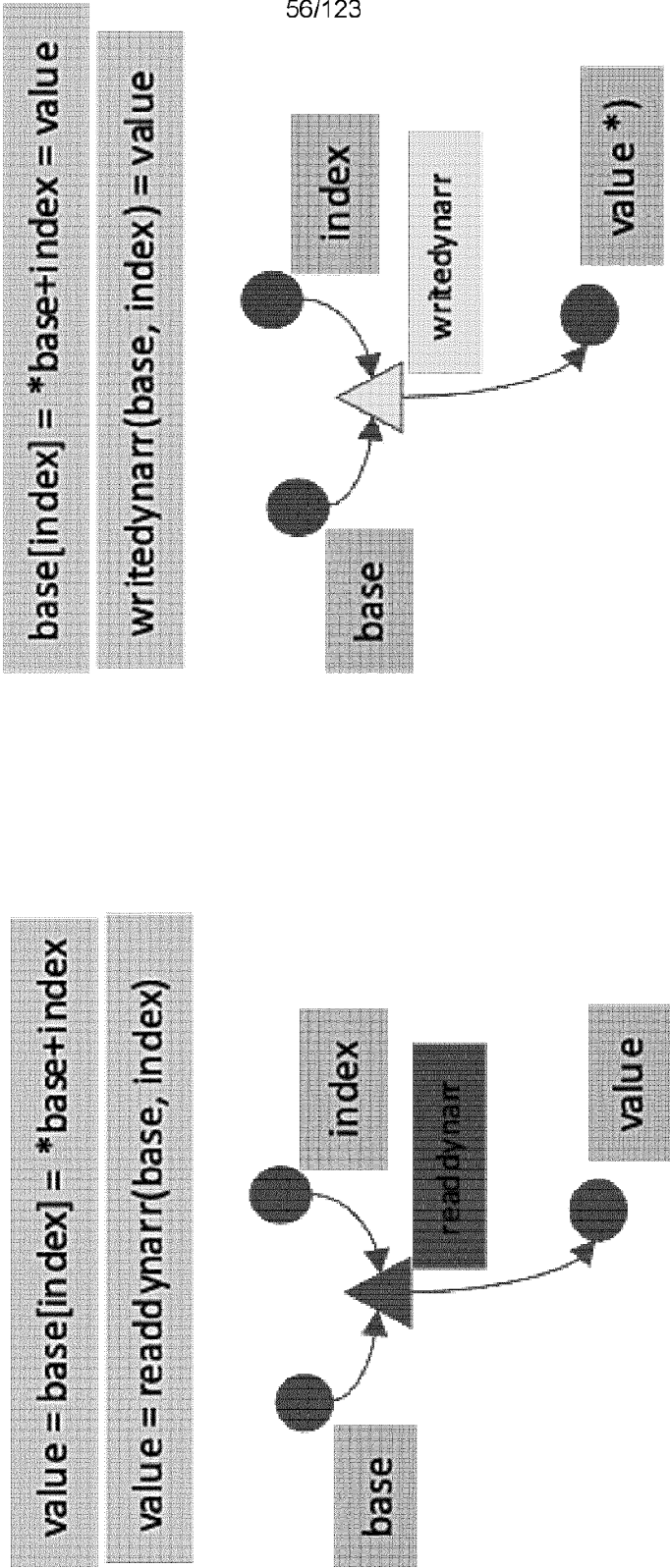


Fig. 56

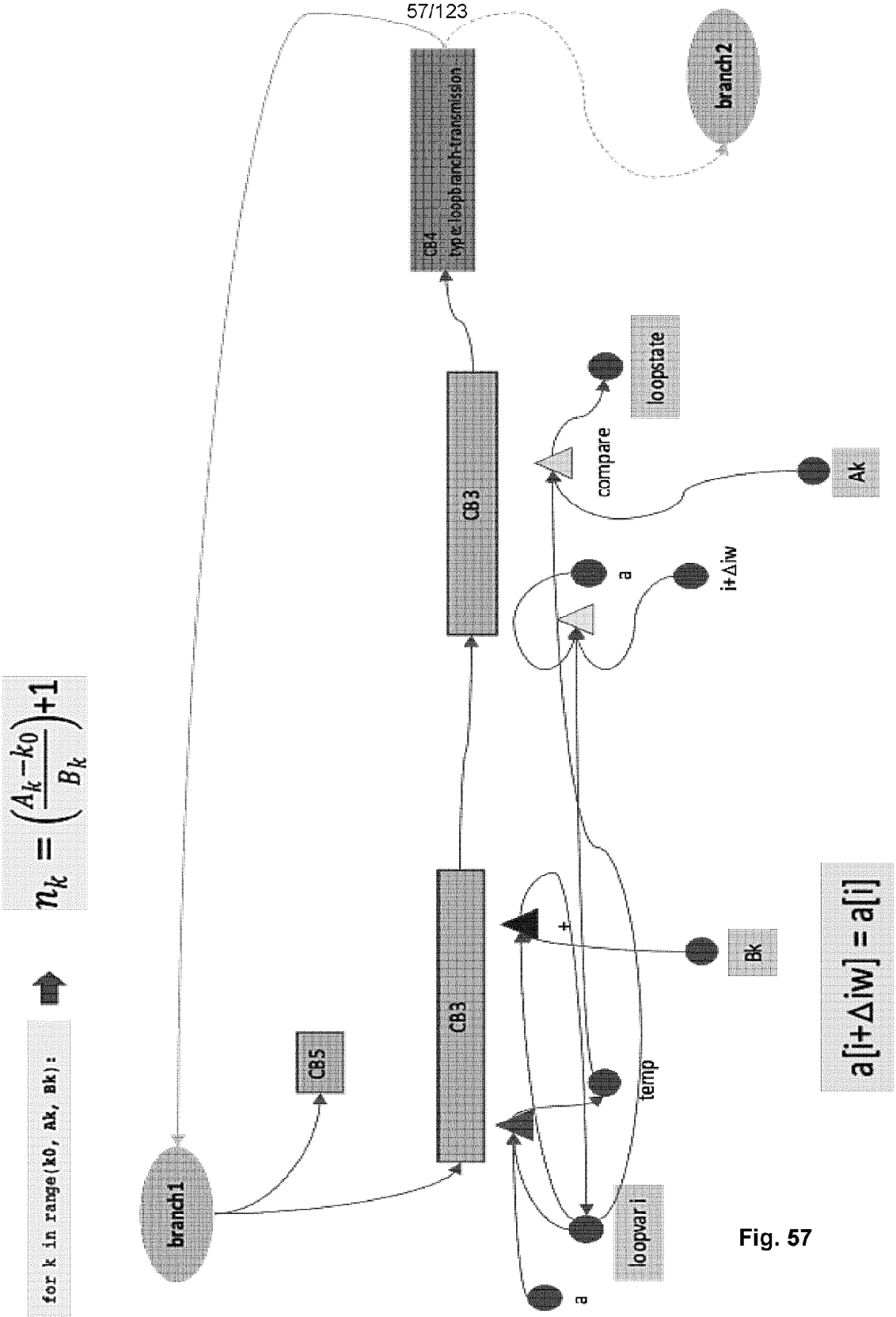


Fig. 57

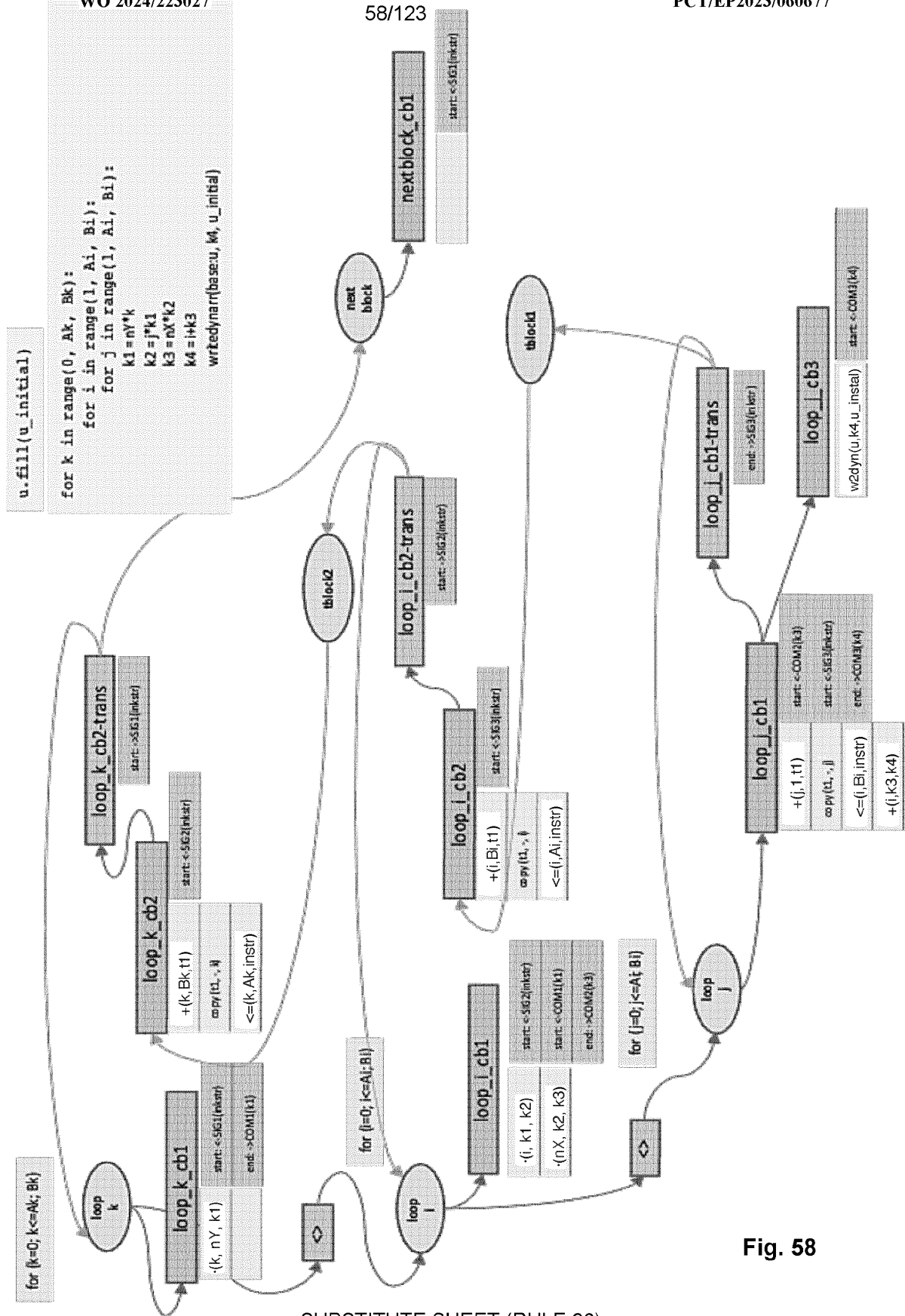
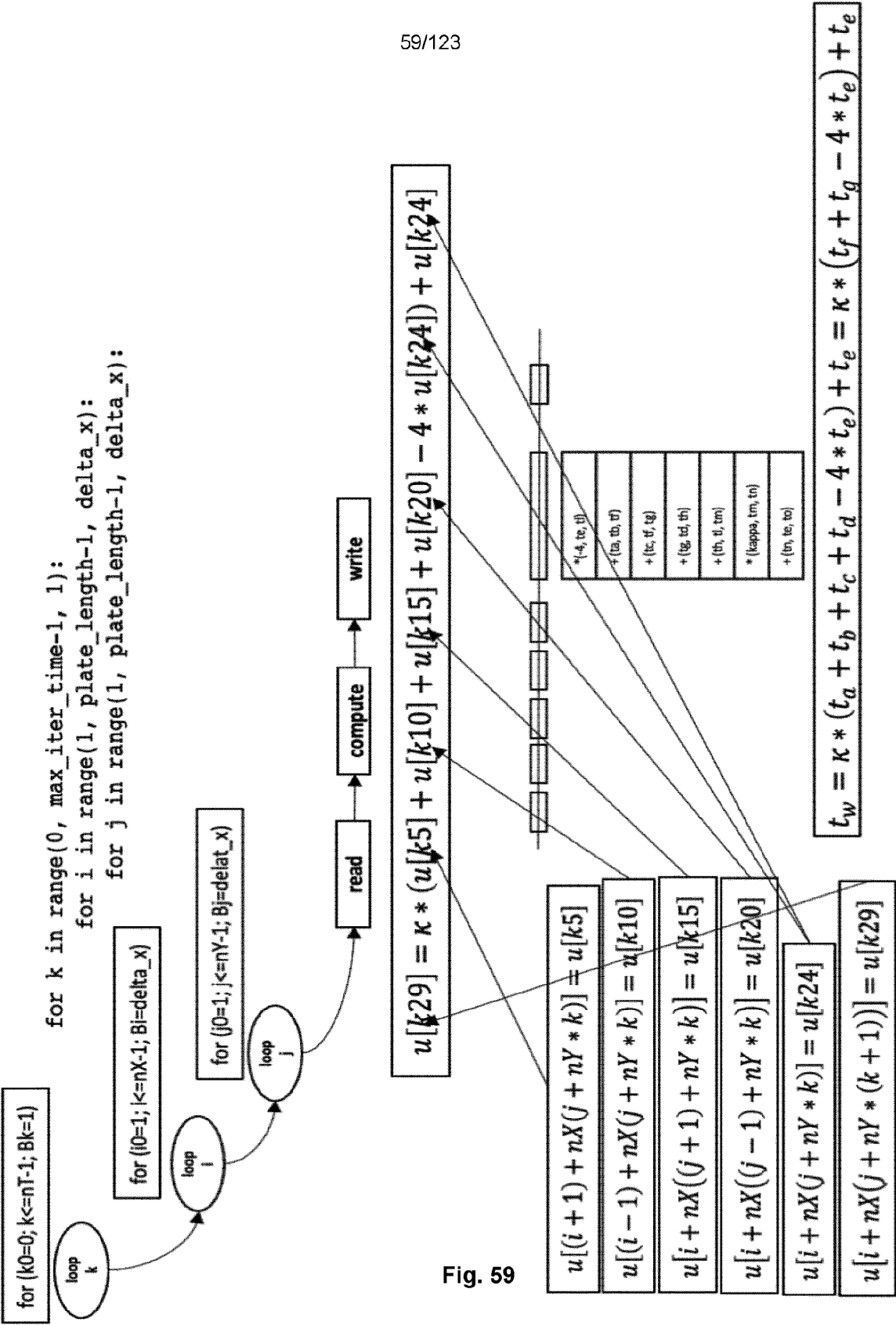


Fig. 58



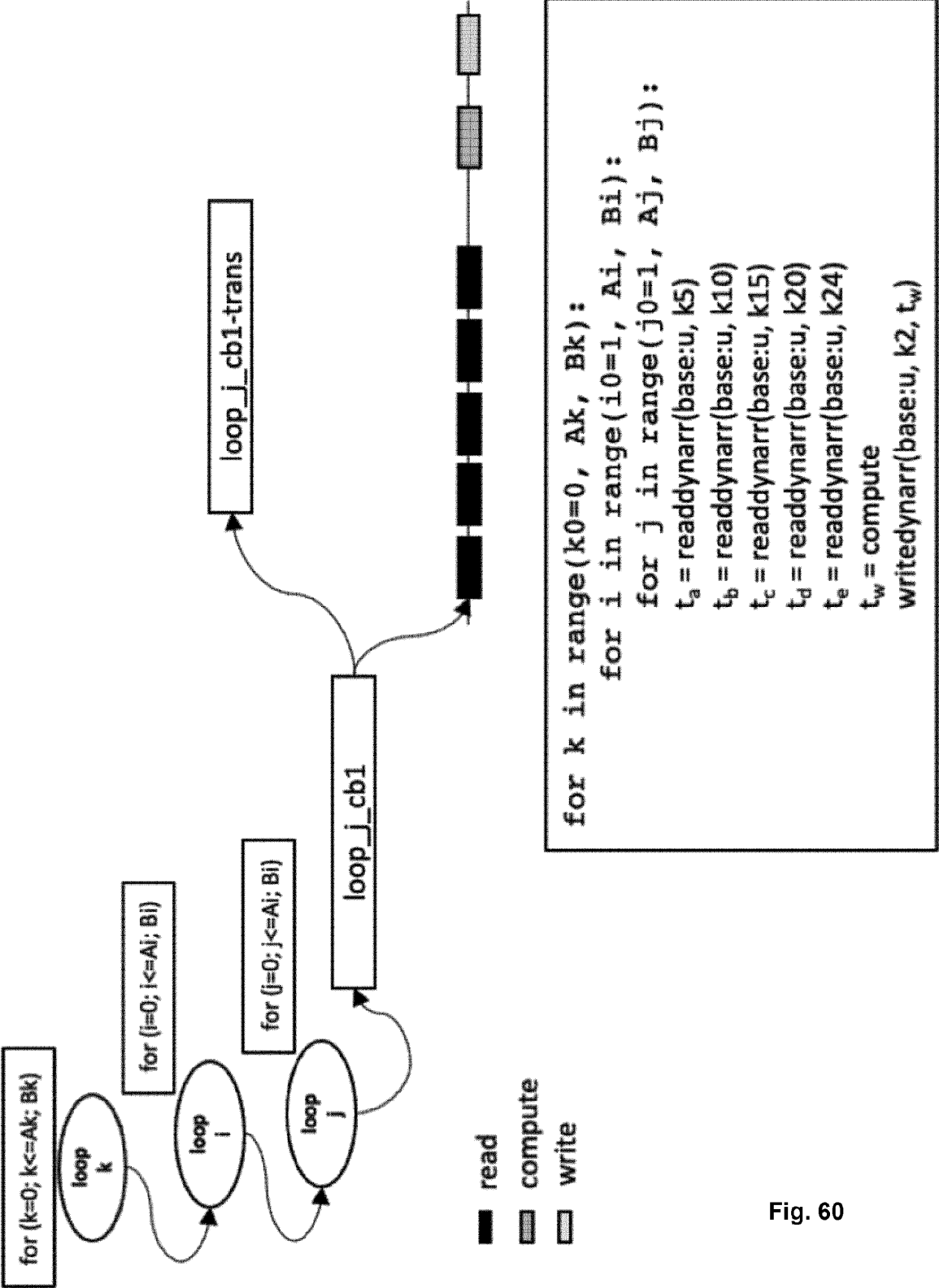


Fig. 60

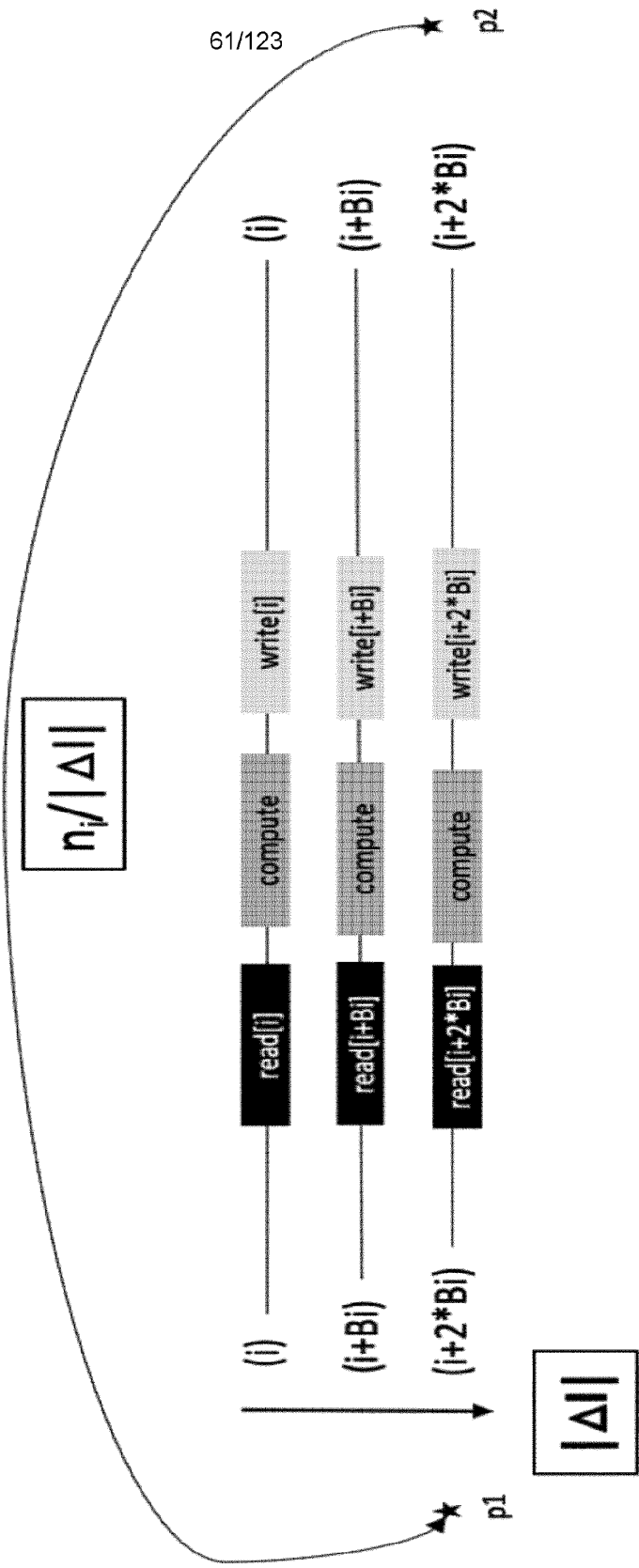


Fig. 61

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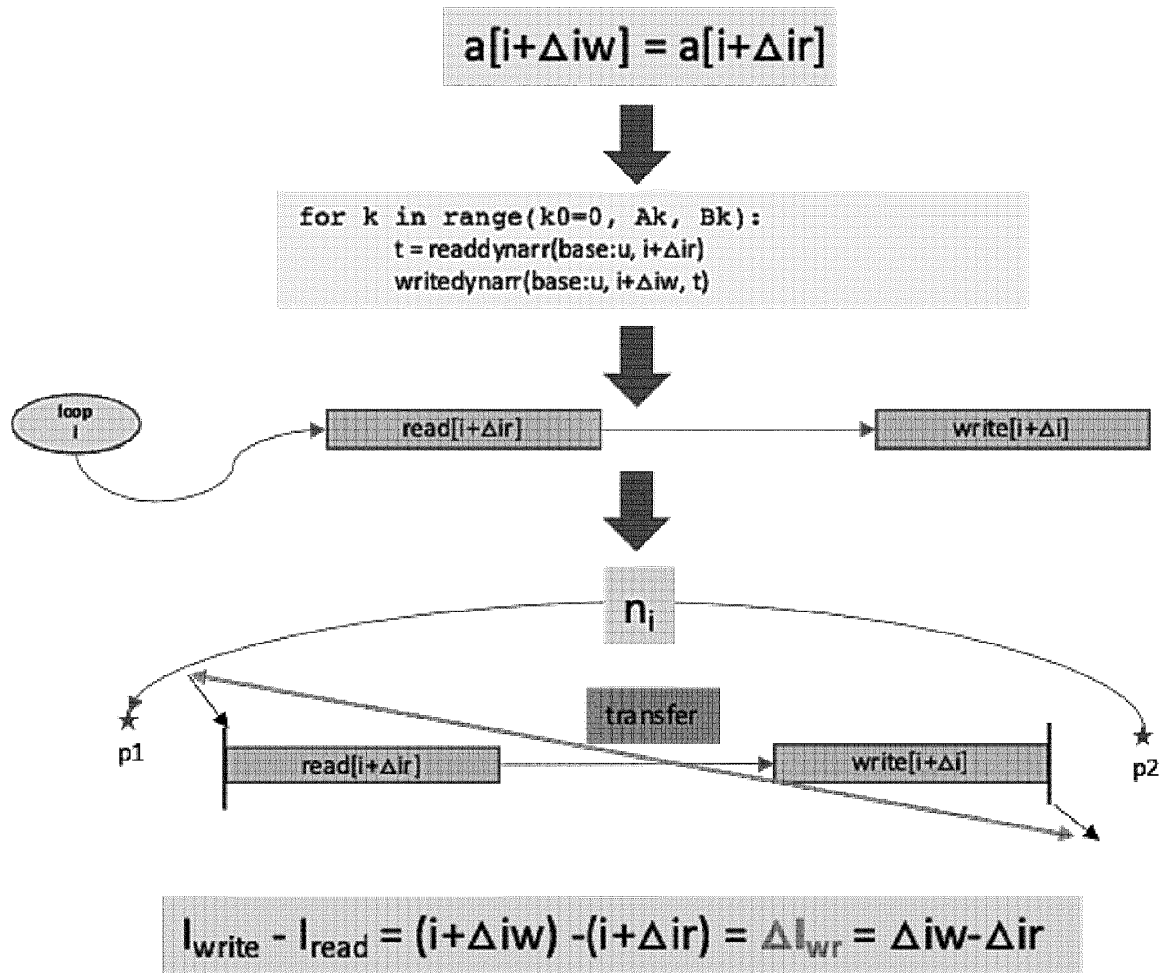


Fig. 62

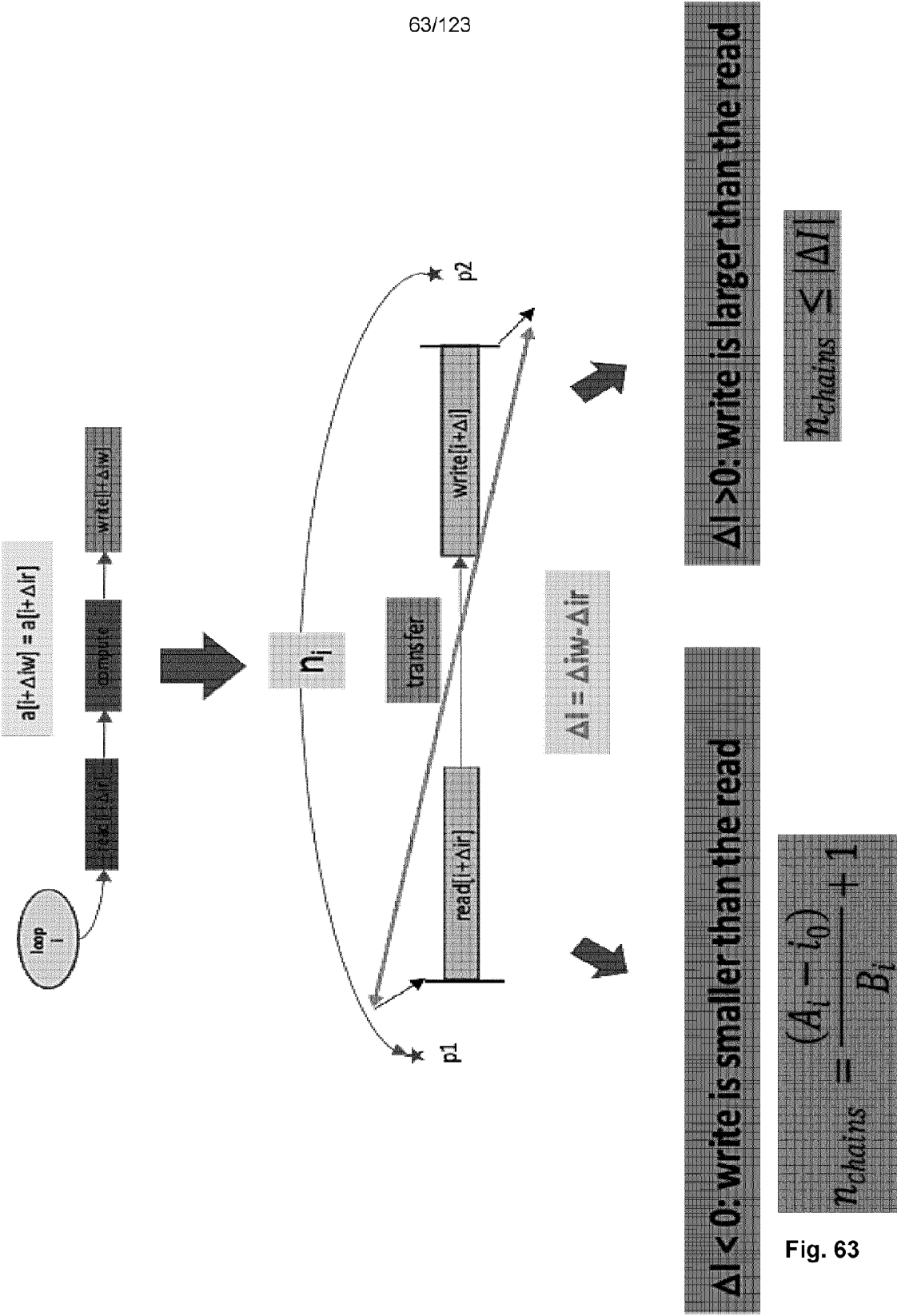


Fig. 63

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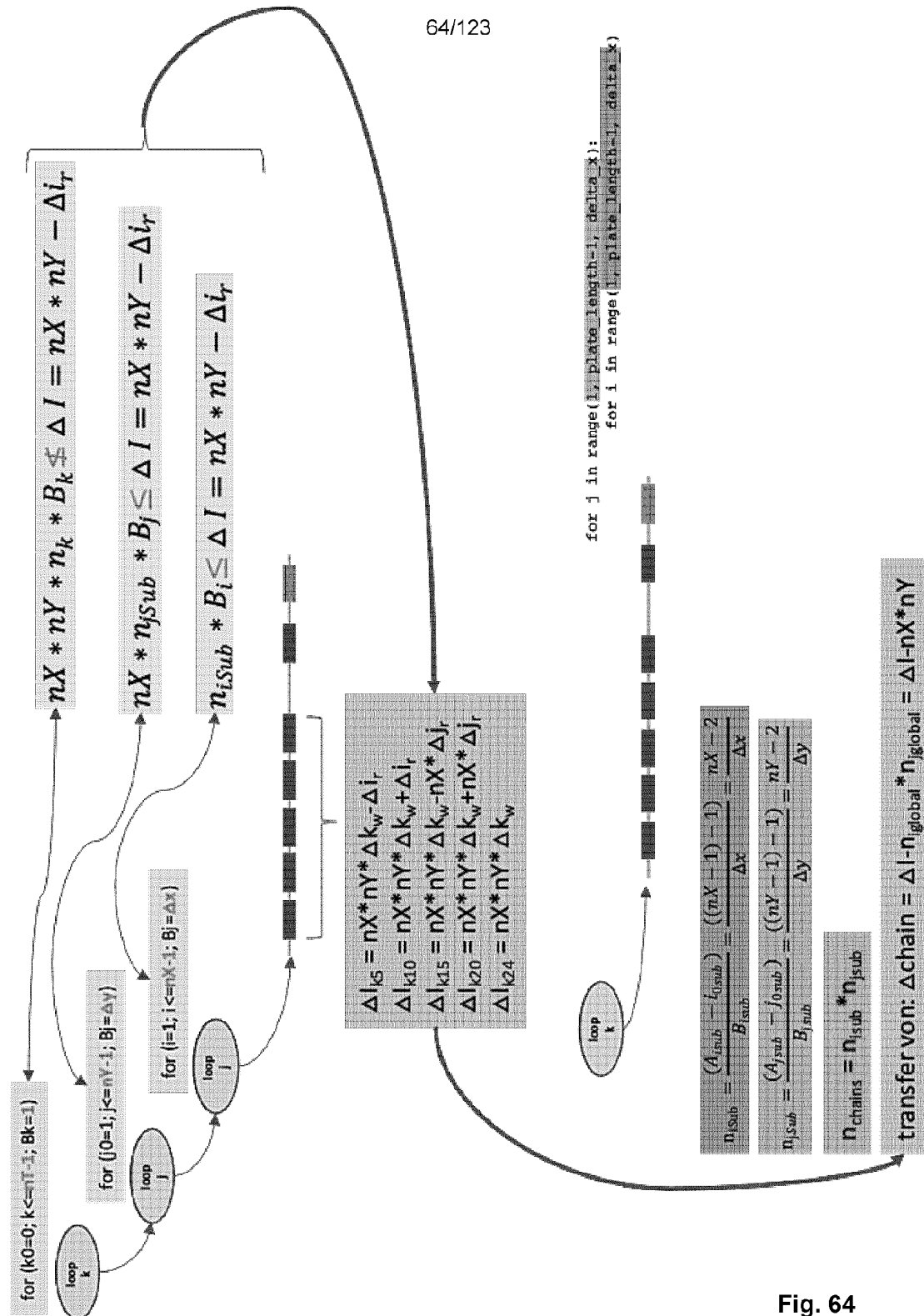
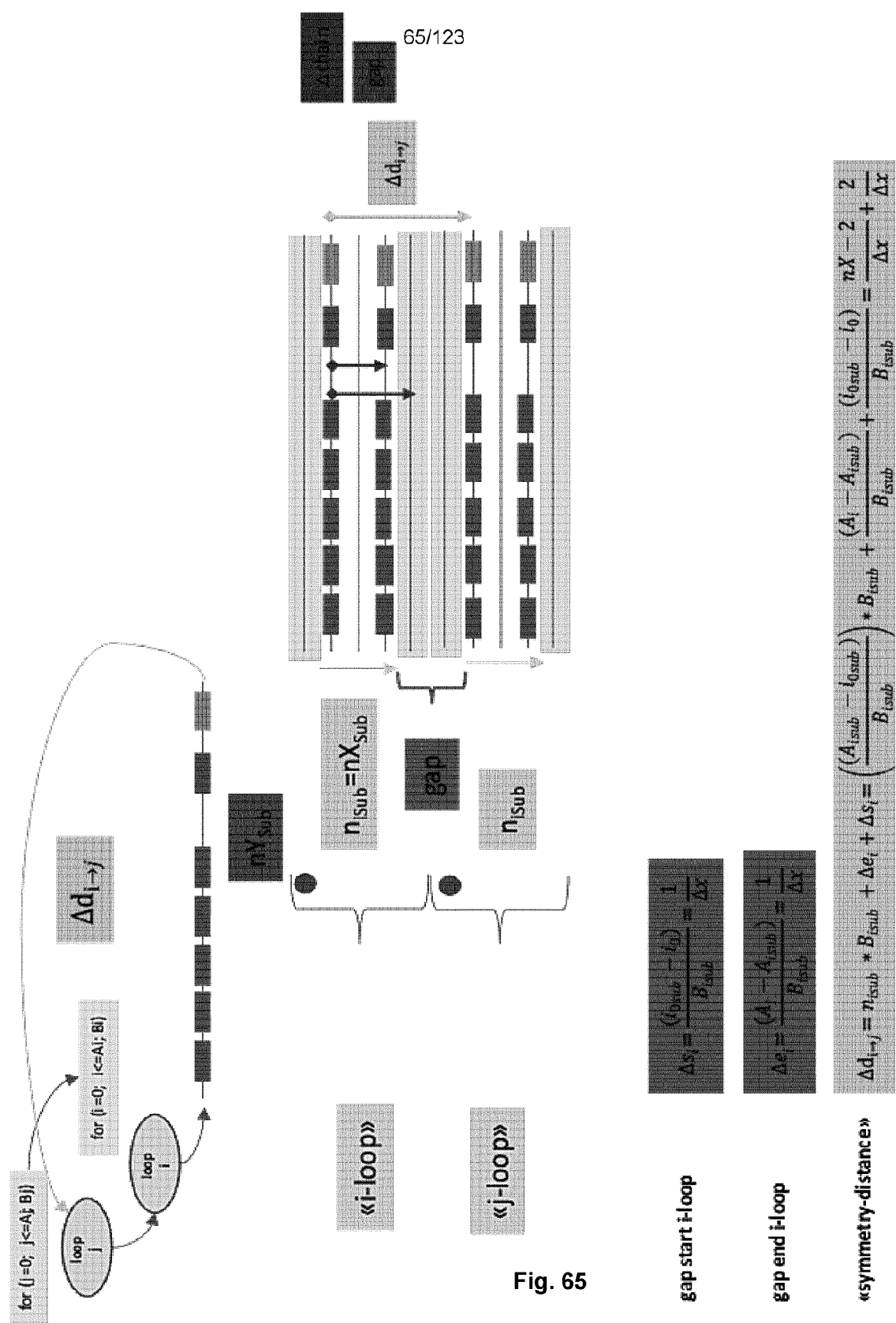


Fig. 64



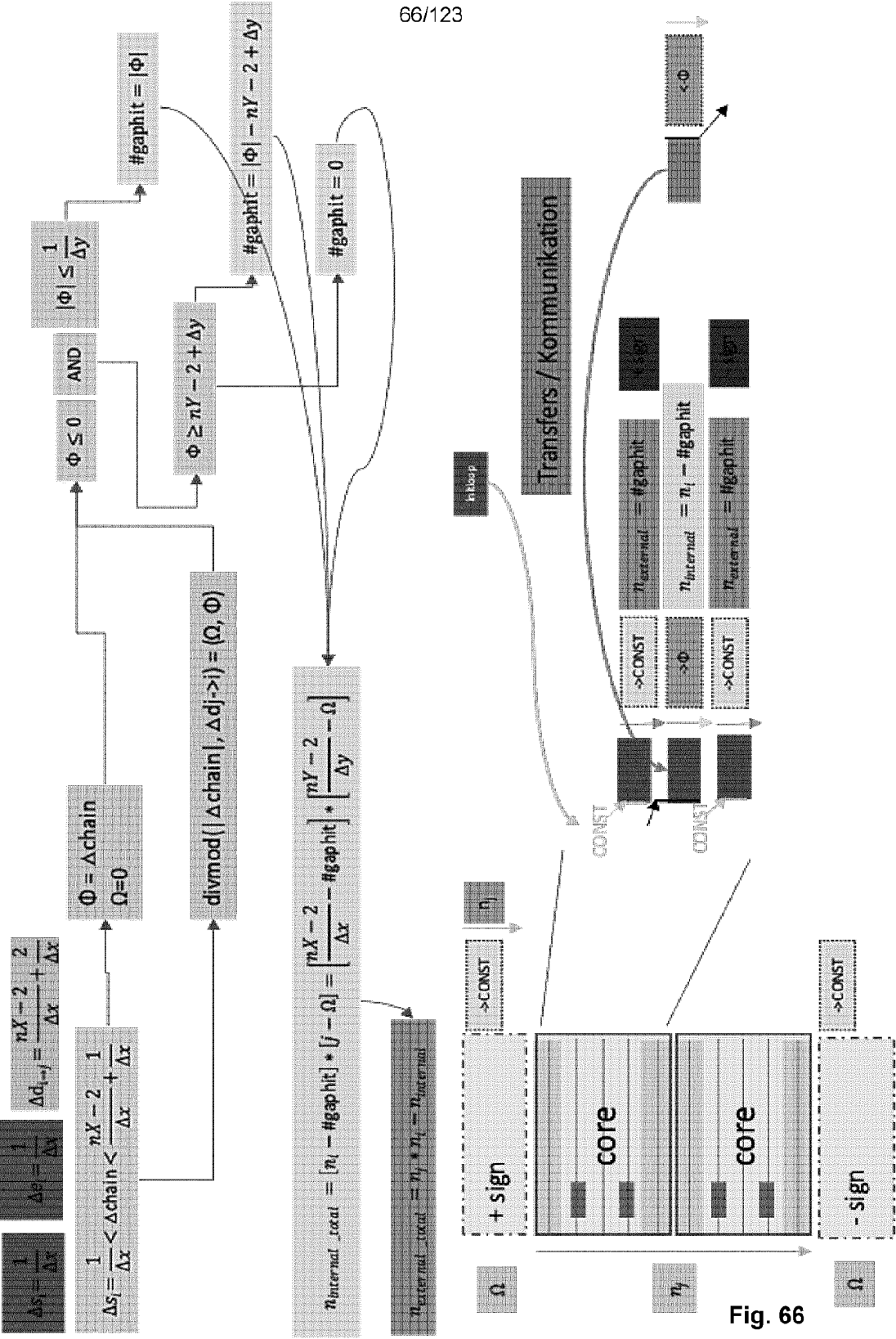


Fig. 66

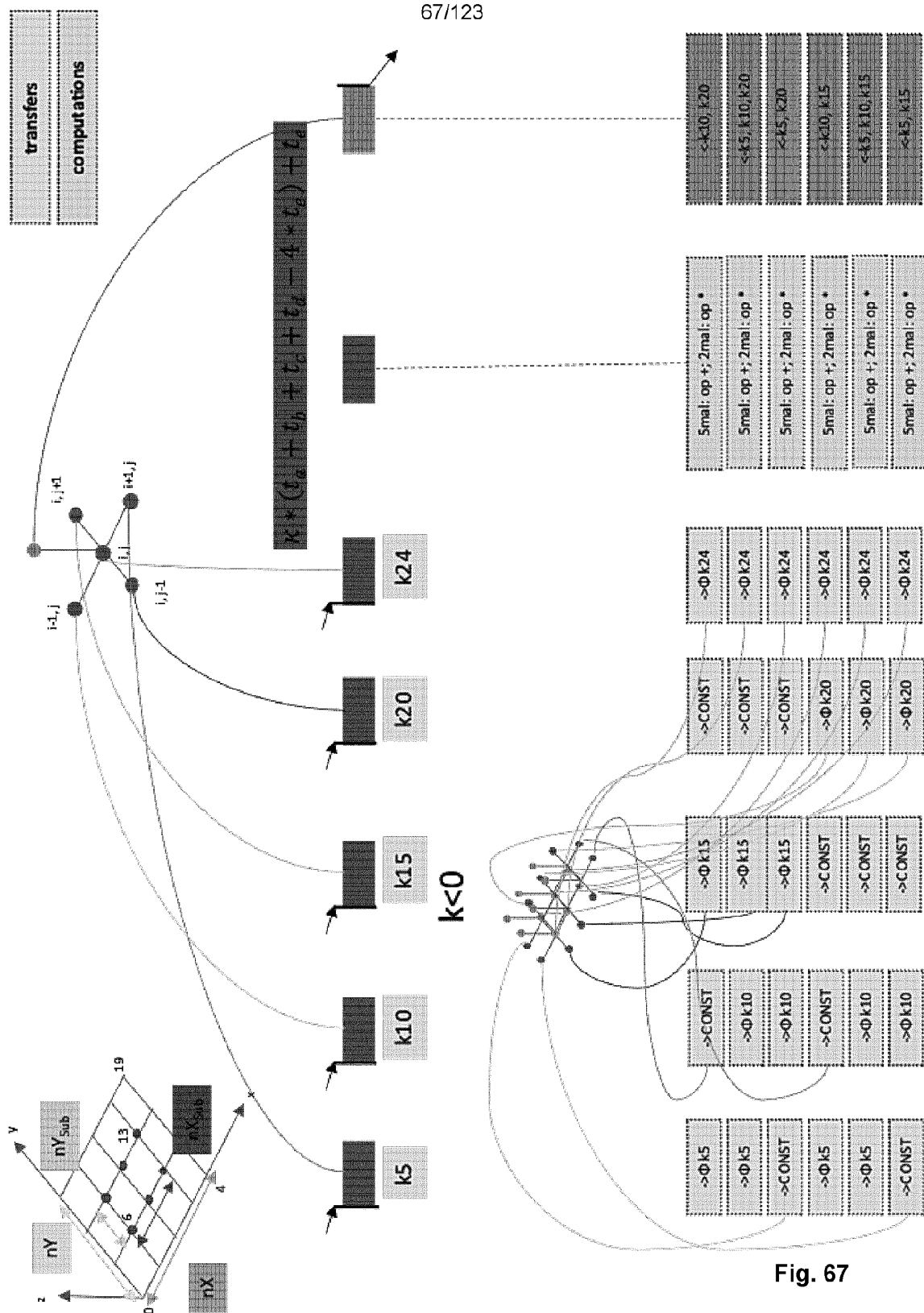


Fig. 67

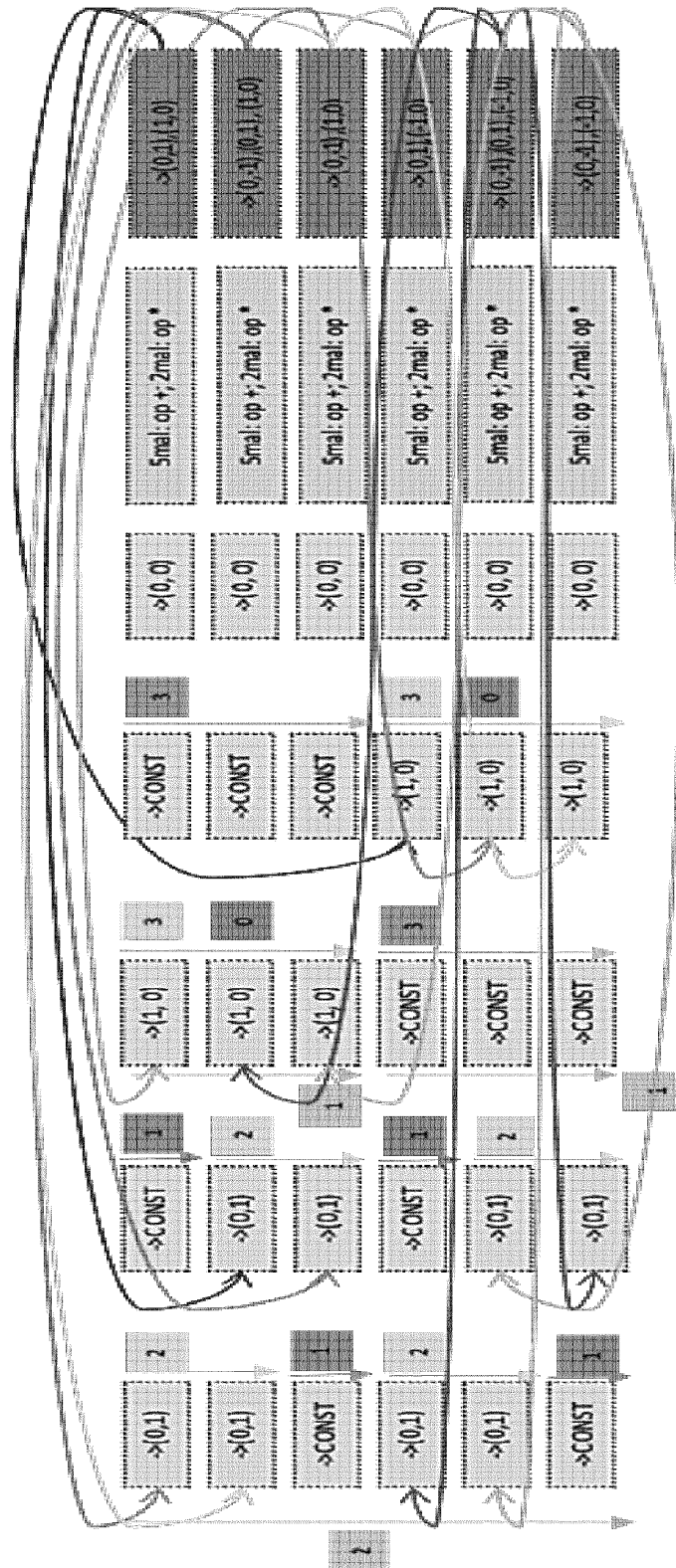


Fig. 68

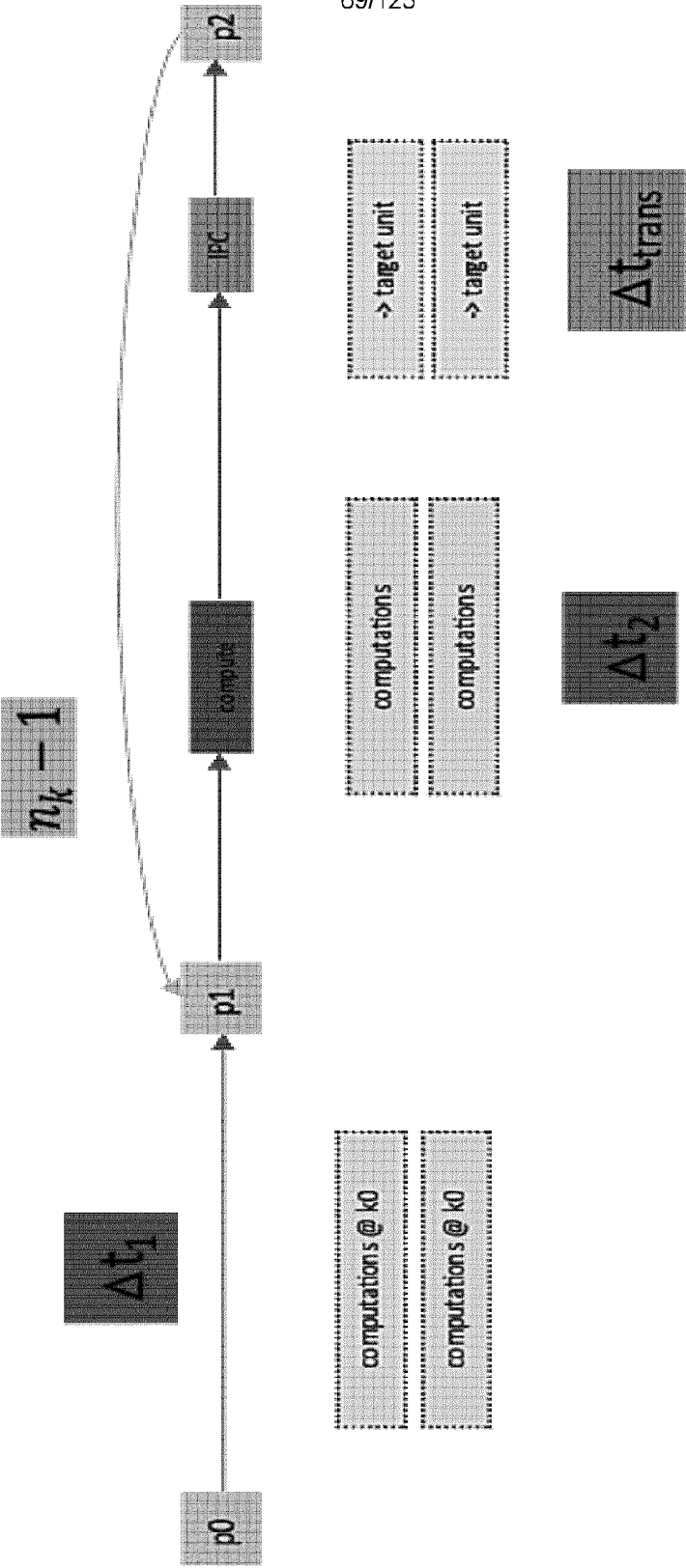


Fig. 69

2→1	0	4→1	0	1→1	5mal: op +; 2mal: op *	send:→2, →4
3→2	1→2	5→2	0	2→2	5mal: op +; 2mal: op *	send:→1, →3, →5
0	2→3	6→3	0	3→3	5mal: op +; 2mal: op *	send:→2, →6
5→4	0	0	1→4	4→4	5mal: op +; 2mal: op *	send:→4, →1
6→5	4→5	0	2→5	5→5	5mal: op +; 2mal: op *	send:→4, →6, →2
0	5→6	0	3→6	6→6	5mal: op +; 2mal: op *	send:→5, →3

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$$\begin{pmatrix} \Gamma \\ \Gamma \\ \Gamma \\ \Gamma \\ \Gamma \\ \Gamma \end{pmatrix} \cdot \Delta t_{latency}$$

$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \cdot \Delta t_{trans}$$

$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ 1 \rightarrow 4 \\ 2 \rightarrow 5 \\ 3 \rightarrow 6 \end{pmatrix} \cdot \Delta t_{trans}$$

$$\begin{pmatrix} 4 \rightarrow 1 \\ 5 \rightarrow 2 \\ 6 \rightarrow 3 \\ 0 \\ 0 \\ 0 \end{pmatrix} \cdot \Delta t_{trans}$$

$$\begin{pmatrix} 0 \\ 1 \rightarrow 2 \\ 2 \rightarrow 3 \\ 0 \\ 4 \rightarrow 5 \\ 5 \rightarrow 6 \end{pmatrix} \cdot \Delta t_{trans}$$

$$\begin{pmatrix} 2 \rightarrow 1 \\ 3 \rightarrow 2 \\ 0 \\ 5 \rightarrow 4 \\ 6 \rightarrow 4 \\ 0 \end{pmatrix} \cdot \Delta t_{trans}$$

$$\Gamma = 5 + 2 \cdot *$$

$$\frac{trans_size}{float_size} =$$

$$cache_size = \begin{pmatrix} 6 \\ 6 \\ 6 \\ 6 \\ 6 \\ 6 \end{pmatrix} float_size$$

meta-values

Fig. 70

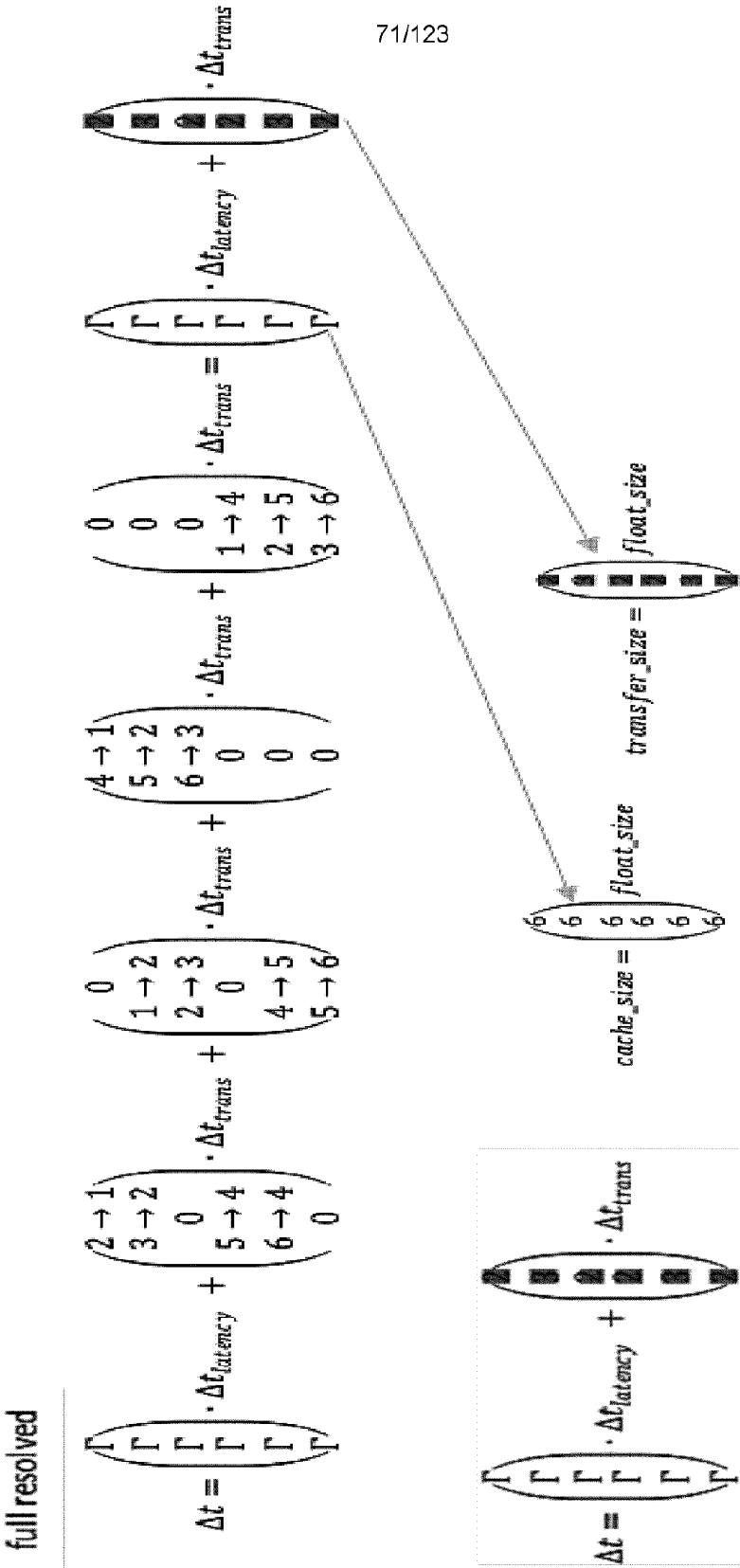


Fig. 71

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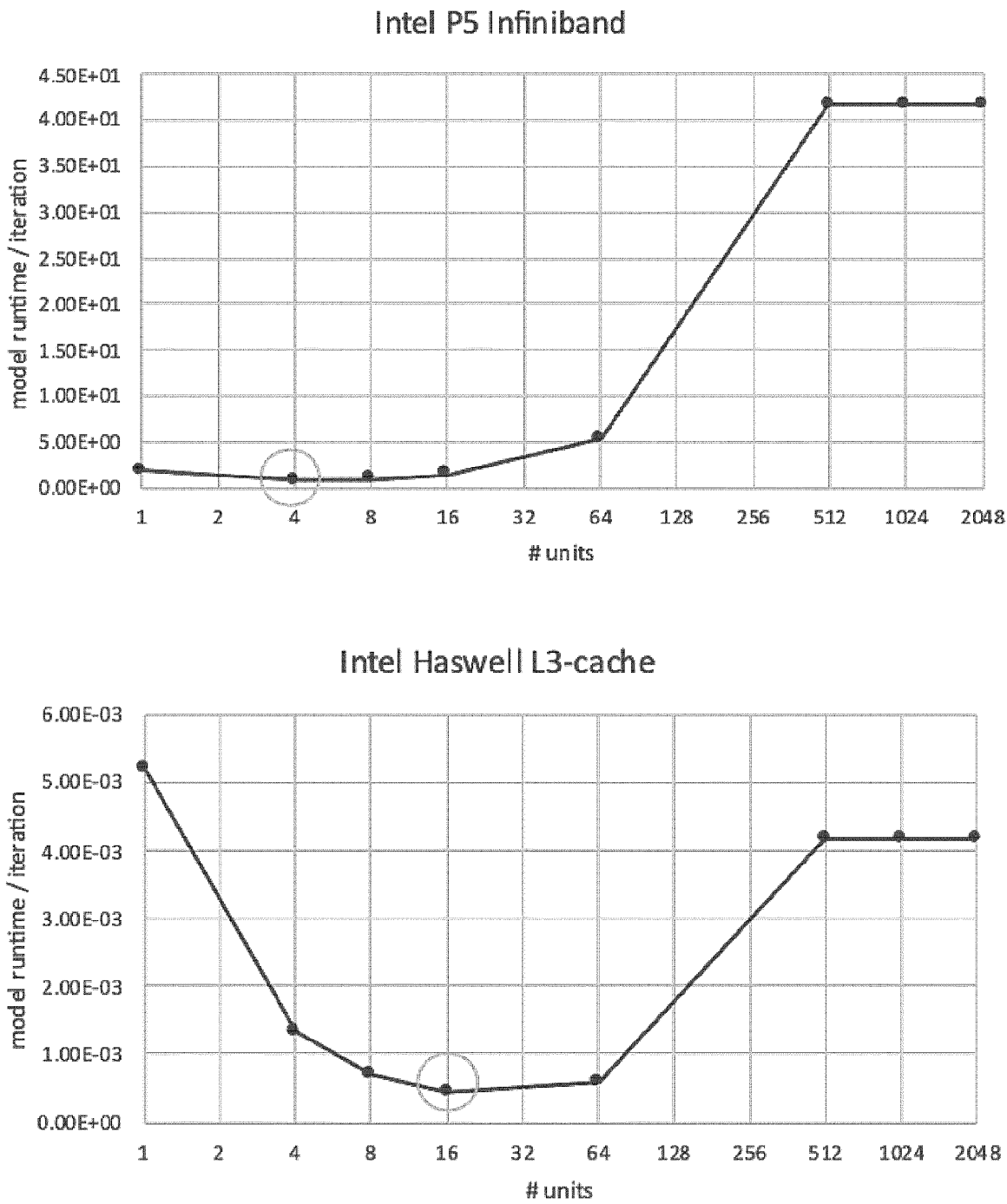


Fig. 72

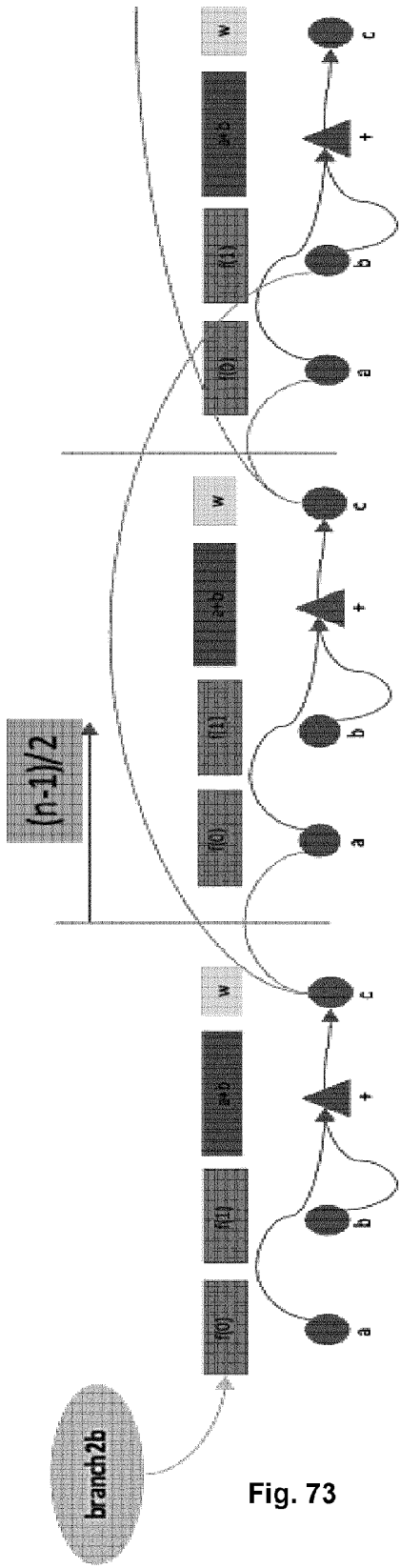
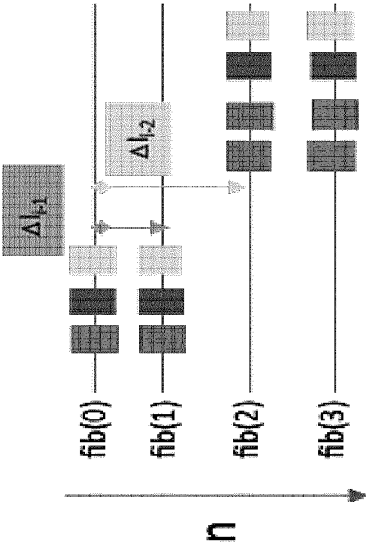


Fig. 73

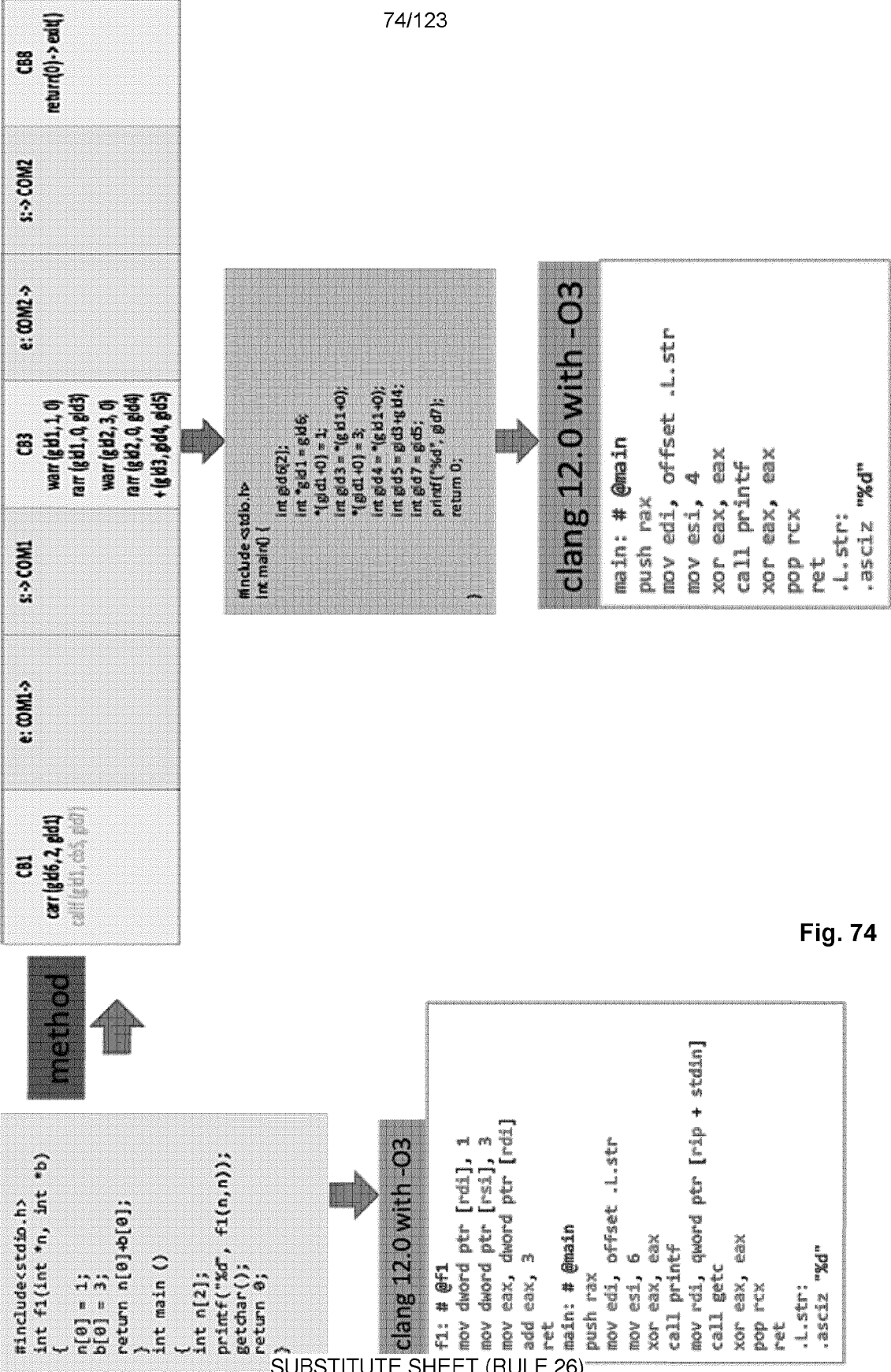


Fig. 74

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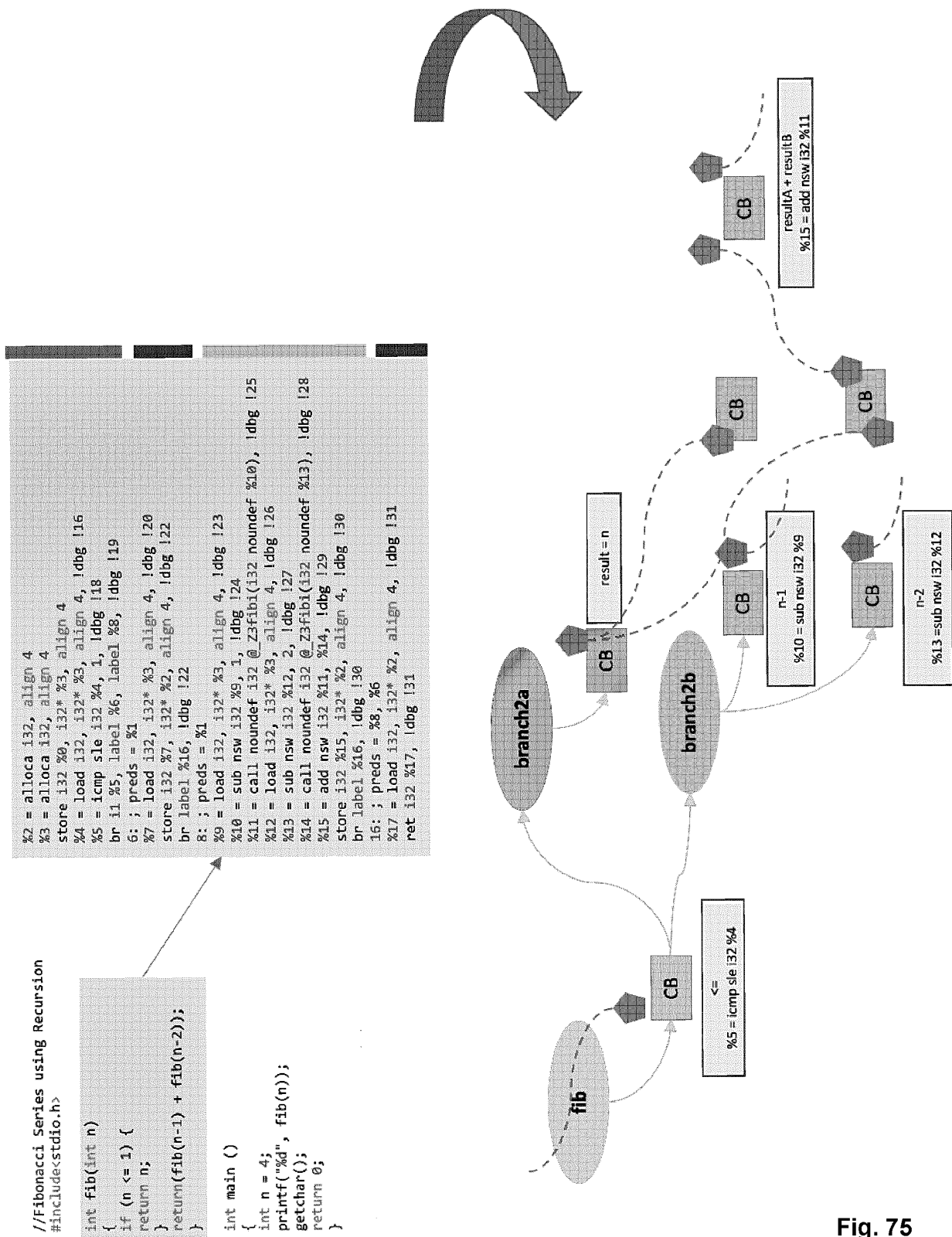


Fig. 75

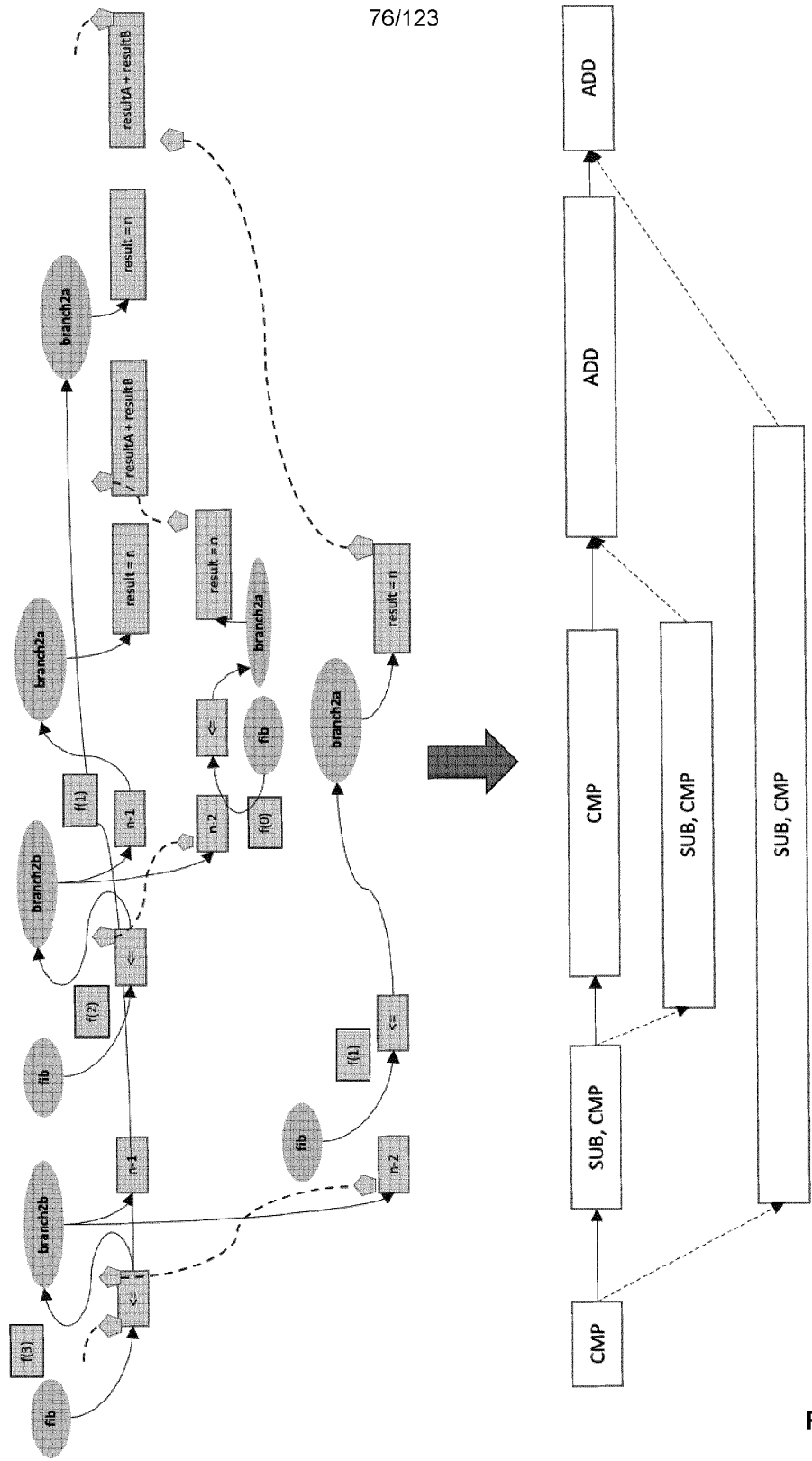


Fig. 76

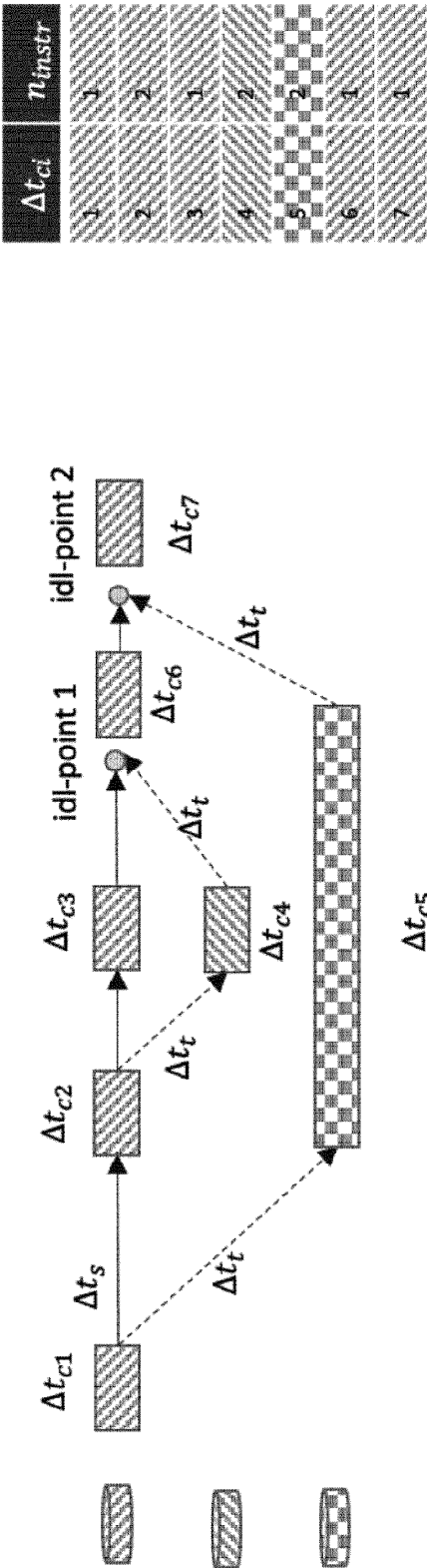


Fig. 77

Δt_{ci}	n_{instr}
1	1
2	2
3	1
4	2
5	2
6	1
7	1

Δt_{ci}	n_{instr}
1	5
3	1
4	2
6	2

Δt_{ci}	n_{instr}
1	1
2	6
5	2
7	1

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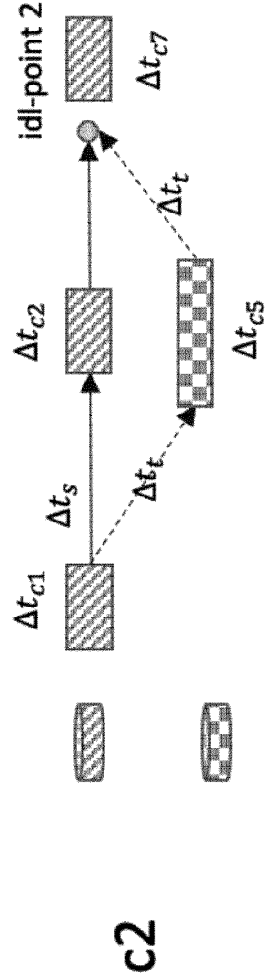
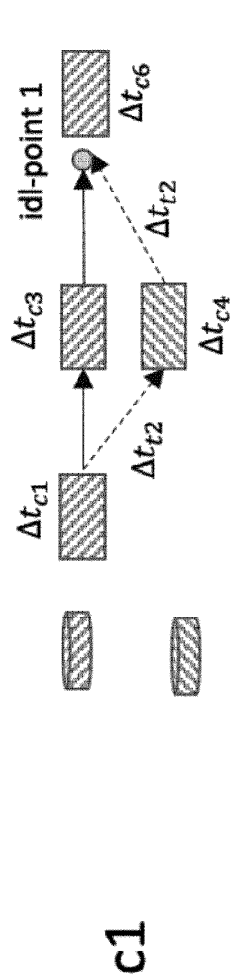


Fig. 78

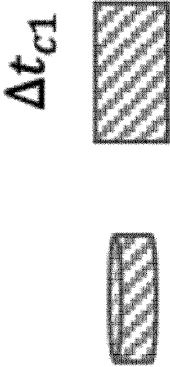
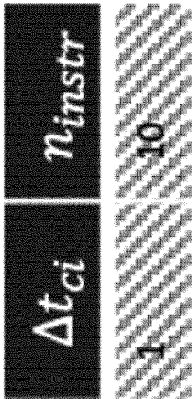


Fig. 79

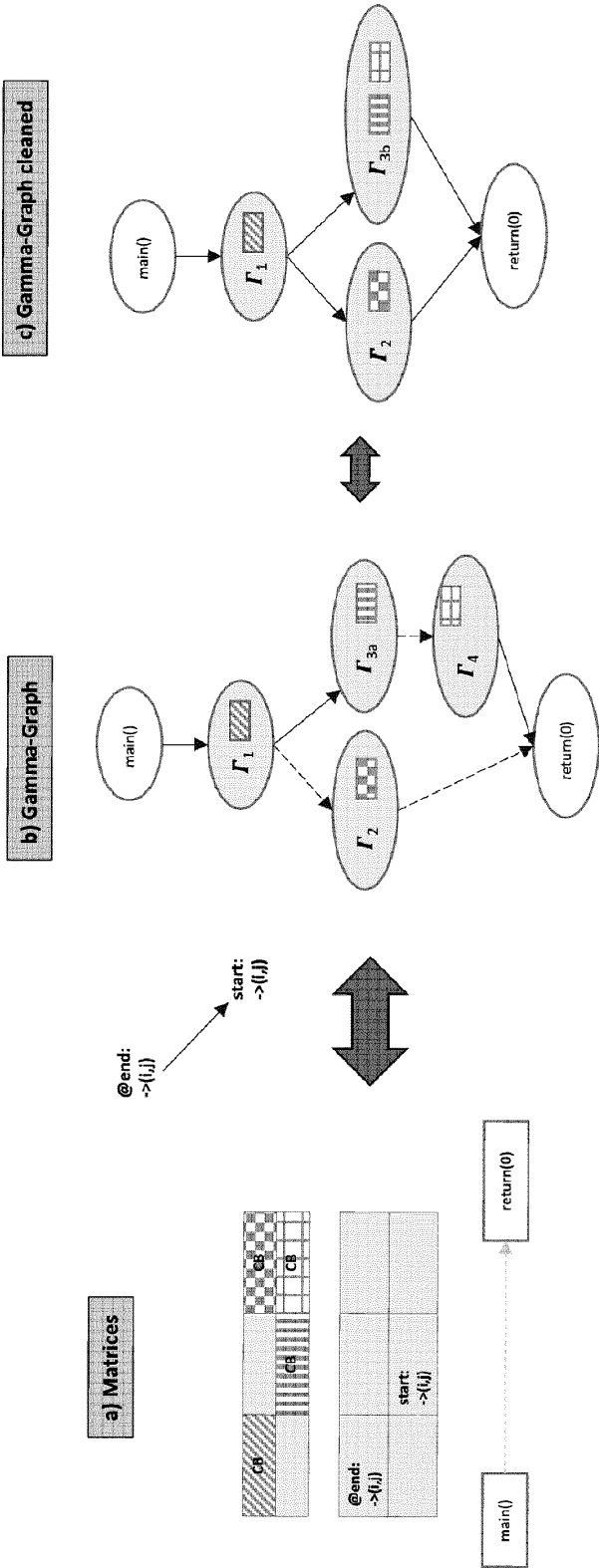


Fig. 80

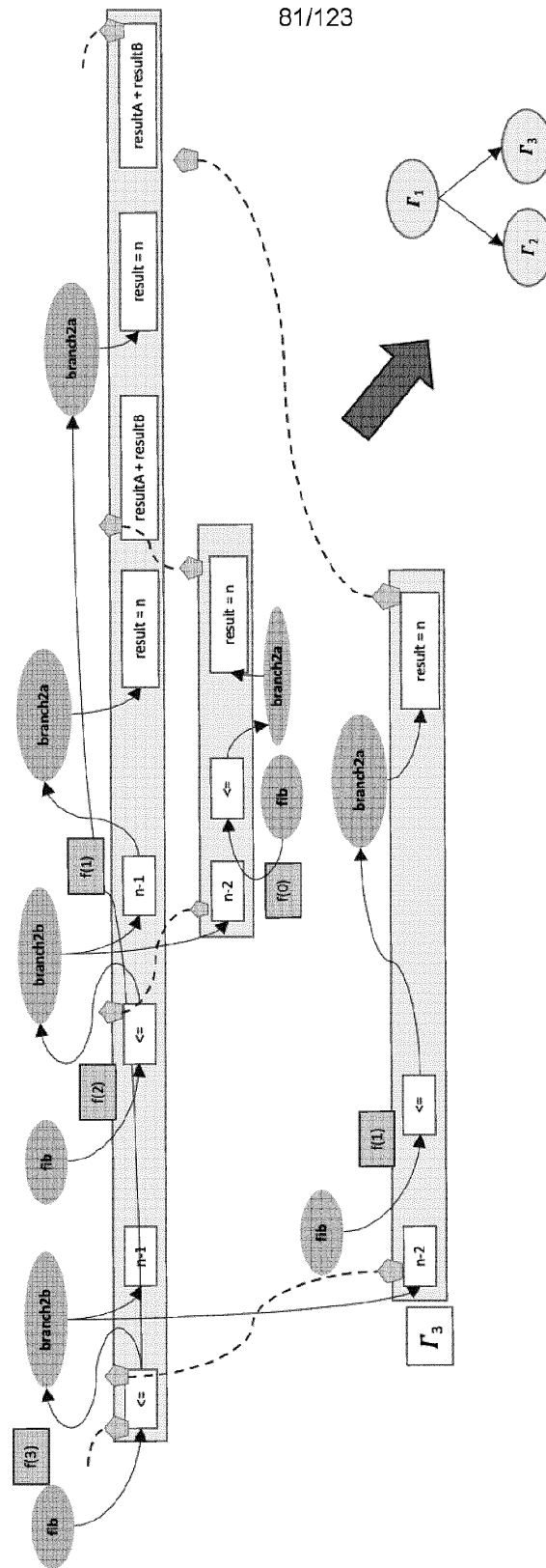


Fig. 81

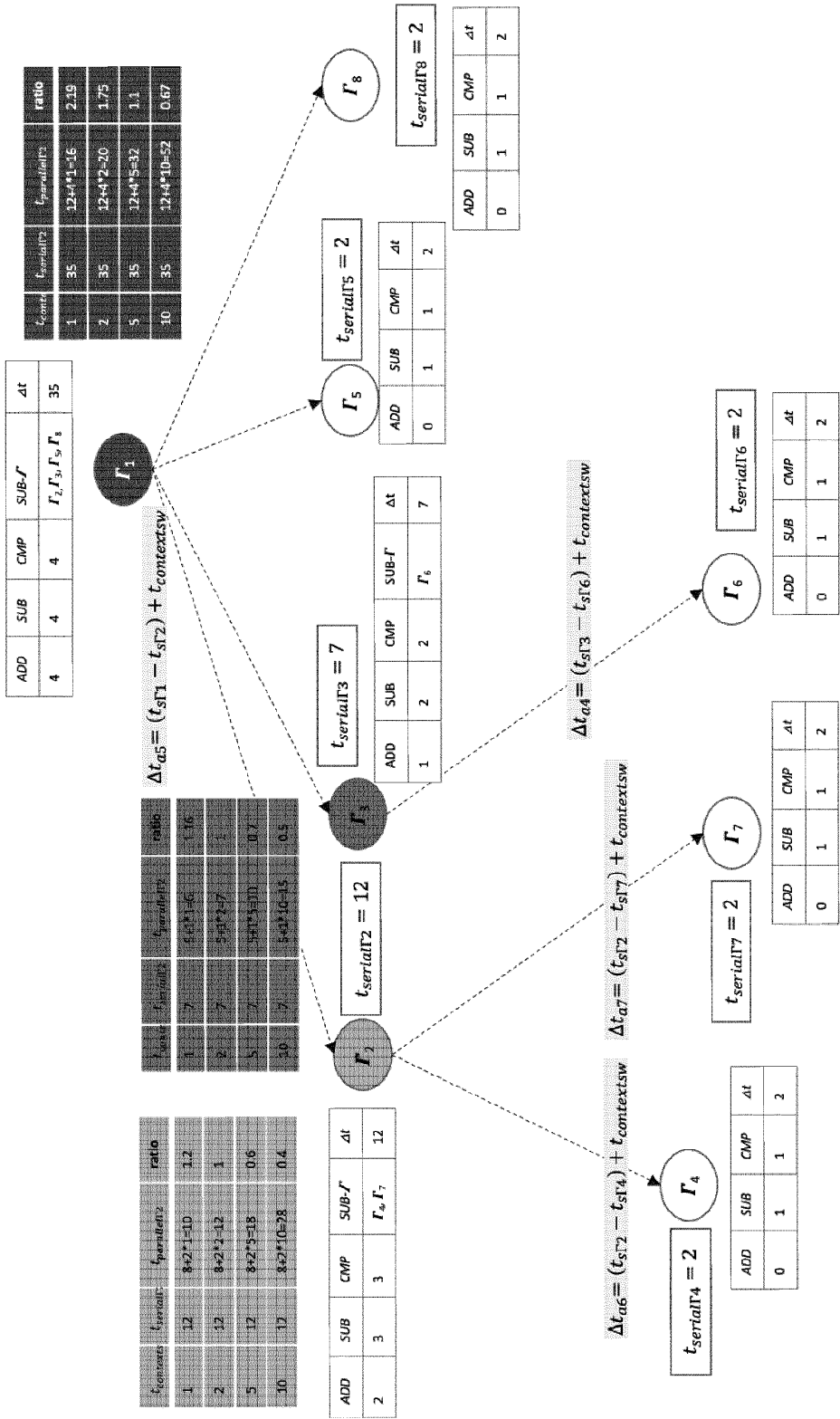


Fig. 82

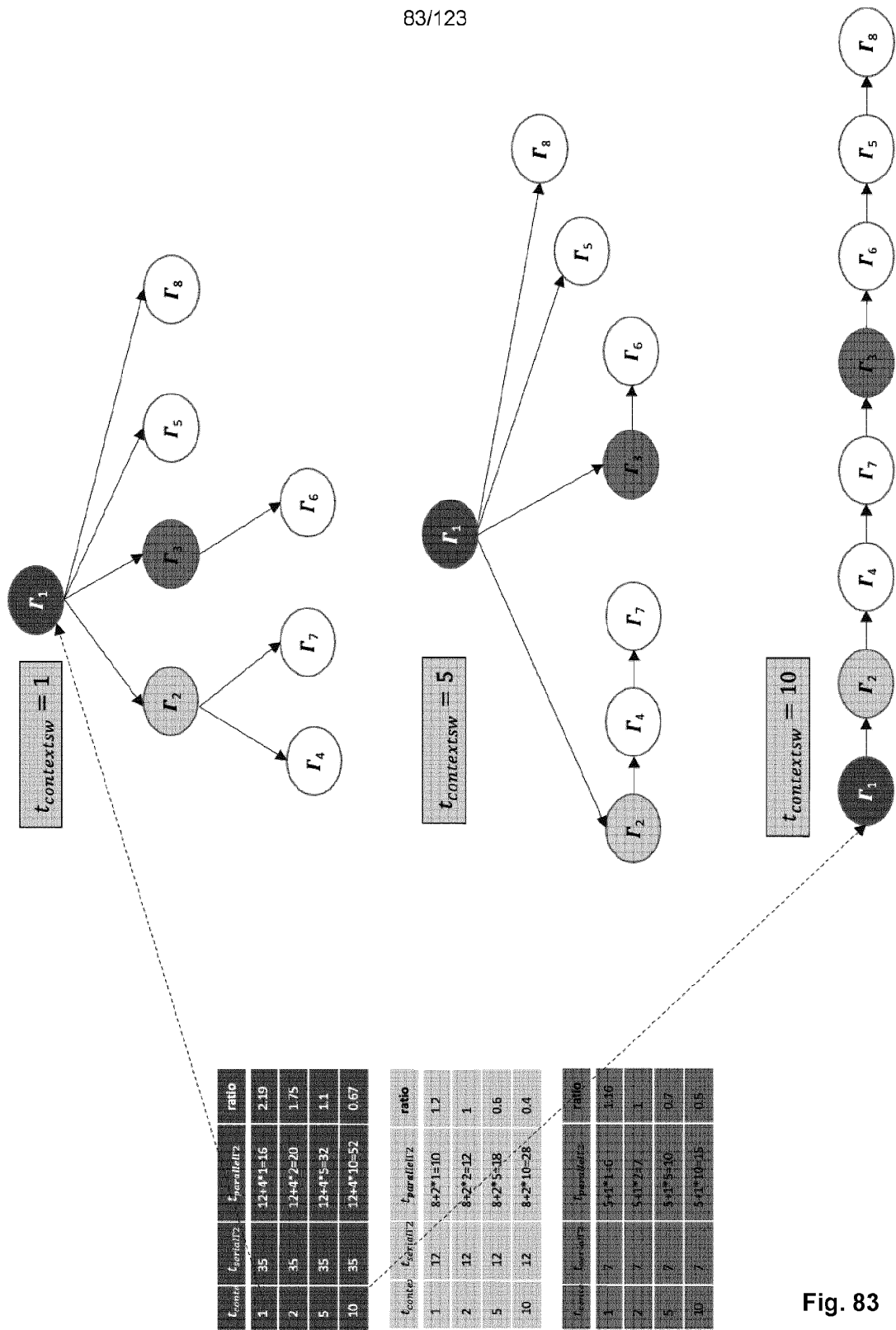


Fig. 83

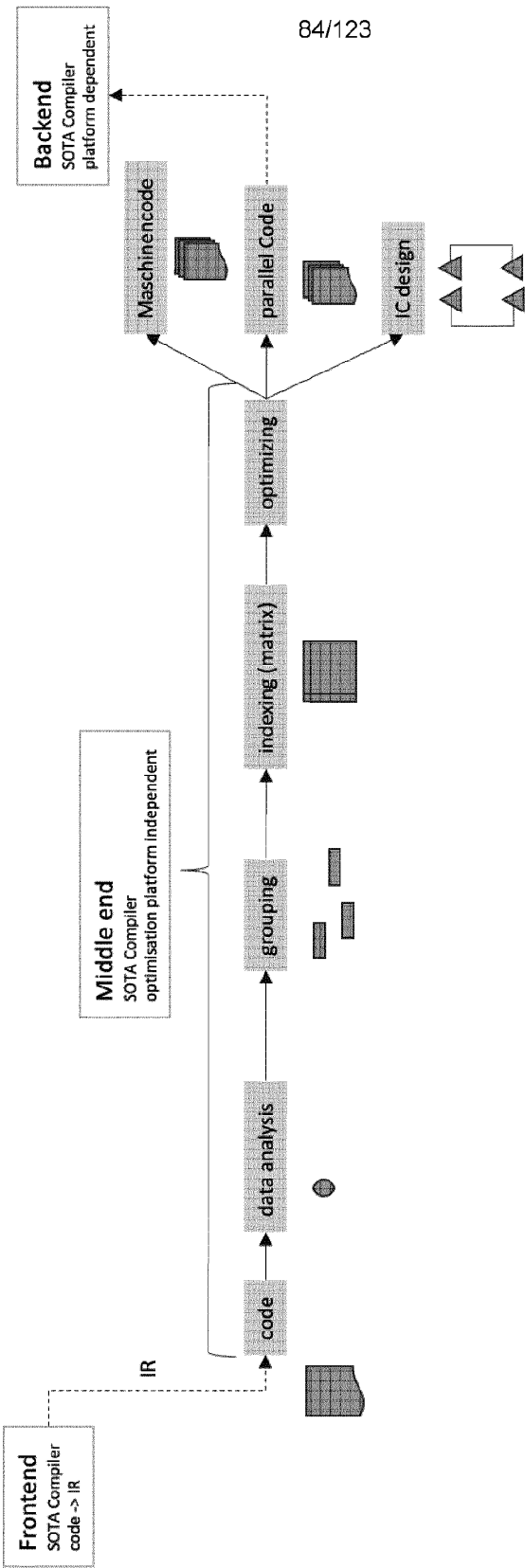


Fig. 84

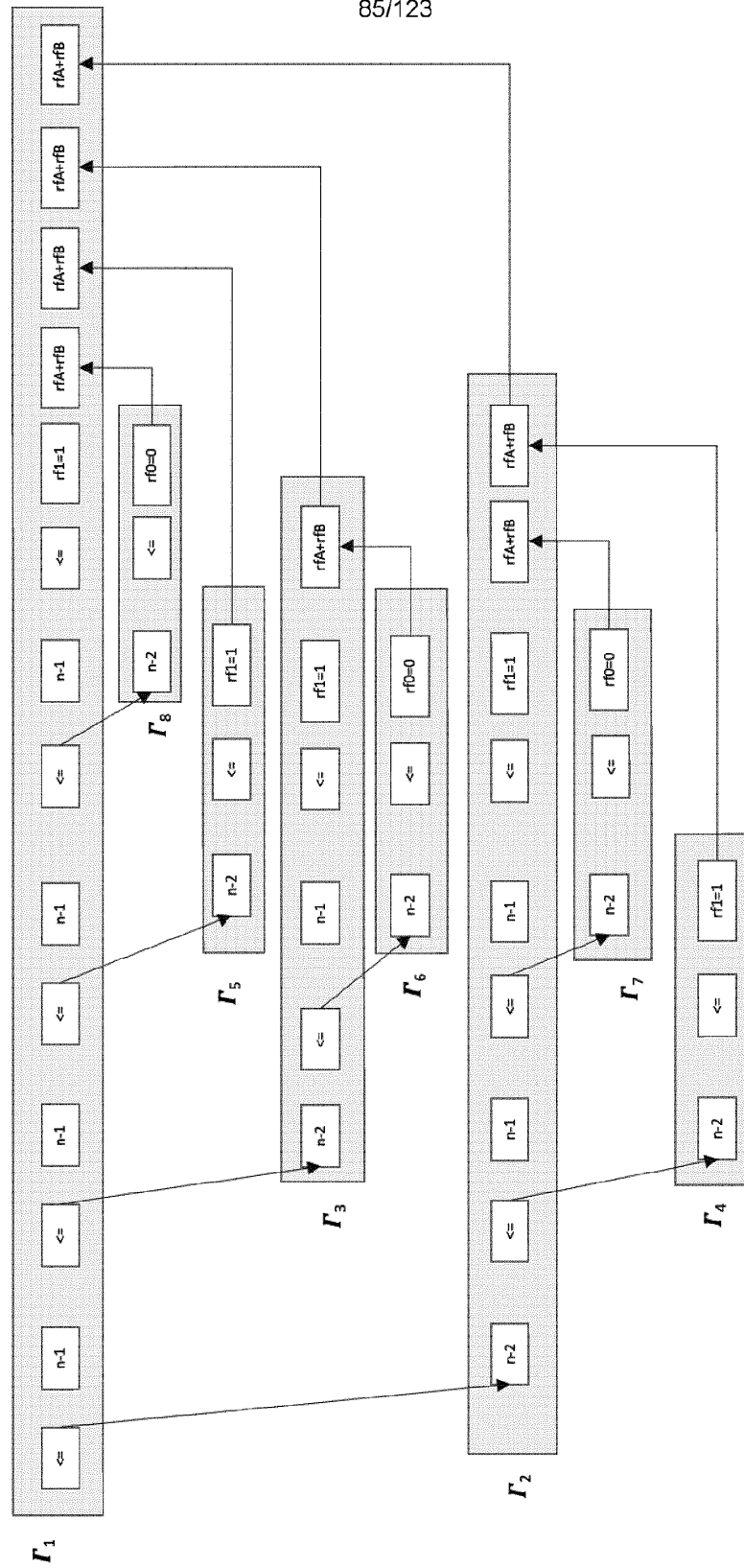


Fig. 85

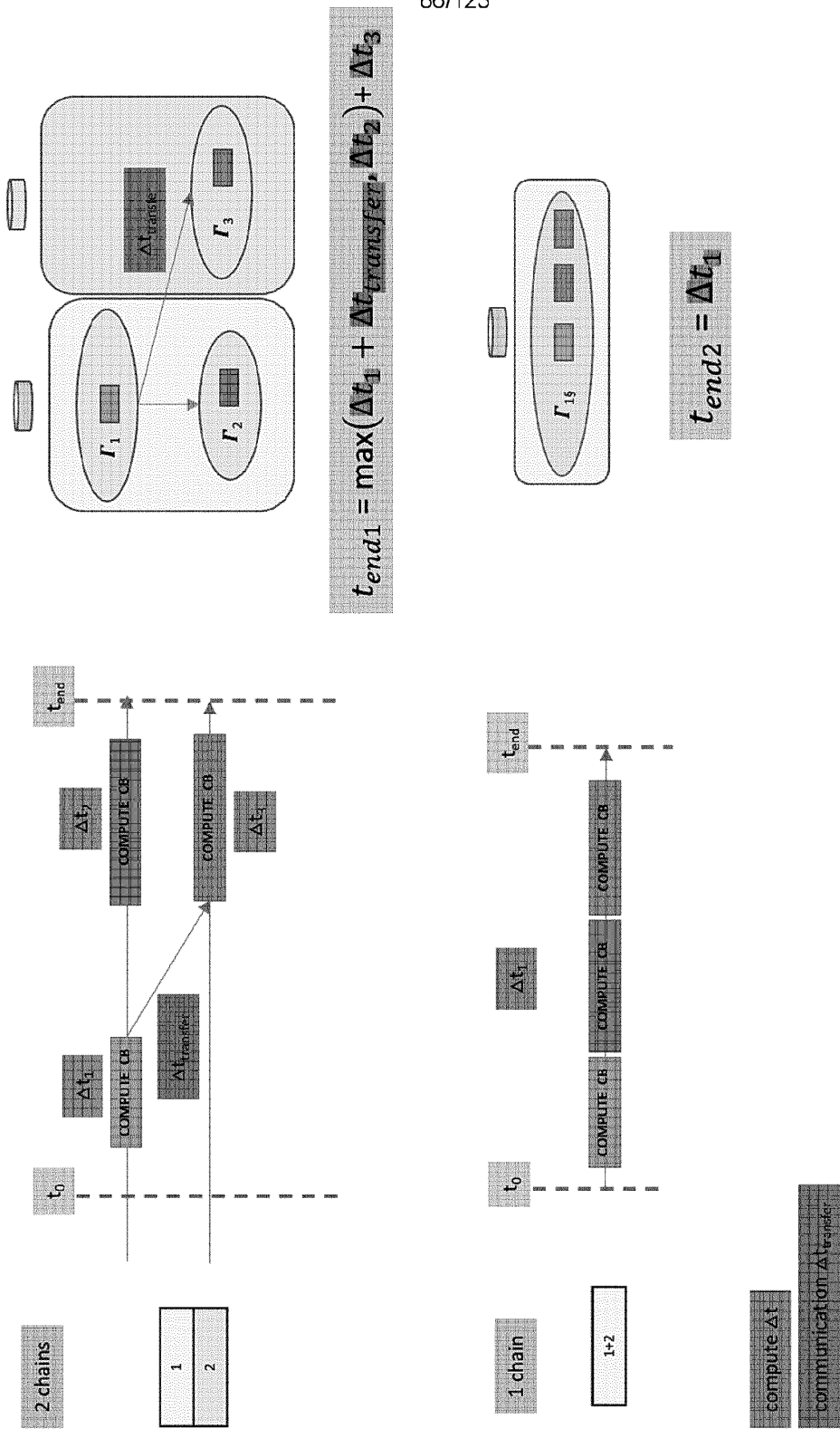


Fig. 86

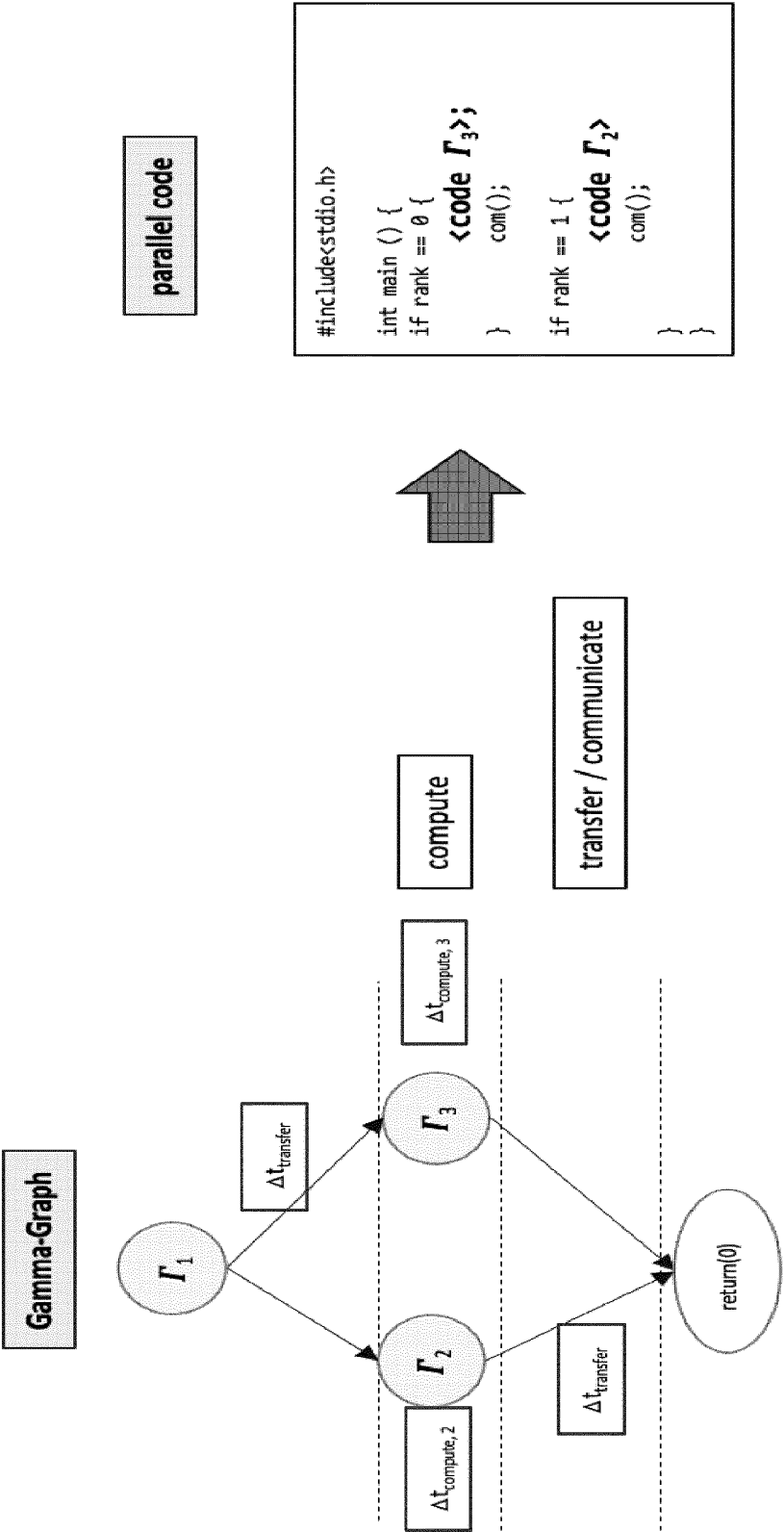


Fig. 87

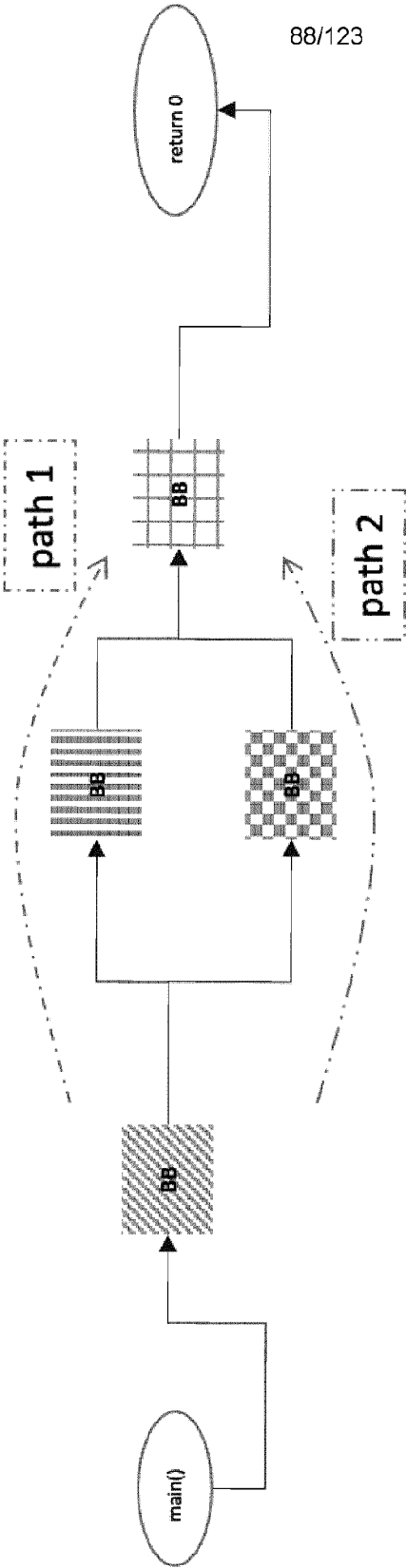


Fig. 88

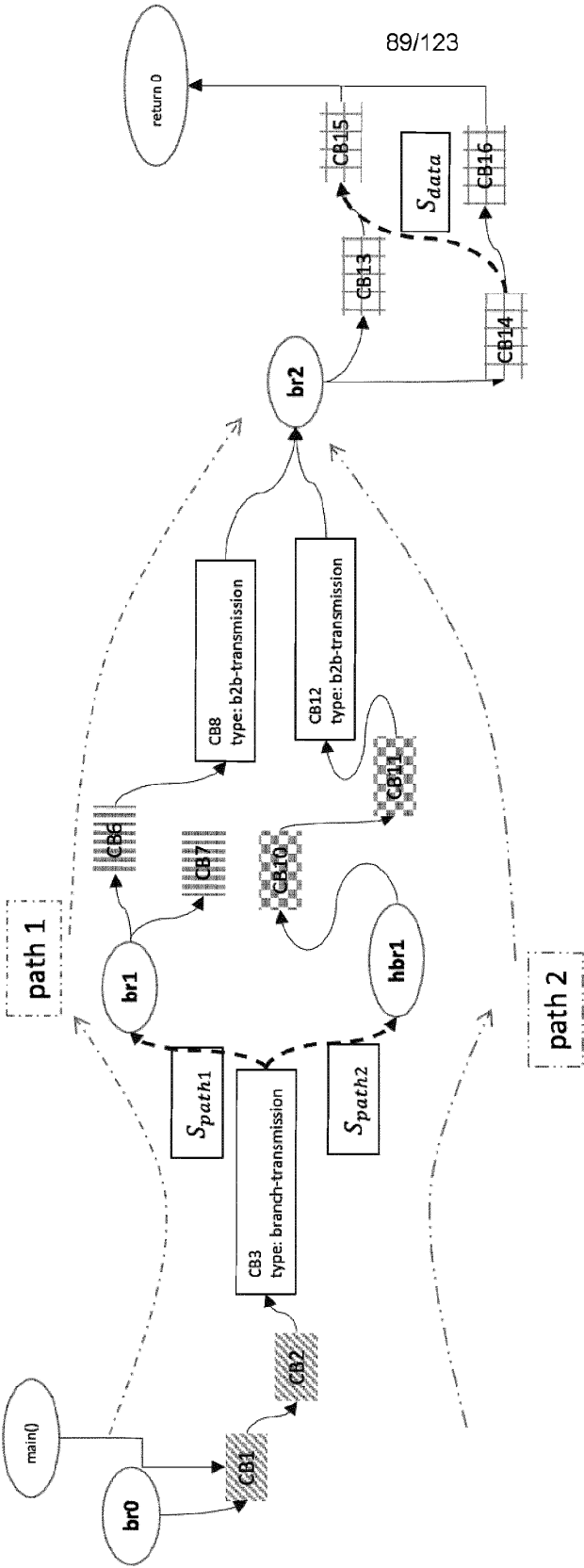


Fig. 89

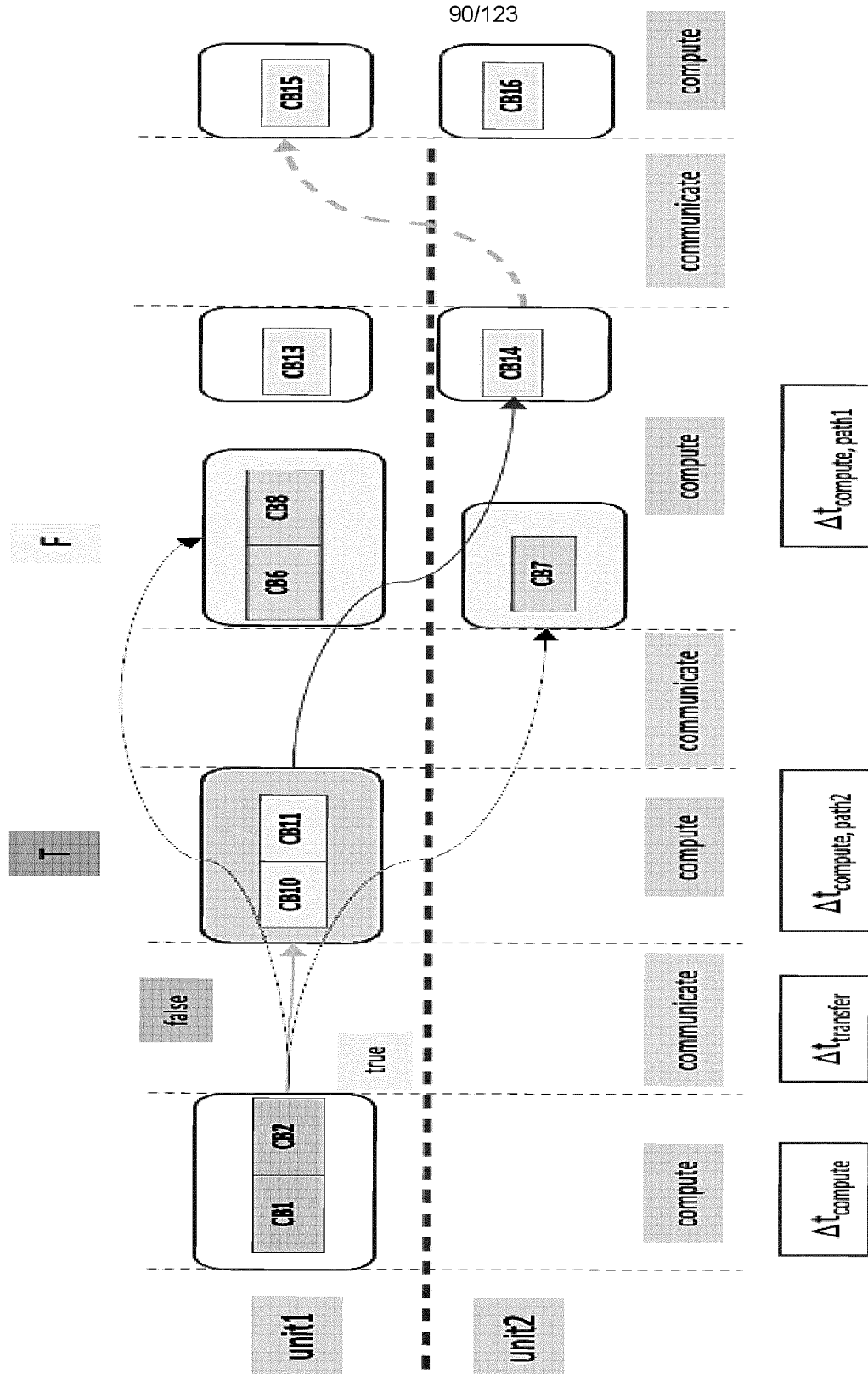


Fig. 90

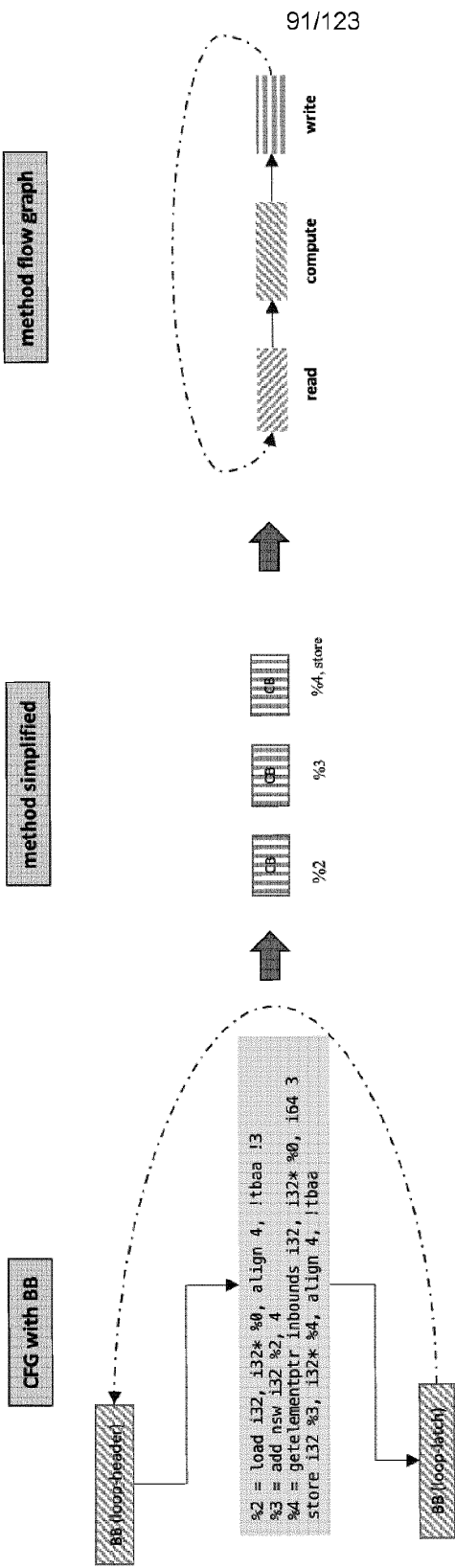


Fig. 91

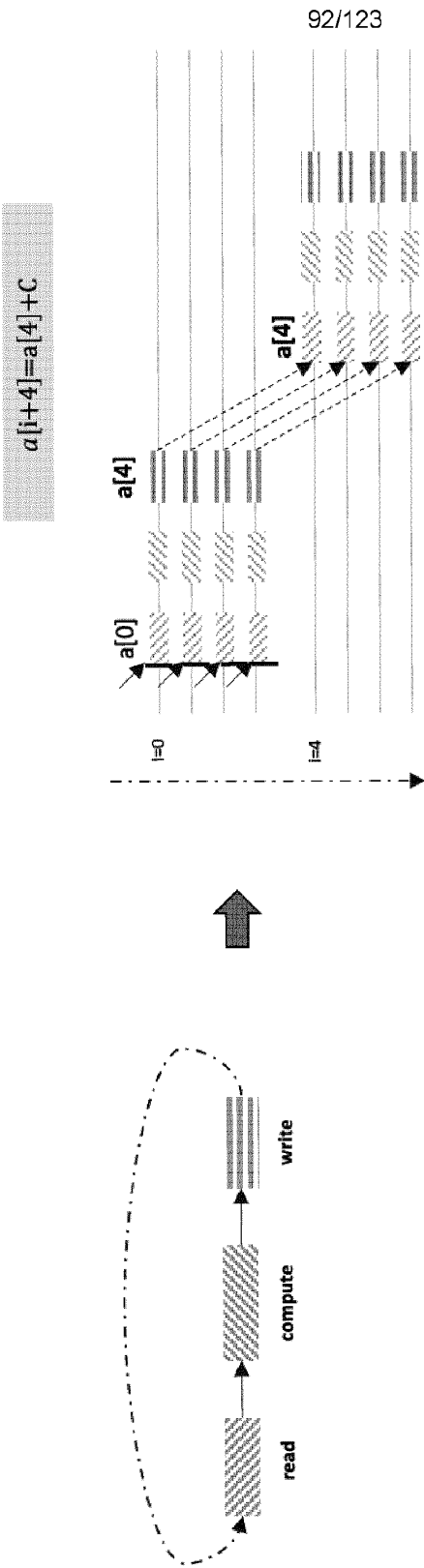


Fig. 92

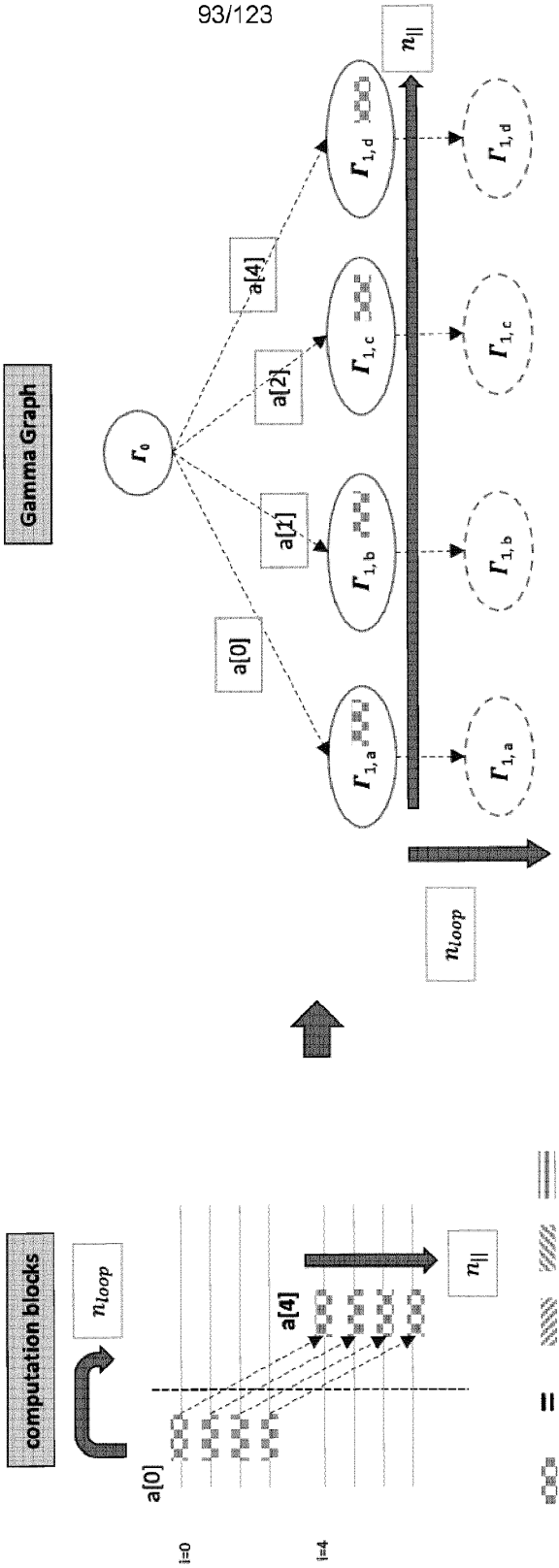


Fig. 93

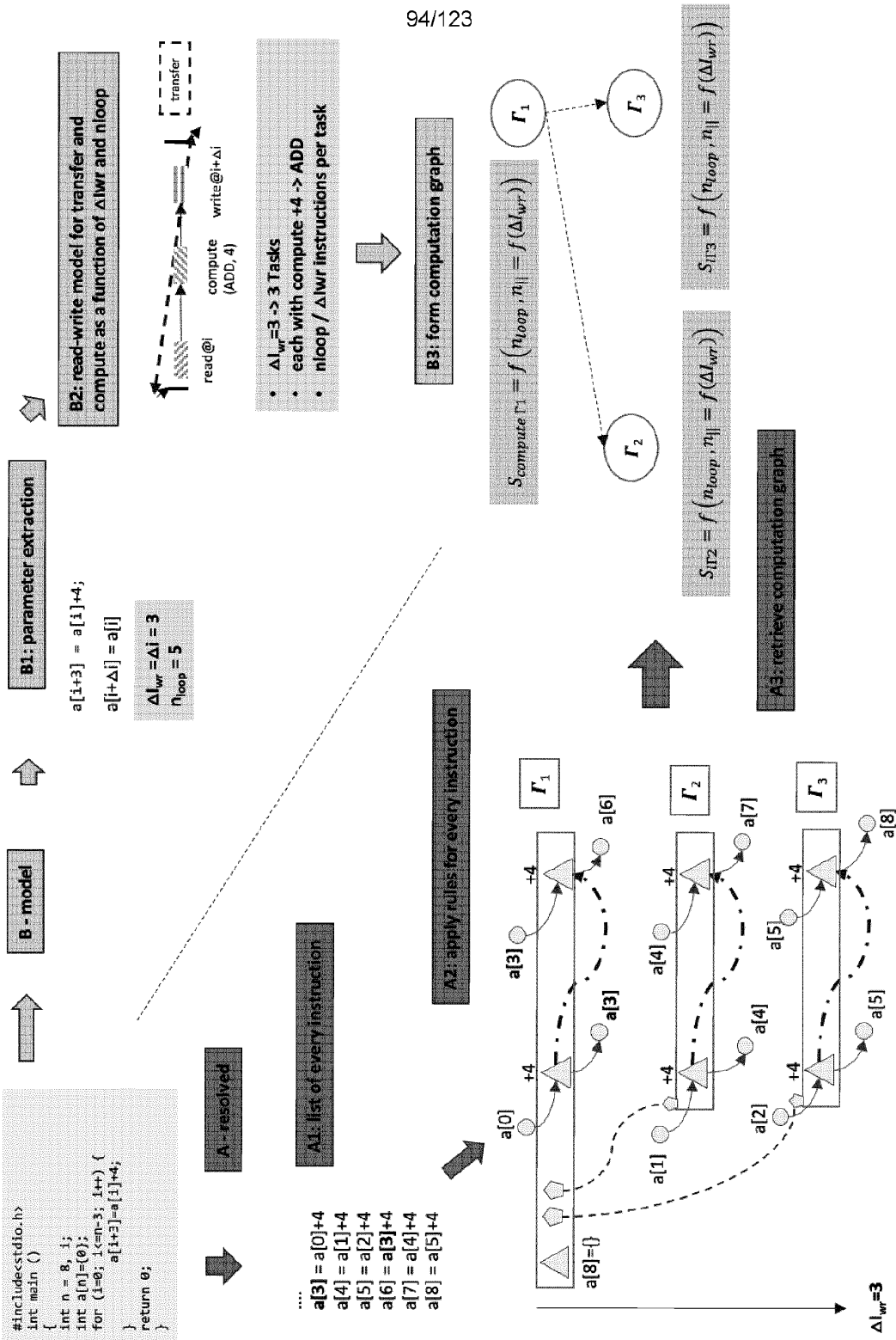


Fig. 94

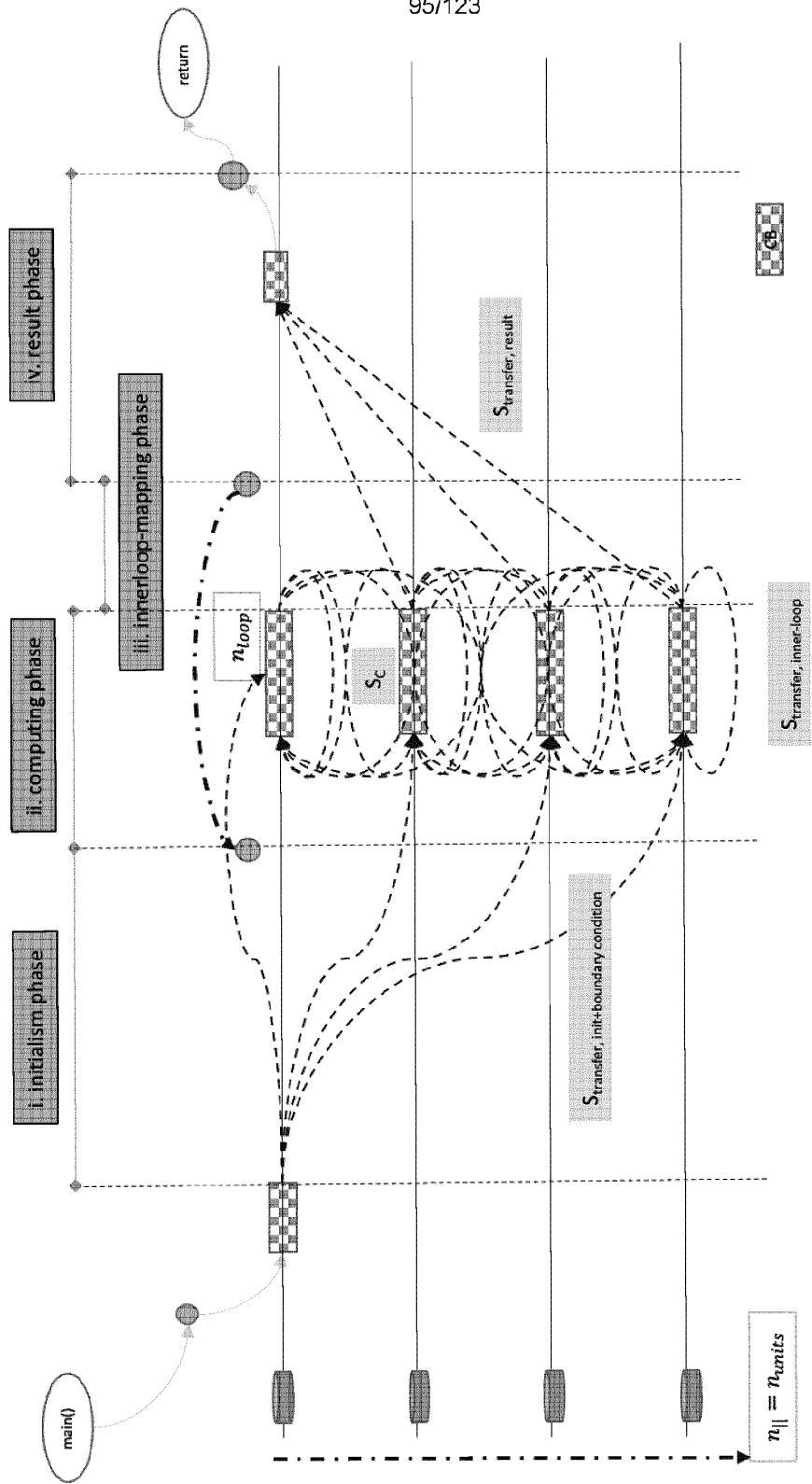


Fig. 95

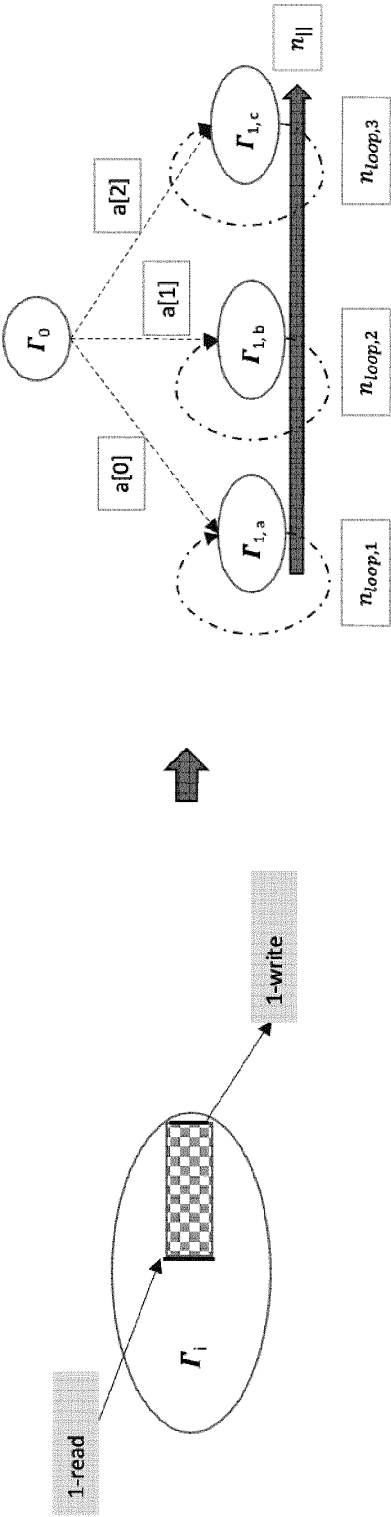


Fig. 96

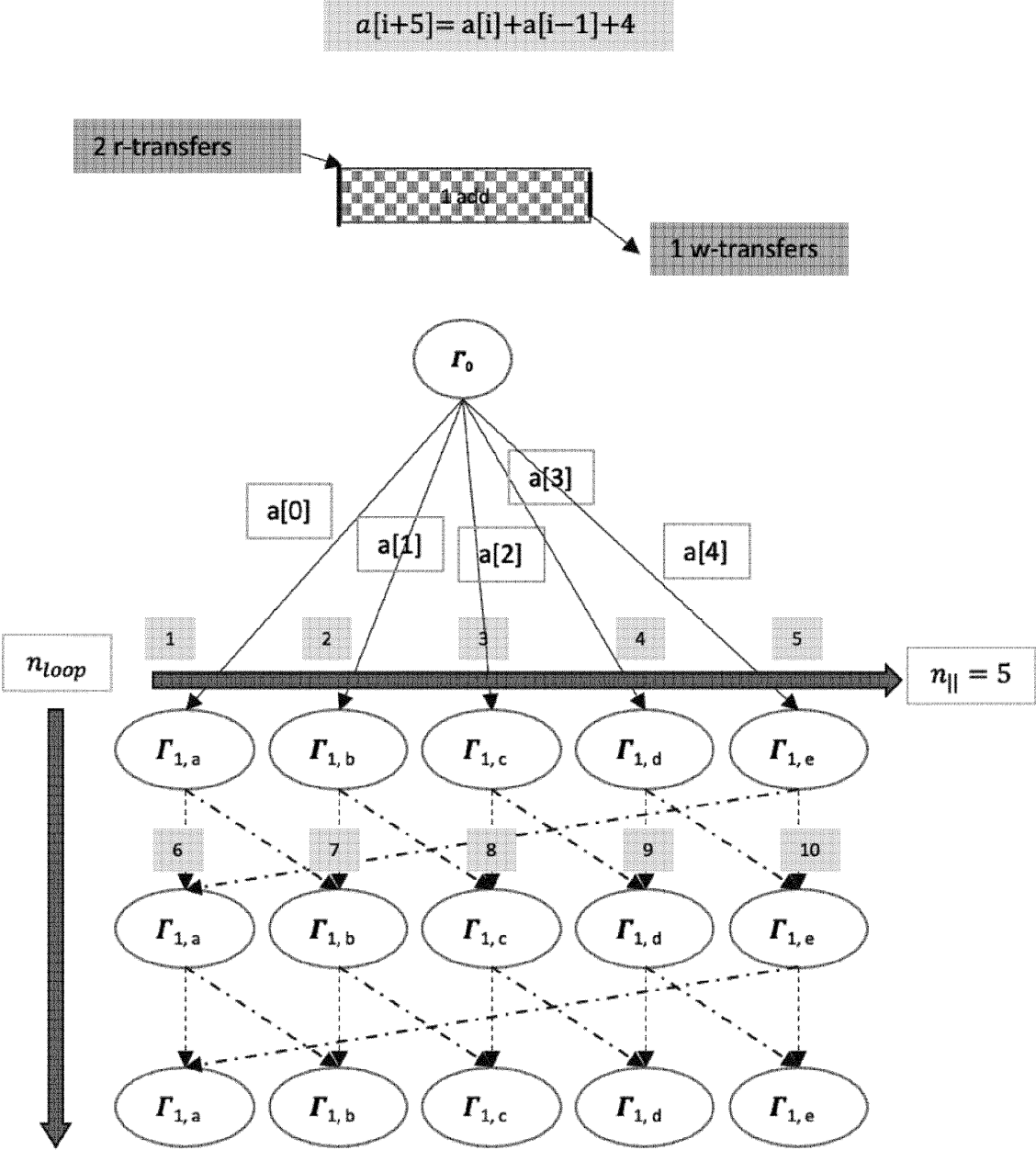


Fig. 97

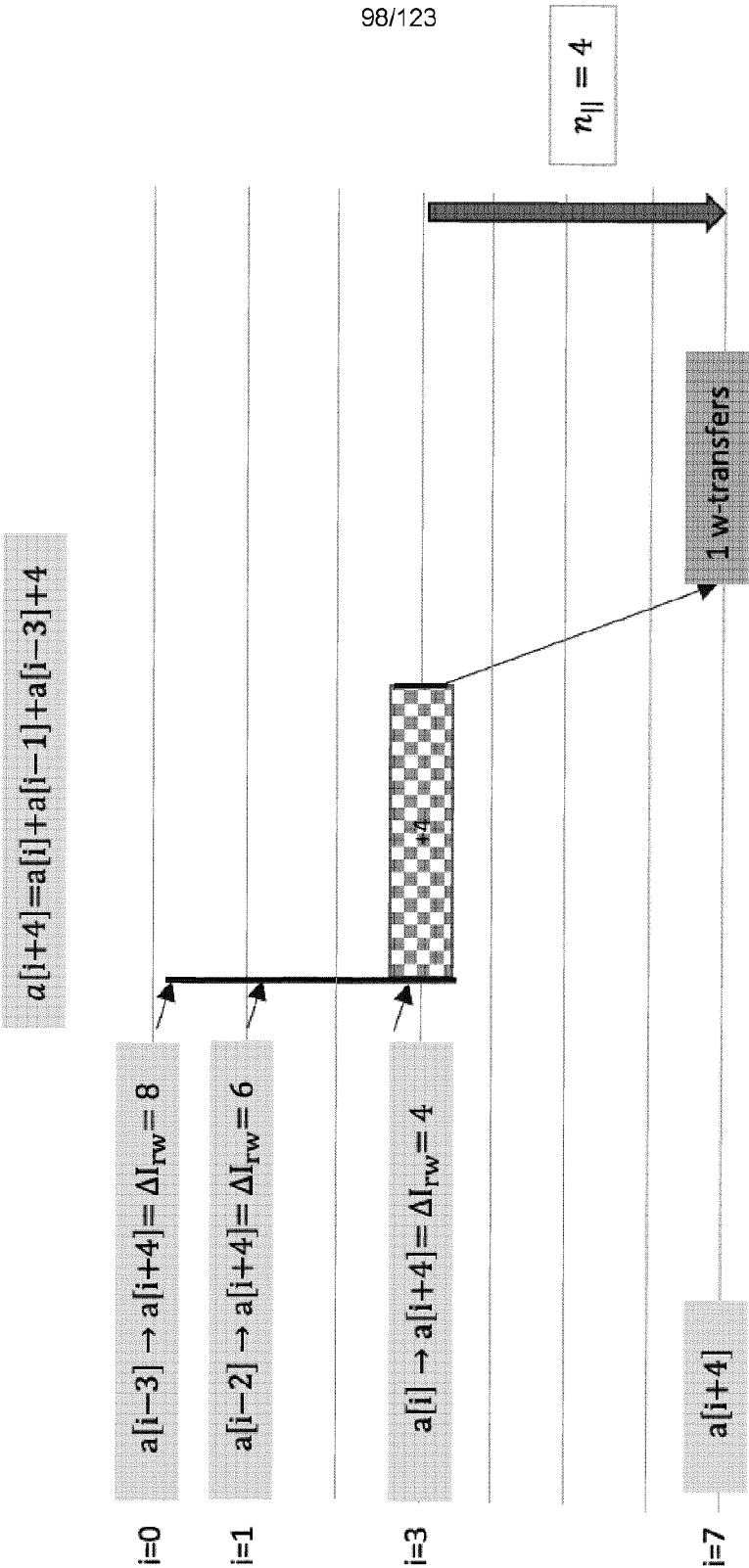


Fig. 98

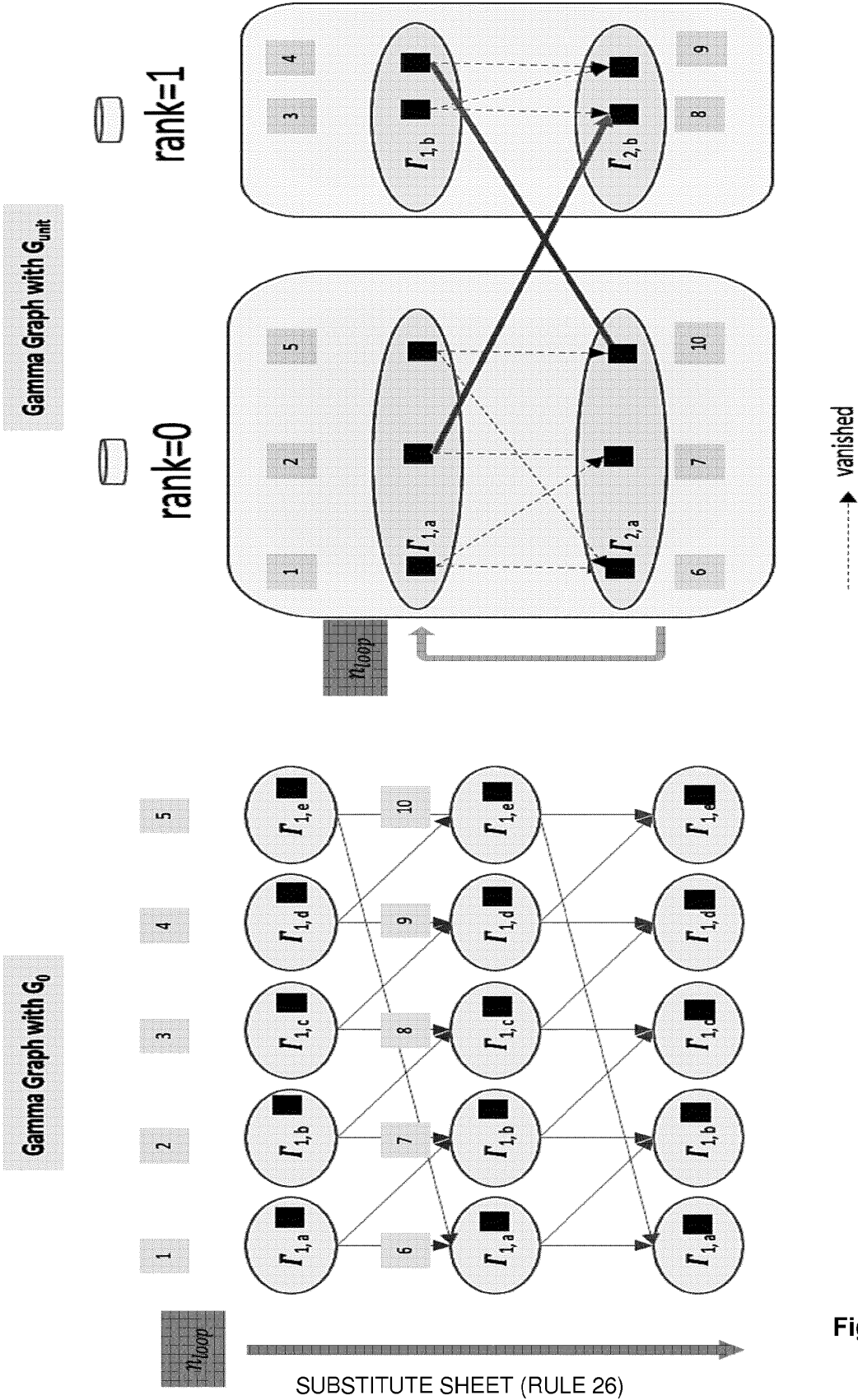


Fig. 99

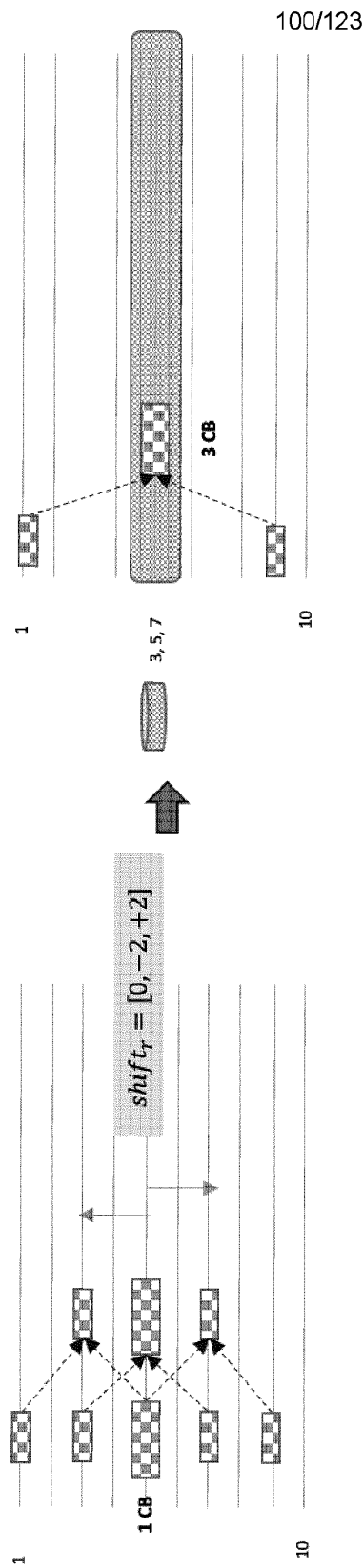


Fig. 100

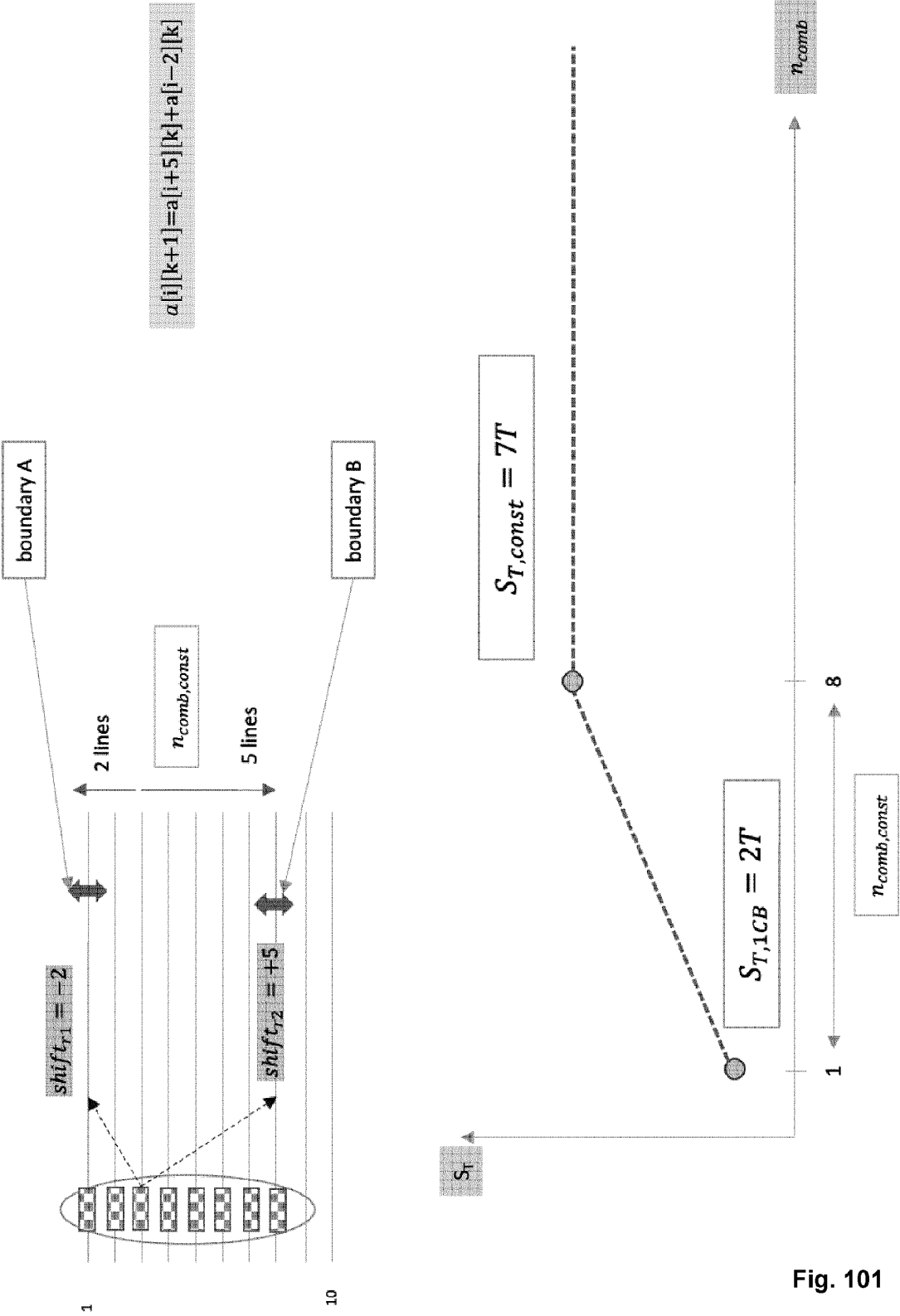


Fig. 101

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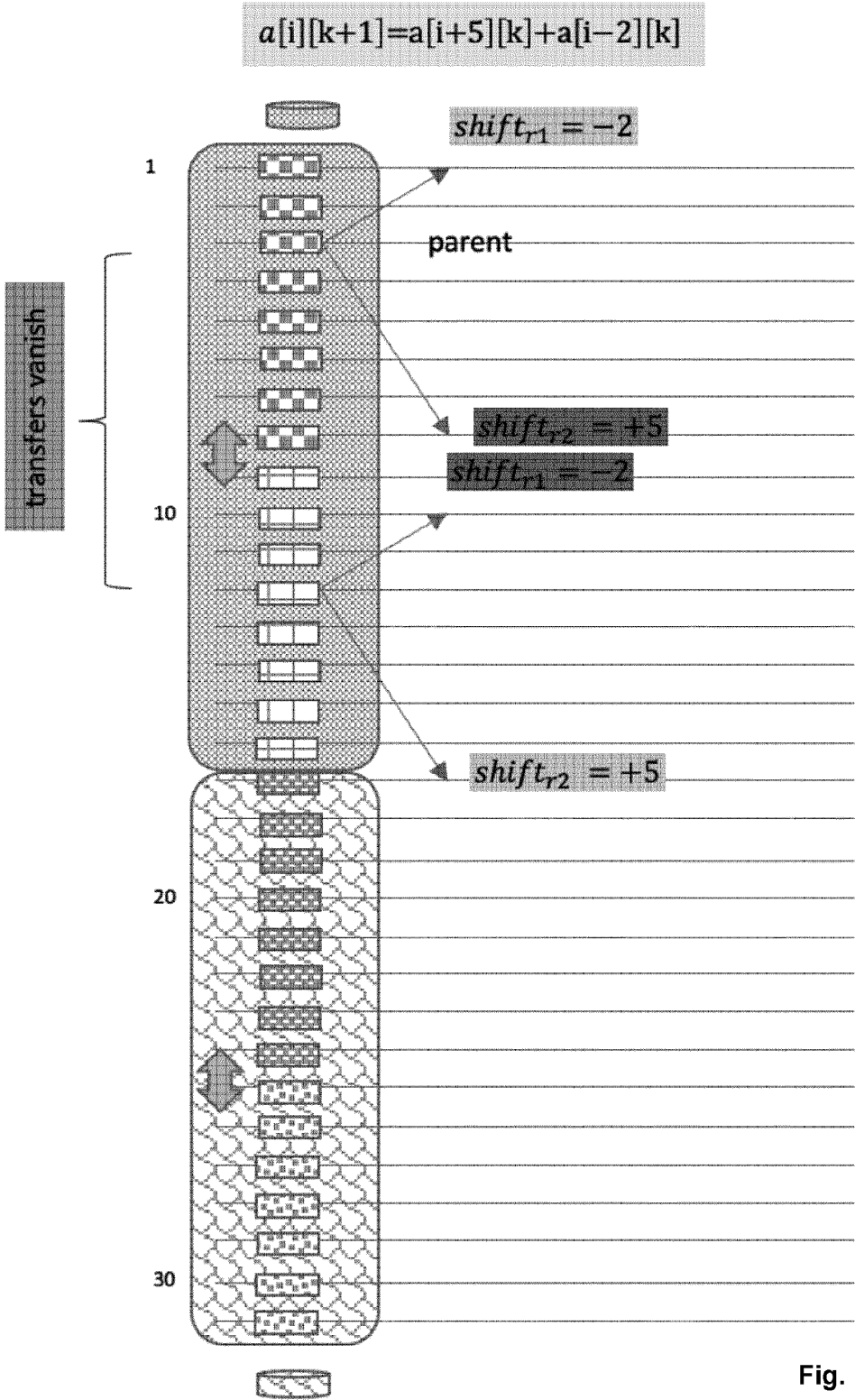


Fig. 102

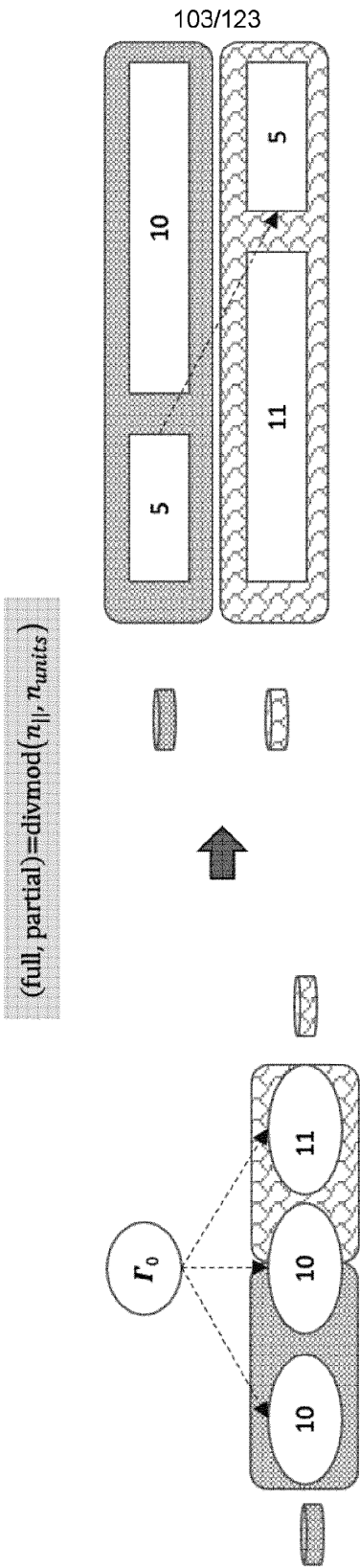


Fig. 103

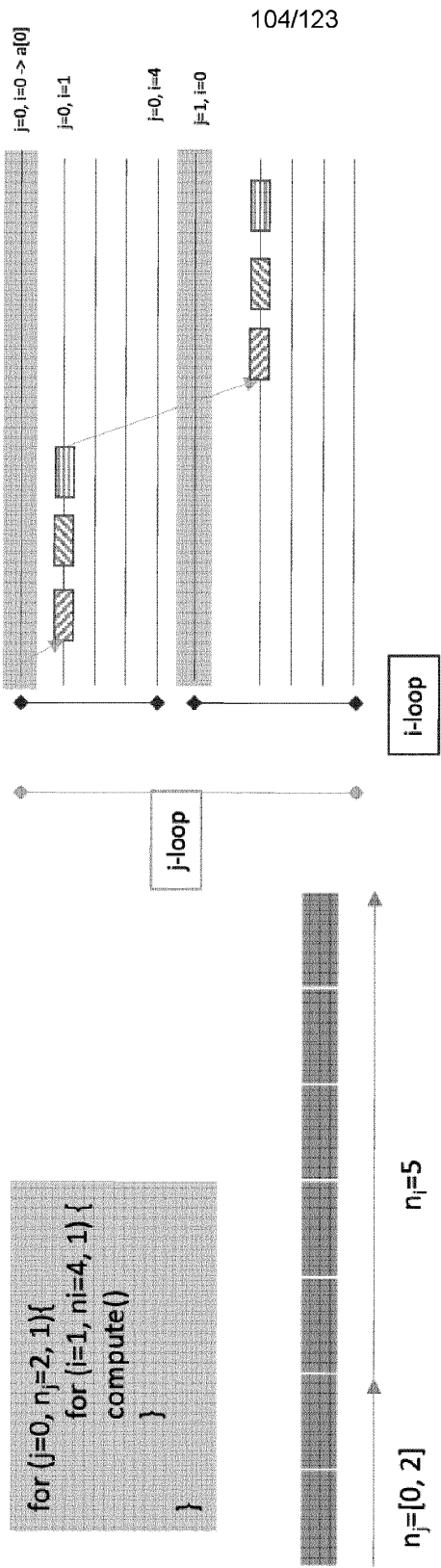


Fig. 104

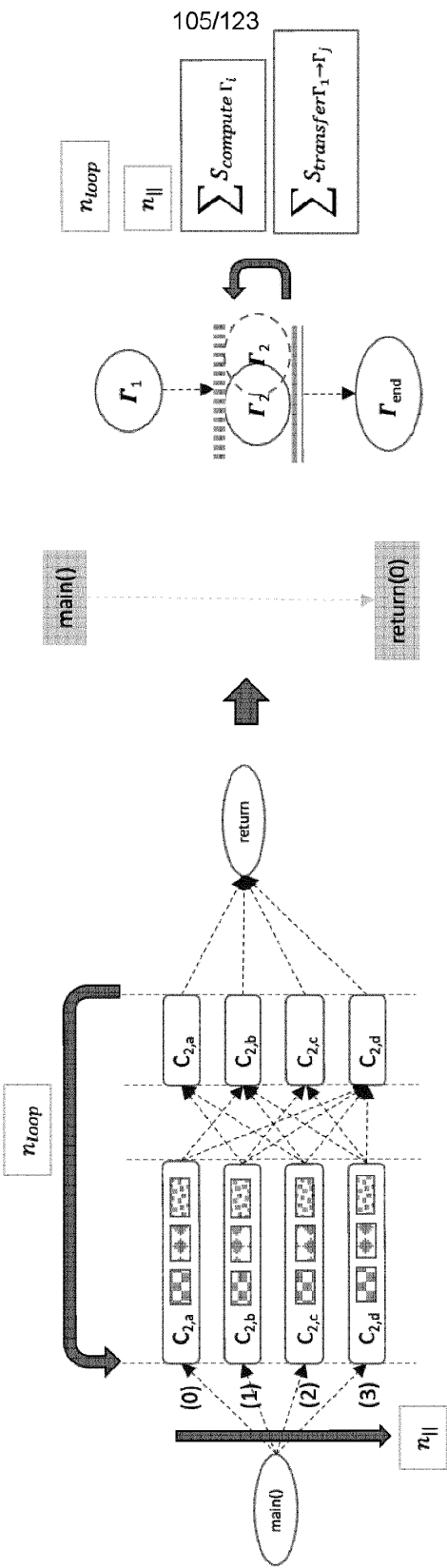


Fig. 105

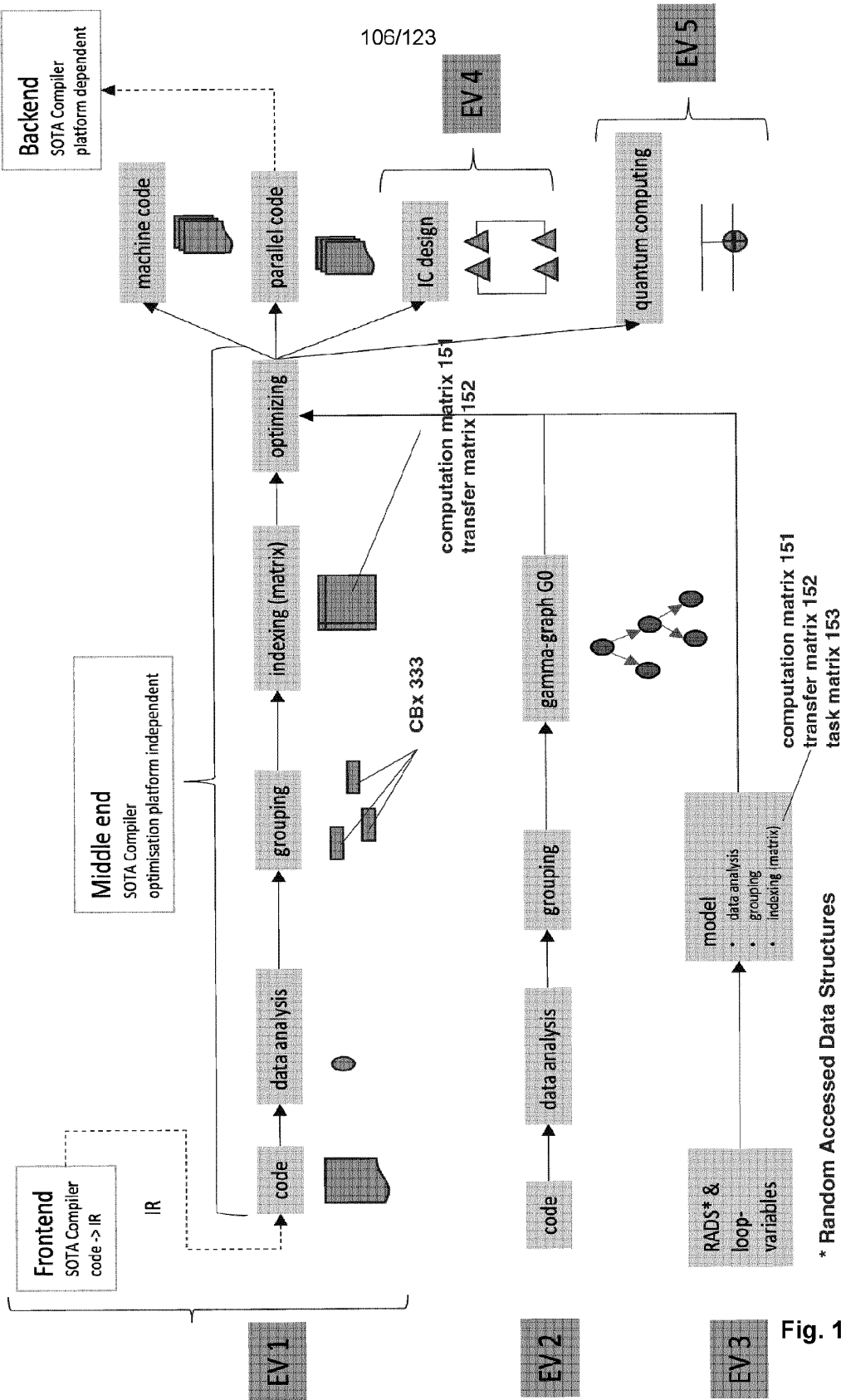


Fig. 106

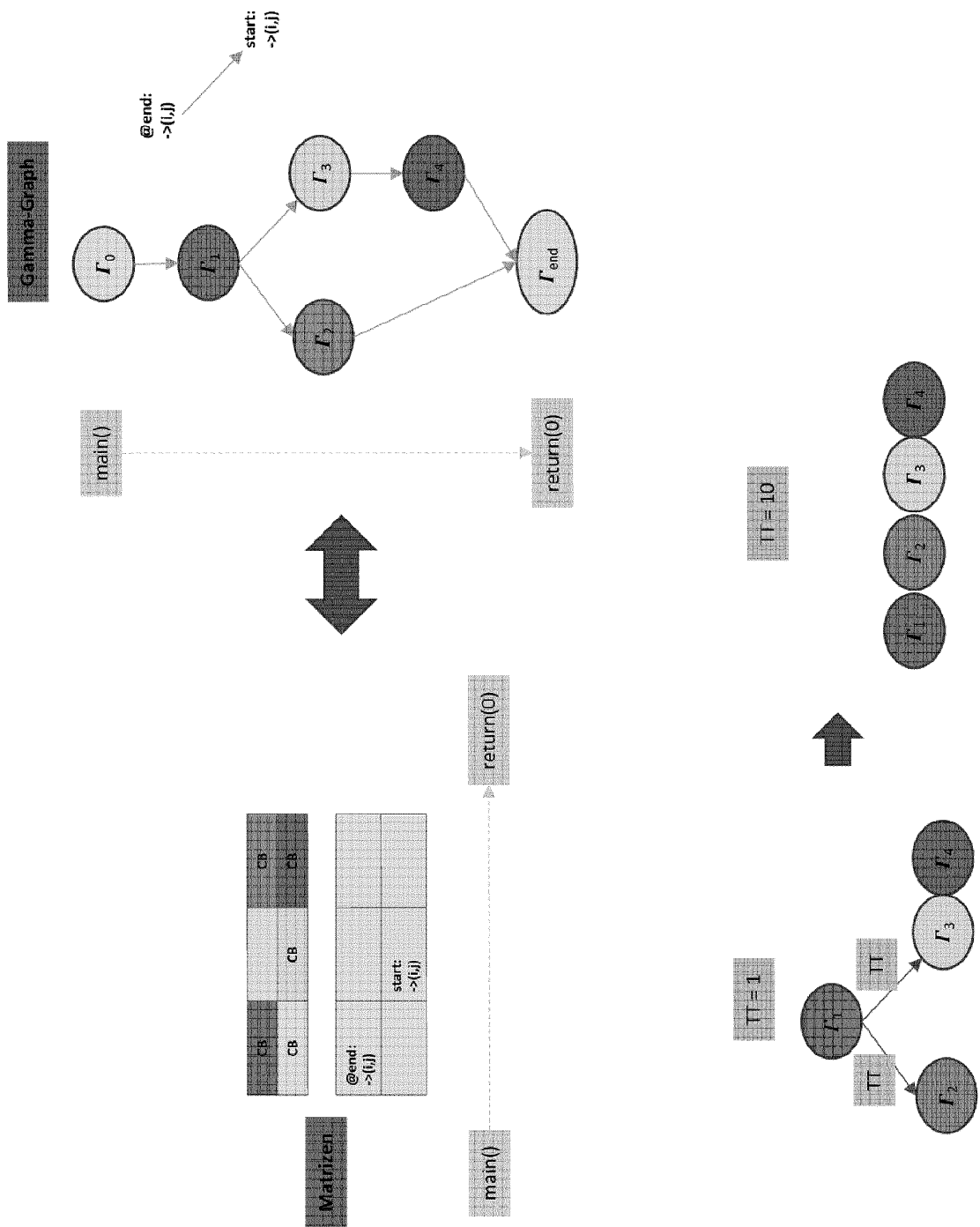


Fig. 107

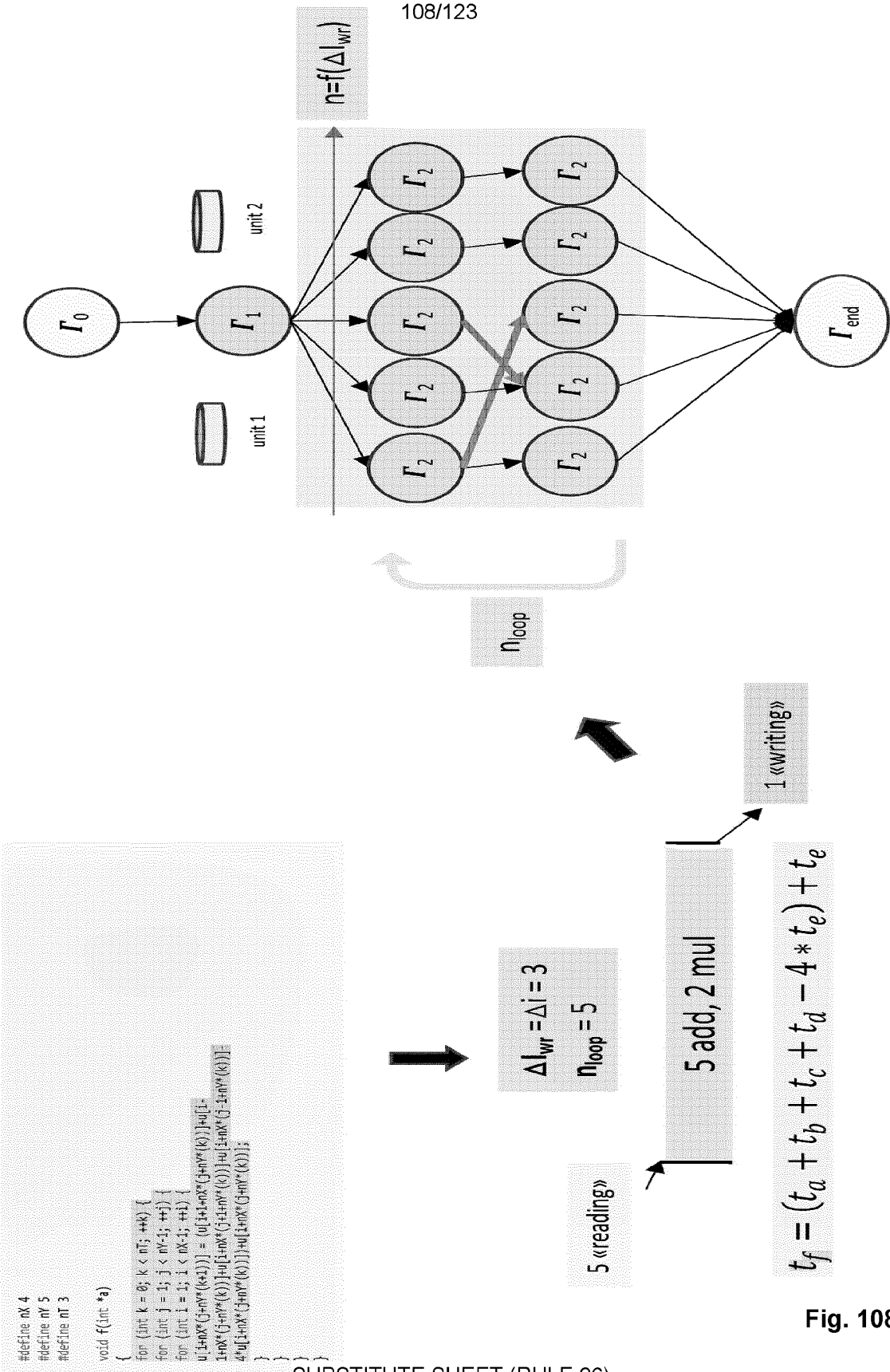


Fig. 108

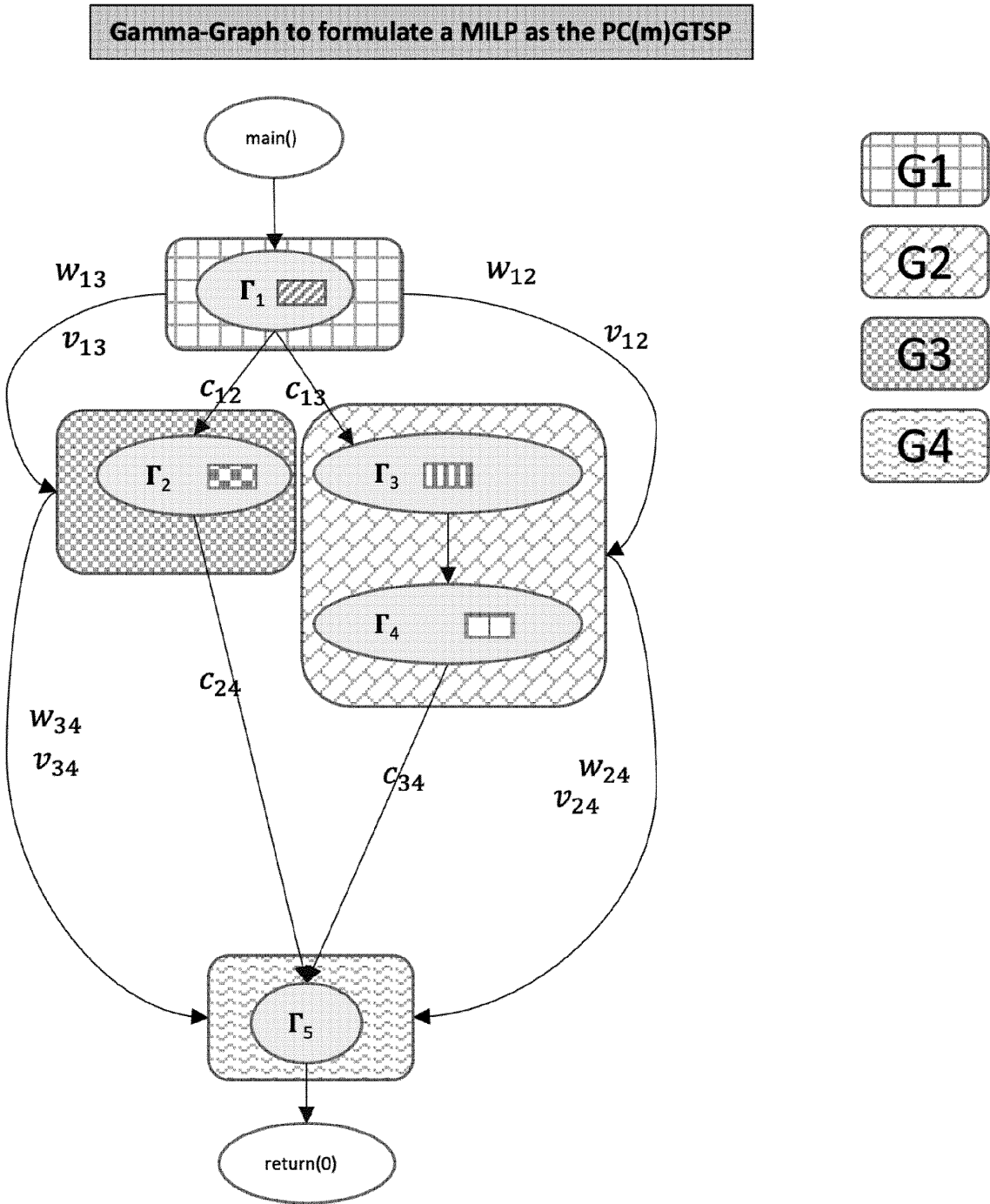


Fig. 109a

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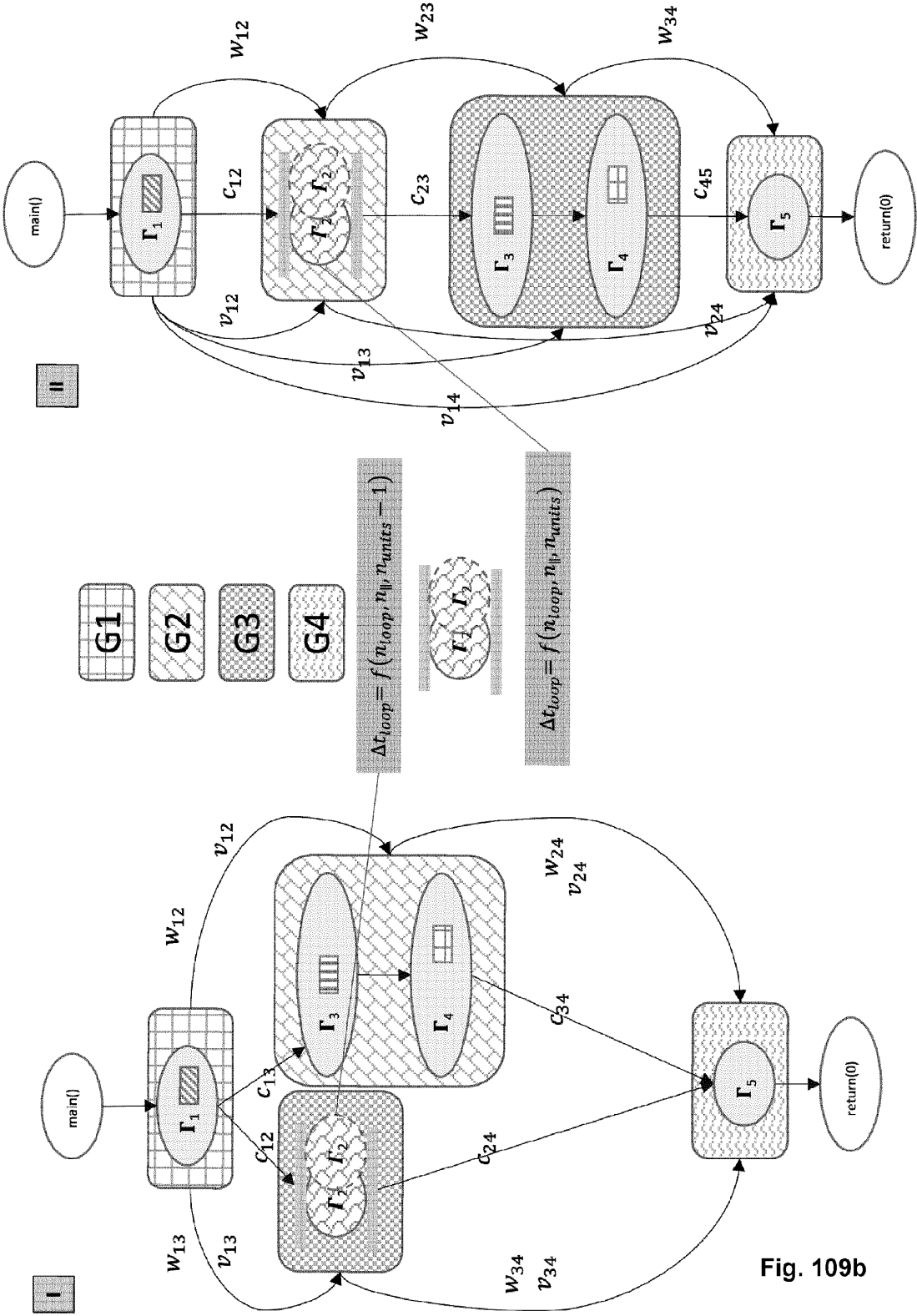
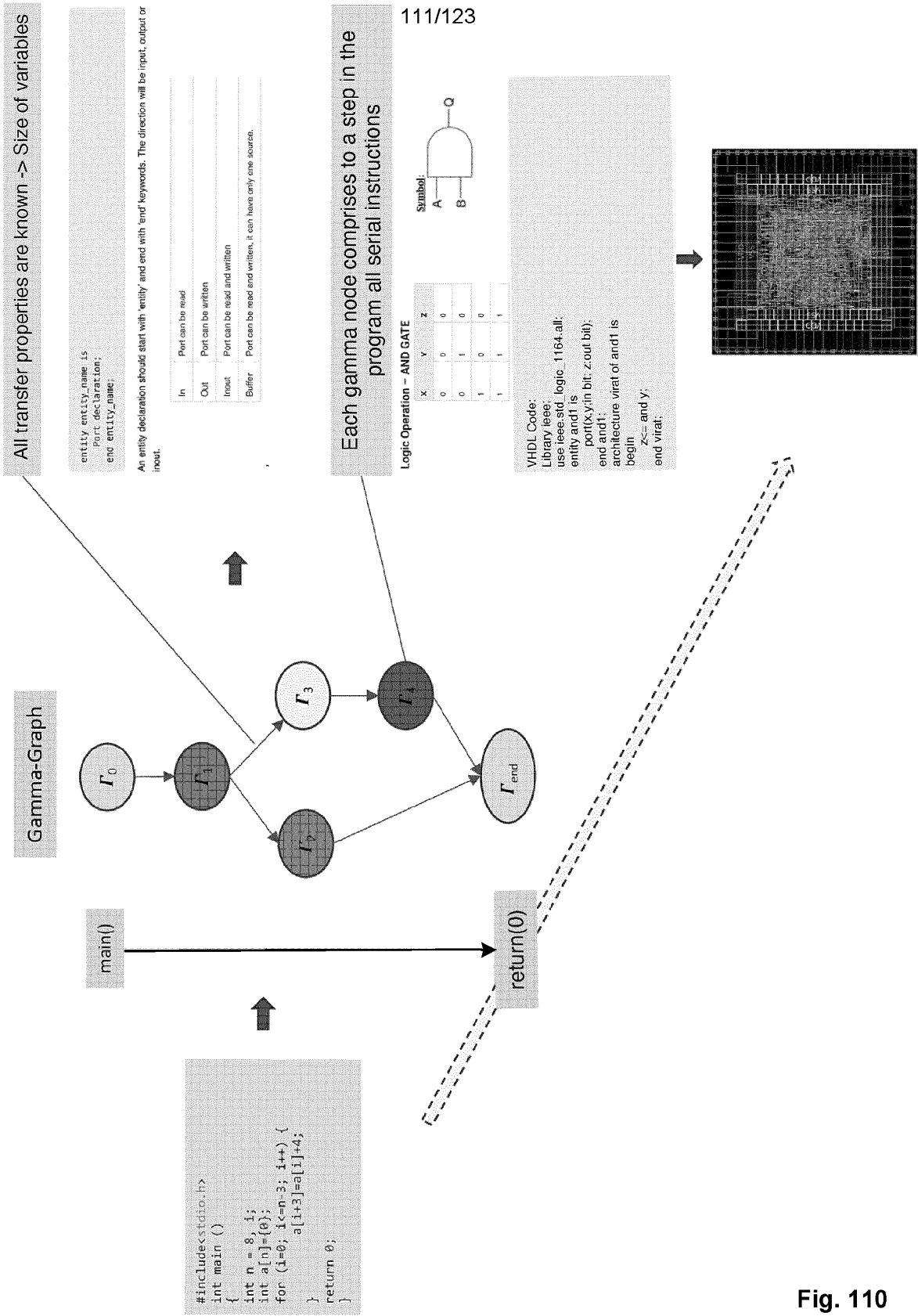


Fig. 109b



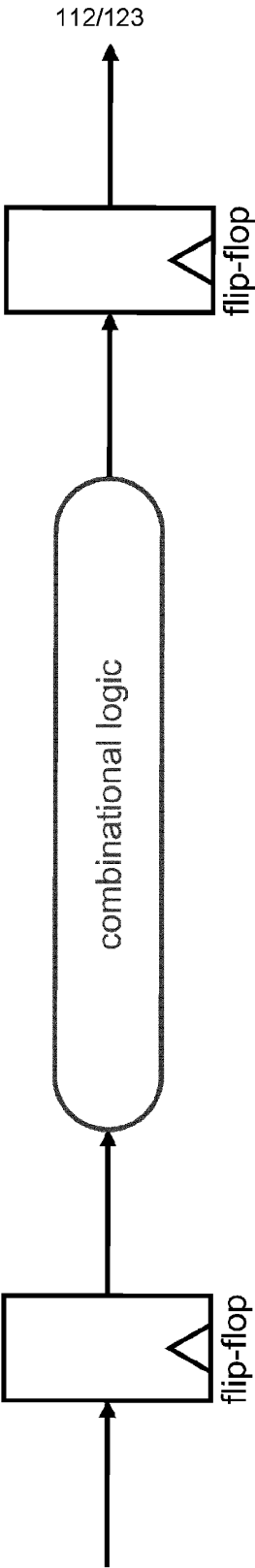


Fig. 111a

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1 write

compute

5 reads

Fig. 111b

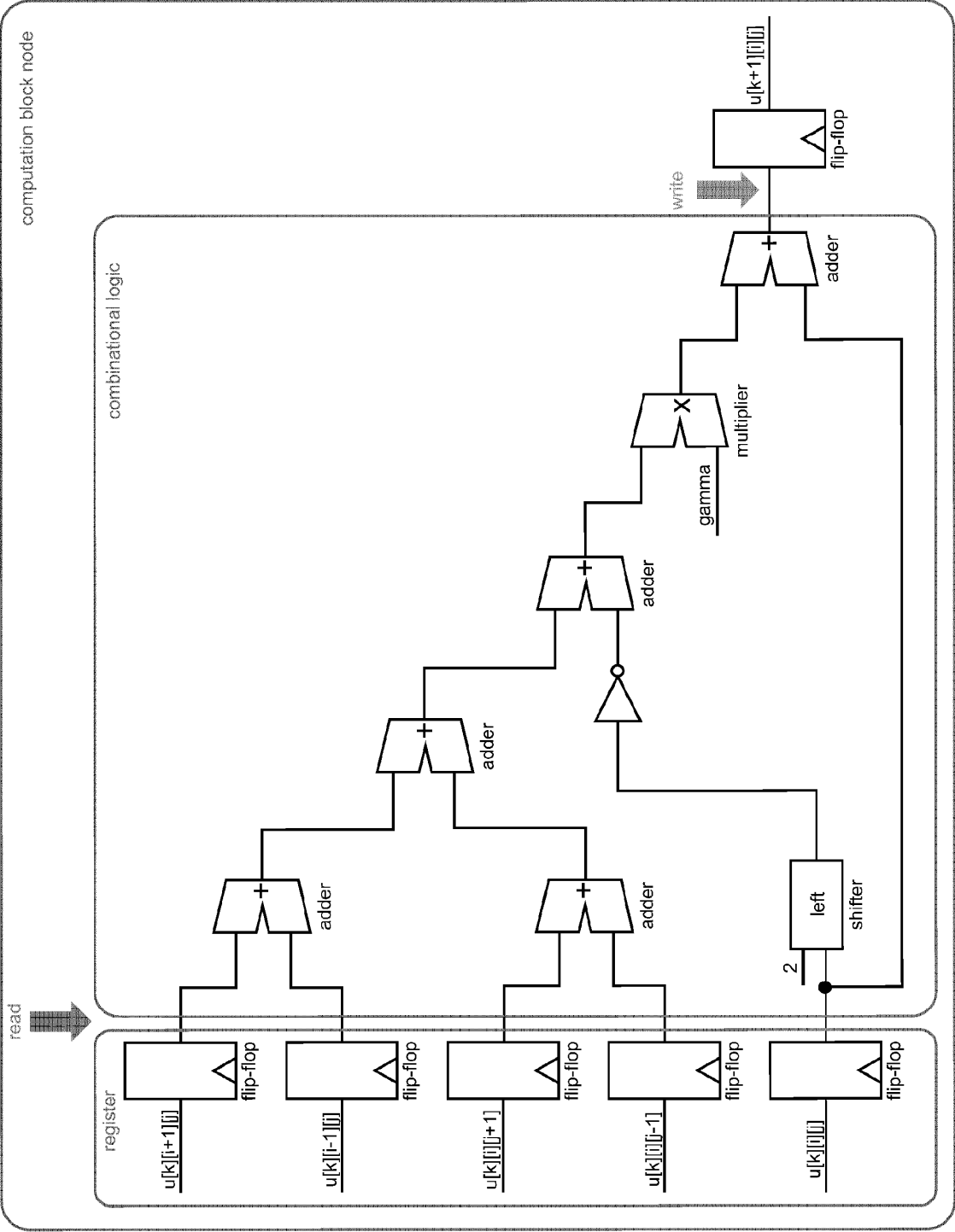


Fig. 111c

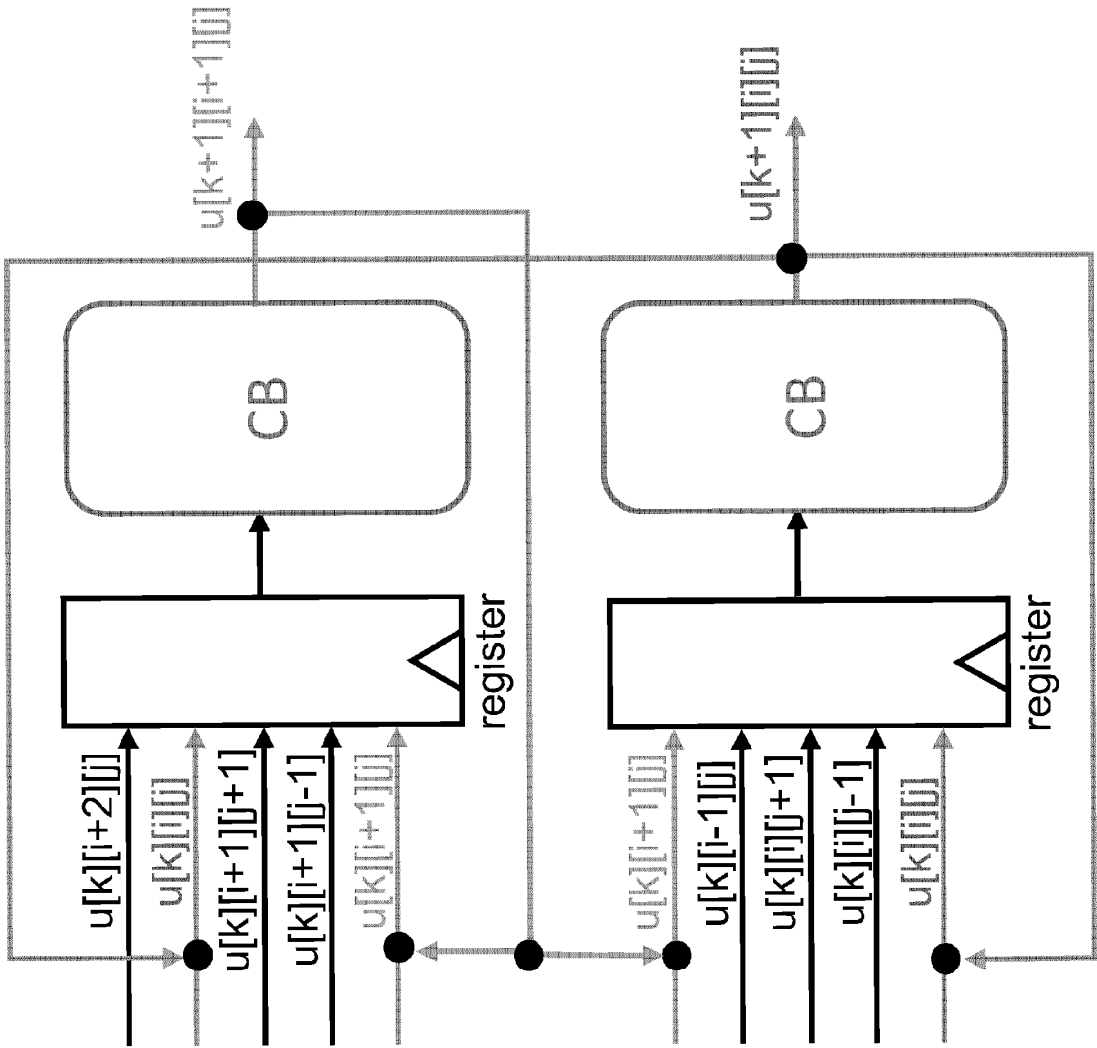


Fig. 111d

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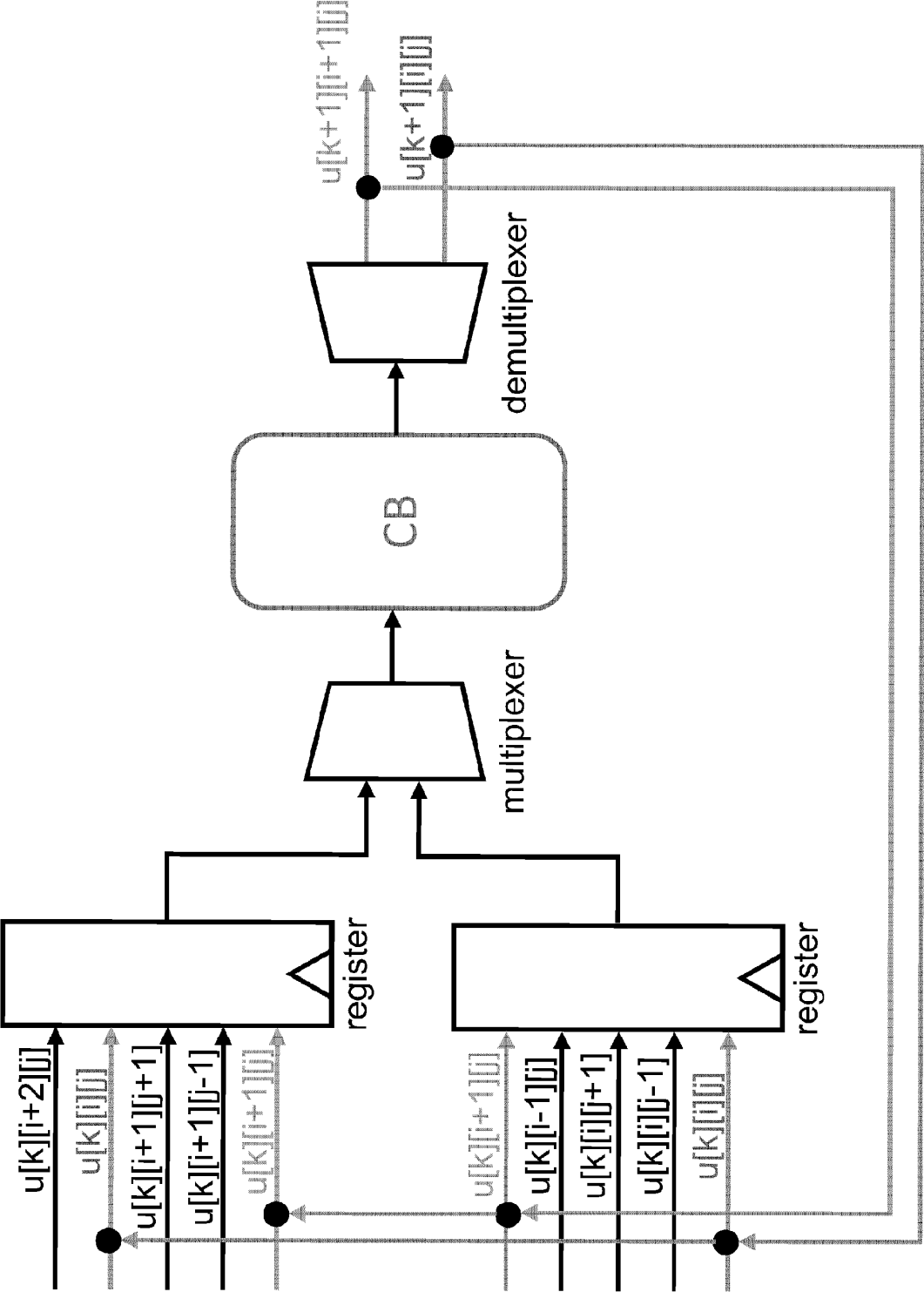


Fig. 111e

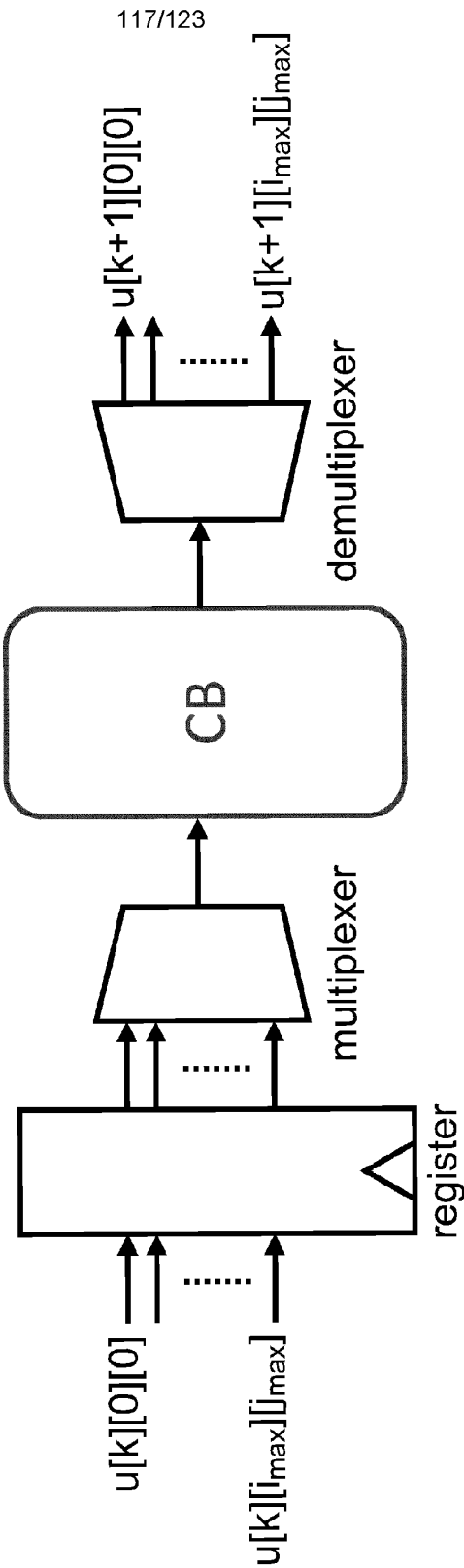


Fig. 111f

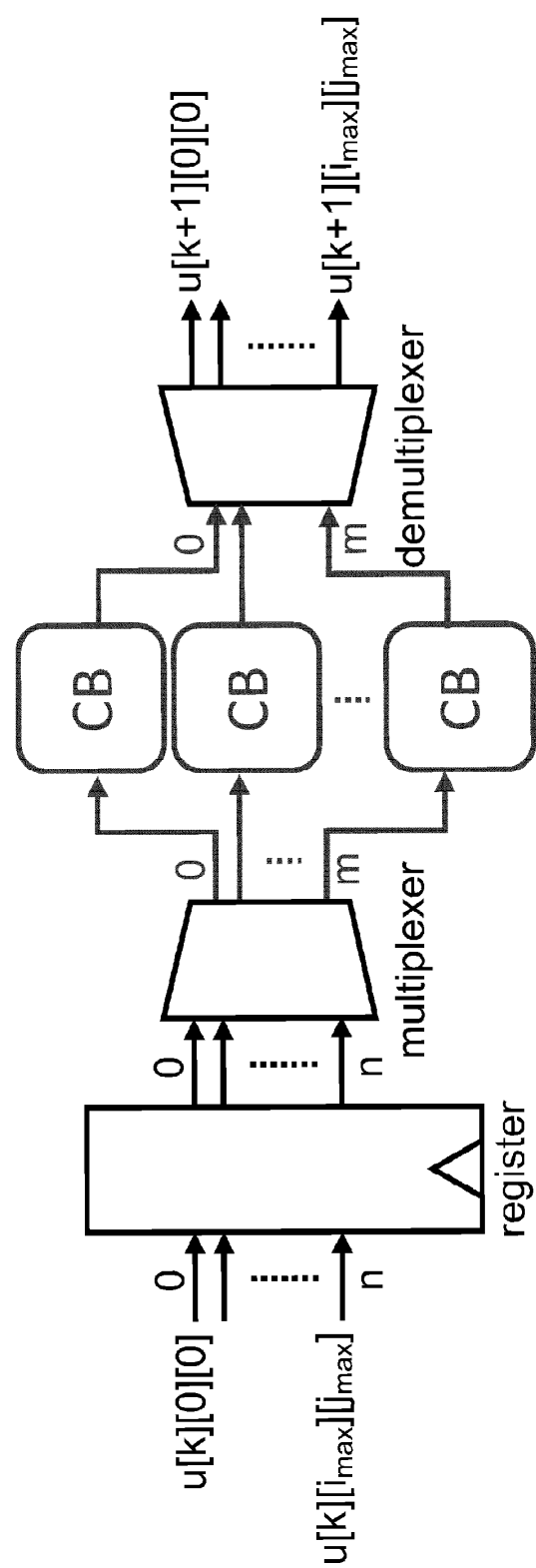


Fig. 111g

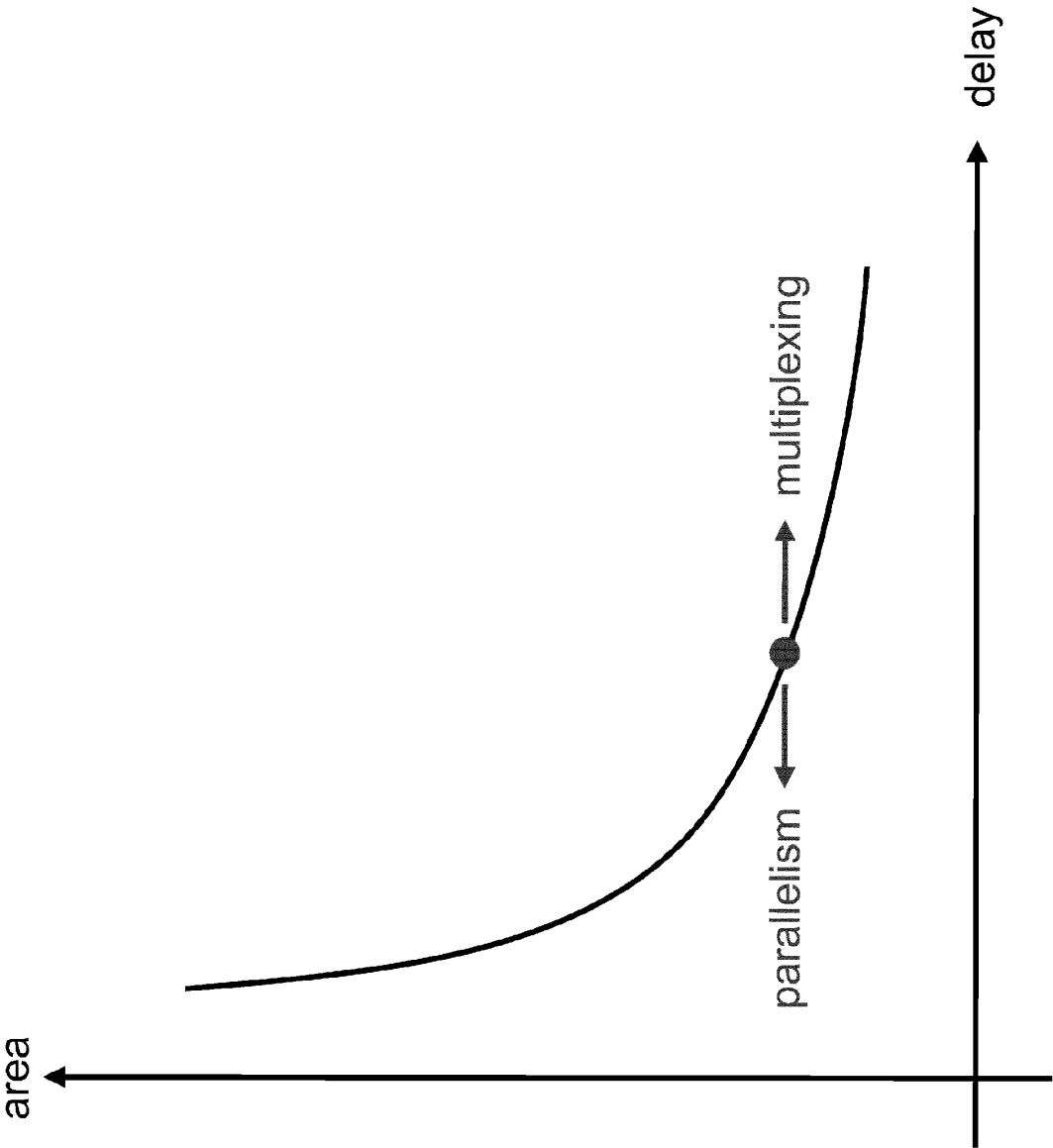


Fig. 111h

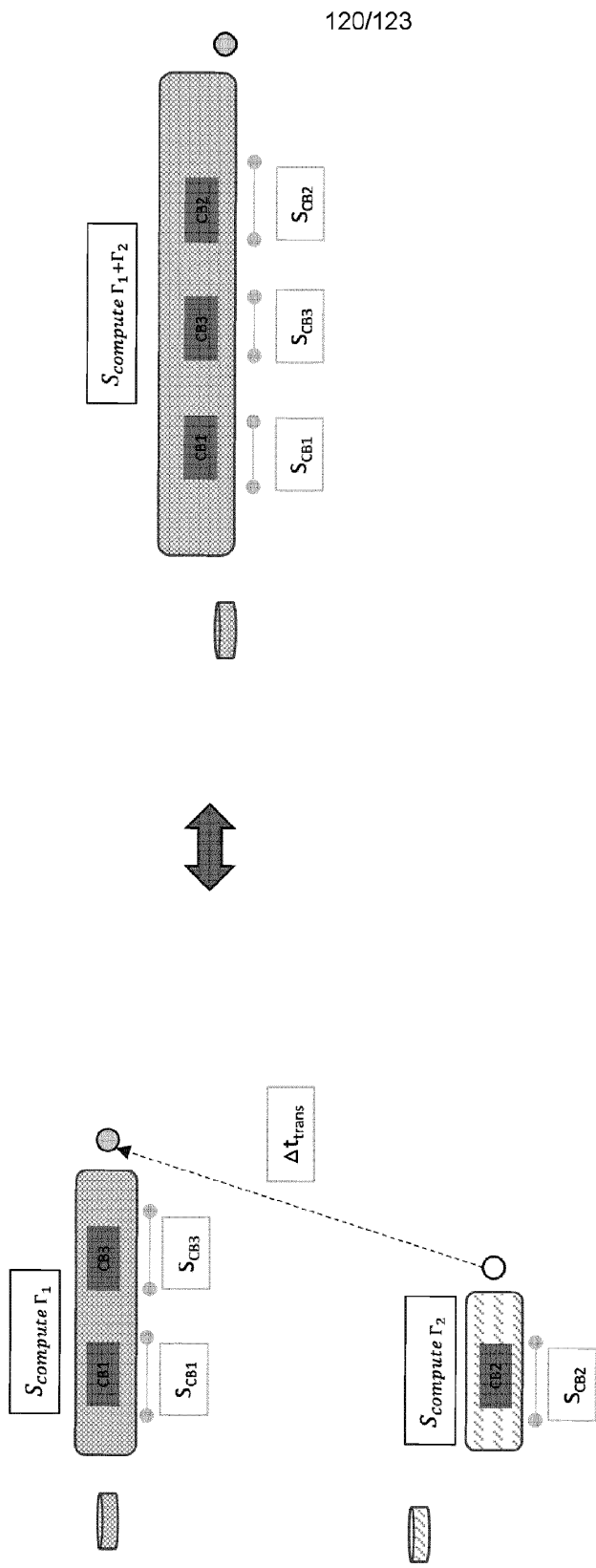


Fig. 112

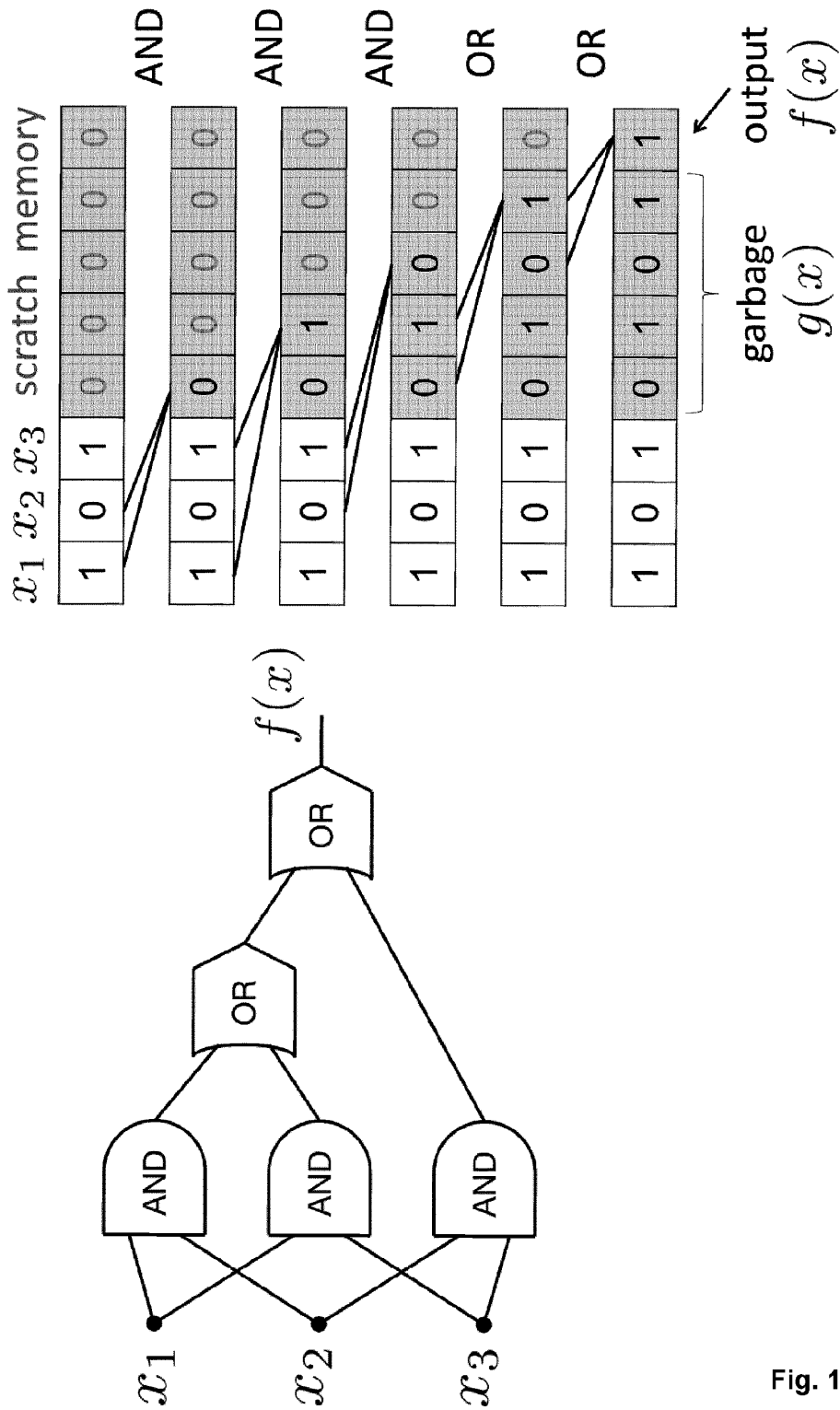


Fig. 113

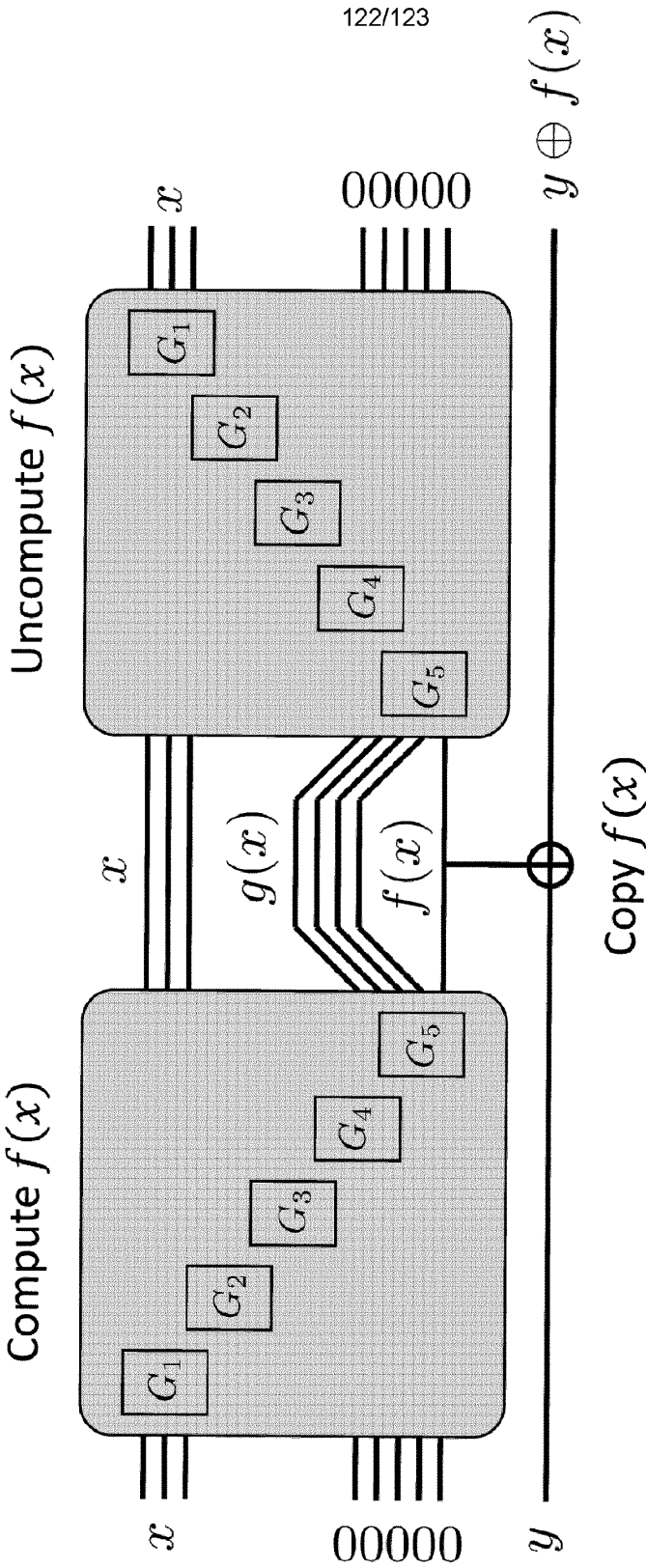


Fig. 114

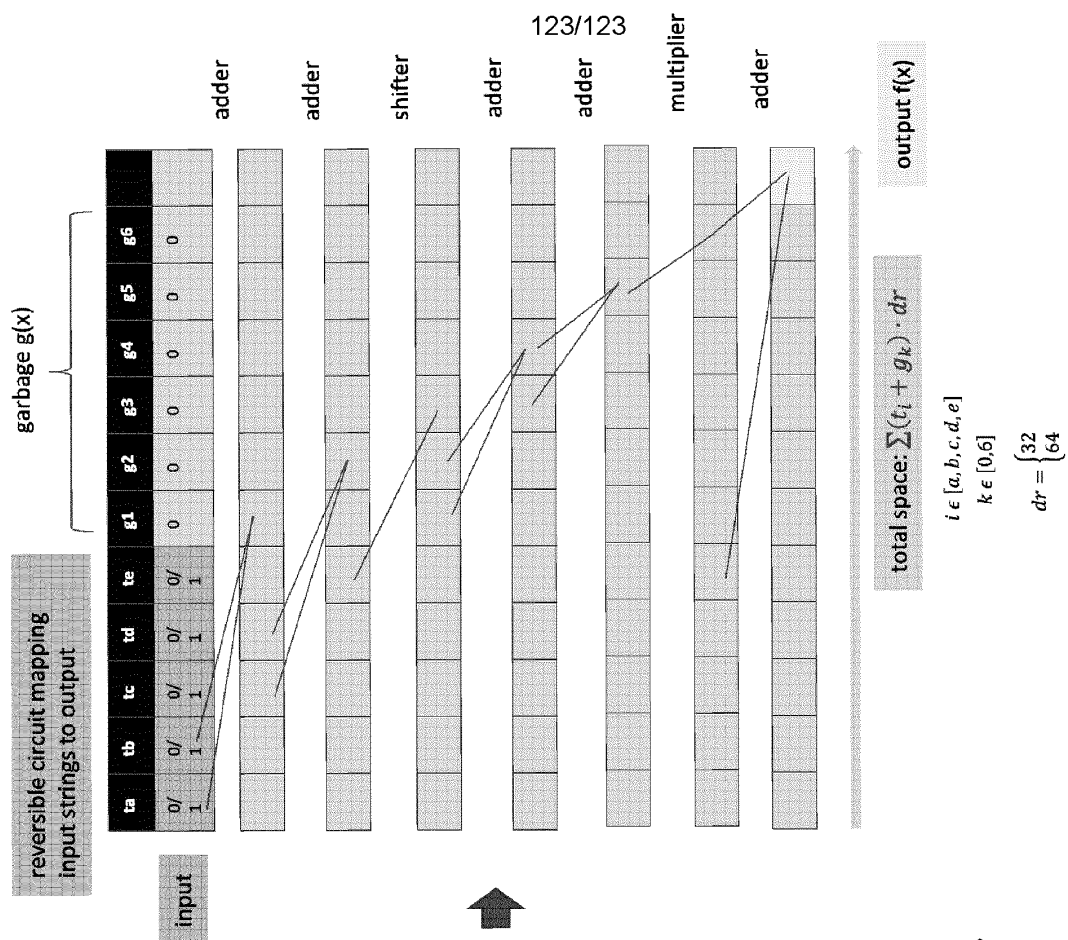


Fig. 59: $t_w = \kappa * (t_a + t_b + t_c + t_d - 4 * t_e) + t_e$

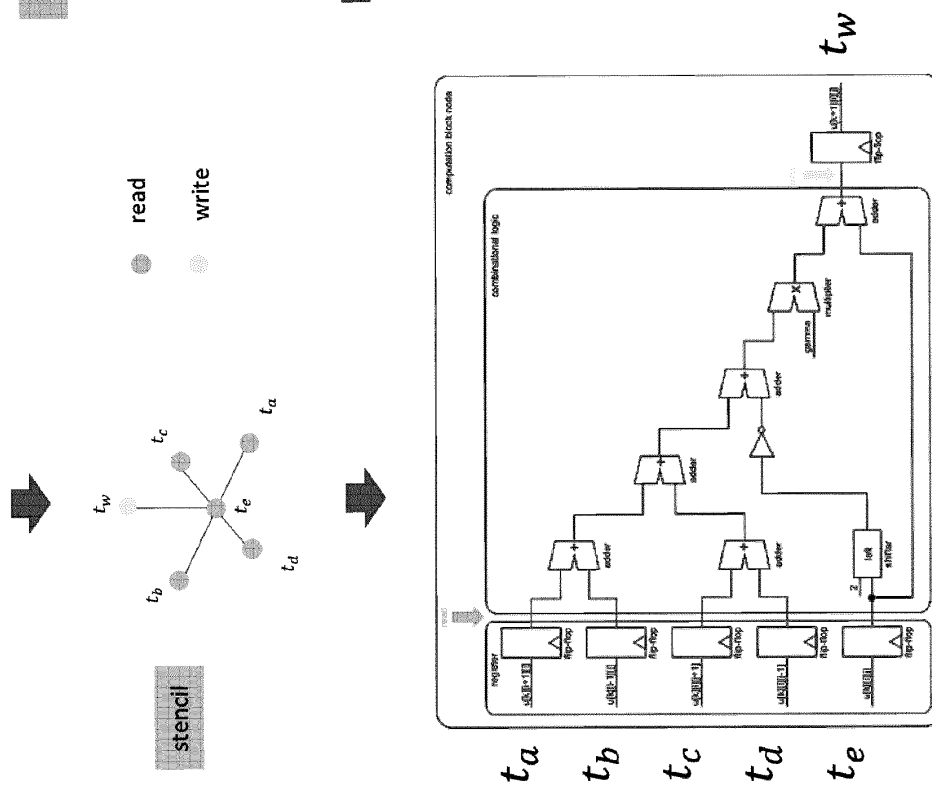


Fig. 111c

combinational ic-circuit