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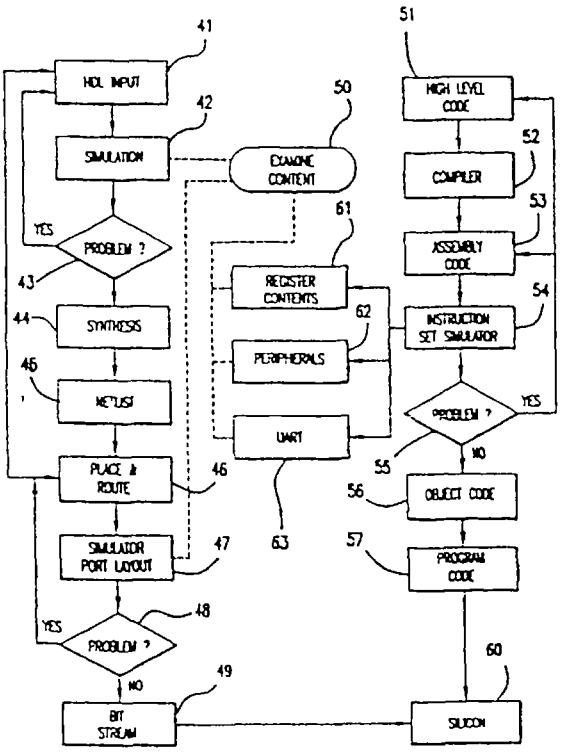
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(54) Title: SOFTWARE TOOL TO ALLOW FILED PROGRAMMABLE SYSTEM LEVEL DEVICES



(57) Abstract: A method and system for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system level integrated circuit. An FPSLIC is simulated (42) in hardware, and a simulator-port layout (47) of the FPSLIC device is generated. In software, the method separately simulates, with an instruction-set simulator (54), the FPSLIC device and outputs register contents (61) from the instruction-set software. The contents from the simulator-port layout (47) are verified with the register contents (61). Additionally, the method may further include outputting peripheral contents (62) from the instruction-set simulator (54), and verifying contents (50) from the simulator-port layout (47) with the peripheral contents (62). UART contents (63) also may be outputted form the instruction-set simulator (54), and verified with contents from the simulator-port layout (47) with the UART contents (63).

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