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ABSTRACT

A METHOD FOR MAKING AUTO-SELF-ALIGNED TOP ELECTRODES FOR DRAM CAPACITORS WITH IMPROVED CAPACITOR-TO-BIT-LINE-CONTACT OVERLAY MARGIN

Novel capacitor top electrodes auto-self-aligned to bit-line regions is achieved with improved process yields. A first insulating layer is formed over the FETs, and a second insulating layer is deposited. Openings are etched for capacitors, and a novel photomask and etching are used to recess the second insulator. A first conducting layer is deposited for bottom electrodes, and a second photoresist is used to remove the first conducting layer on the top surfaces of the second insulating layer. A thin dielectric layer is deposited, and a second conducting layer is deposited, and polished back to form novel auto-self- aligned top electrodes to the second insulating layer for bit-line contact openings. This increases overlay margins, and the recessing of the second insulating layer in the first openings prevents polish-back damage to the bottom electrodes.

(Fig. 1)