~~THE INVENTION CLAIMED IS:~~

1. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a pair of trenches in the semiconductor substrate to define an active region therebetween;

forming an implanted source region in one of the trenches on one side of the active region;

forming an implanted drain region in the other trench on the other side of the active region;

forming shallow trench isolations in the trenches;

forming at least one gate over the active region; and

forming respective contacts to the implanted source region and the implanted drain region.

2. The method of claim 1 wherein the at least one gate is a floating gate, and further comprising forming an interpoly dielectric layer over at least portions of the shallow trench isolations, the implanted source and drain regions, and the floating gate.

3. The method of claim 2 further comprising forming a control gate over the interpoly dielectric layer.

4. The method of claim 1 further comprising forming a device dielectric layer over at least the shallow trench isolations and gate.

5. The method of claim 4 wherein the step of forming respective contacts to the implanted source region and the implanted drain region further comprises forming the respective source and drain contacts through the device dielectric layer to the implanted source region and the implanted drain region.

6. A method for manufacturing a flash memory integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a pad oxide layer on the semiconductor substrate;

patterning and forming a first photomask on the pad oxide layer, the first photomask having mask openings therein for forming shallow trench isolation trenches;

forming shallow trench isolation trenches in the semiconductor substrate;

implanting buried junctions in the trenches, the implanted area of one such buried junction in one such trench, along the sidewall thereof adjacent another such trench, forming an implanted source region, the implanted area of the buried junction along the sidewall of the other such trench adjacent the implanted source region forming an implanted drain region, and the portion of the semiconductor substrate between the implanted source region and the implanted drain region forming an active region for the integrated circuit structure;

forming shallow trench isolations in the trenches; and

forming a floating gate over the active region between the implanted source and the implanted drain regions.

7. The method of claim 6 further comprising forming an interpoly dielectric layer over at least portions of the shallow trench isolations, the buried junctions, and the floating gate.

8. The method of claim 7 further comprising forming a control gate over the interpoly dielectric layer;

9. The method of claim 6 further comprising forming a device dielectric layer over at least the shallow trench isolations and floating gate.

10. The method of claim 9 further comprising forming source and drain contacts through the device dielectric layer to the implanted source region and the implanted drain region, respectively.

11. An integrated circuit structure, comprising:

a semiconductor substrate;

a pair of trenches in the semiconductor substrate defining an active region therebetween;

an implanted source region in one of the trenches on one side of the active region;

an implanted drain region in the other trench on the other side of the active region;

shallow trench isolations in the trenches;

at least one gate over the active region; and

contacts connected respectively to the implanted source region and the implanted drain region.

12. The integrated circuit structure of claim 11 wherein the at least one gate is a floating gate, and further comprising an interpoly dielectric layer over at least portions of the shallow trench isolations, the implanted source and drain regions, and the floating gate.

13. The integrated circuit structure of claim 12 further comprising a control gate over the interpoly dielectric layer.

14. The integrated circuit structure of claim 11 further comprising a device dielectric layer over at least the shallow trench isolations and gate.

15. The integrated circuit structure of claim 14 wherein the contacts to the implanted source region and the implanted drain region further comprise source and drain contacts connected respectively through the device dielectric layer to the implanted source region and the implanted drain region.

16. A flash memory integrated circuit structure, comprising:

a semiconductor substrate;

a pad oxide layer on the semiconductor substrate;

shallow trench isolation trenches in the semiconductor substrate;

buried junctions implanted in the trenches, the implanted area of one such buried junction in one such trench, along the sidewall thereof adjacent another such trench, forming an implanted source region, the implanted area of the buried junction along the sidewall of the other such trench adjacent the implanted source region forming an implanted drain region, and the portion of the semiconductor substrate between the implanted source region and the implanted drain region forming an active region for the integrated circuit structure;

shallow trench isolations in the trenches; and

a floating gate over the active region between the implanted source and the implanted drain regions.

17. The integrated circuit structure of claim 16 further comprising an interpoly dielectric layer over at least portions of the shallow trench isolations, the buried junctions, and the floating gate.

18. The integrated circuit structure of claim 17 further comprising a control gate over the interpoly dielectric layer;

19. The integrated circuit structure of claim 16 further comprising a device dielectric layer over at least the shallow trench isolations and floating gate.

20. The integrated circuit structure of claim 19 further comprising source and drain contacts through the device dielectric layer to the implanted source region and the implanted drain region, respectively.

WHAT IS CLAIMED IS:

1. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a pair of trenches in the semiconductor substrate to define an active region therebetween;

forming an implanted source region in one of the trenches on one side of the active region;

forming an opposing implanted drain region in the other trench on the other side of the active region opposite the implanted source region in the one trench;

forming shallow trench isolations in the trenches;

forming at least one gate extending laterally across the active region and the implanted source and drain regions; and

forming respective contacts to the implanted source region and the implanted drain region.

2. The method of claim 1 wherein the at least one gate is a floating gate, and further comprising forming an interpoly dielectric layer over at least portions of the shallow trench isolations, the implanted source and drain regions, and the floating gate.

3. The method of claim 2 further comprising forming a control gate over the interpoly dielectric layer.

4. The method of claim 1 further comprising forming a device dielectric layer over at least the shallow trench isolations and gate.

5. The method of claim 4 wherein the step of forming respective contacts to the implanted source region and the implanted drain region further comprises forming the respective source and drain contacts through the device dielectric layer to the implanted source region and the implanted drain region.

6. A method for manufacturing a flash memory integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a pad oxide layer on the semiconductor substrate;

patterning and forming a first photomask on the pad oxide layer, the first photomask having mask openings therein for forming shallow trench isolation trenches;

forming shallow trench isolation trenches in the semiconductor substrate;

implanting buried junctions in the trenches, the implanted area of one such buried junction in one such trench, along the sidewall thereof adjacent another such trench, forming an implanted source region, the implanted area of the buried junction along the opposing sidewall of the other such trench opposite the implanted source region in the one such trench and adjacent the implanted source region forming an implanted drain region, and the portion of the semiconductor substrate between the implanted source region and the implanted drain region forming an active region for the integrated circuit structure;

forming shallow trench isolations in the trenches;

forming a floating gate over the active region between the implanted source and the implanted drain regions; and

forming at least one gate extending laterally across the active region and the implanted source and drain regions.

7. The method of claim 6 further comprising forming an interpoly dielectric layer over at least portions of the shallow trench isolations, the buried junctions, and the floating gate.

8. The method of claim 7 further comprising forming a control gate over the interpoly dielectric layer.

9. The method of claim 6 further comprising forming a device dielectric layer over at least the shallow trench isolations and floating gate.

10. The method of claim 9 further comprising forming source and drain contacts through the device dielectric layer to the implanted source region and the implanted drain region, respectively.