CLAIMS

1. A method of making a quad flat no-lead (QFN), dual flat no-lead (DFN) or small outline no-lead (SON) package without a leadframe, comprising:

disposing at least two semiconductor chips face-up on a temporary carrier, the at least two semiconductor chips each comprising conductive stumps over an active layer of each of the at least two semiconductor chips;

disposing a first layer of encapsulant in a single step around four side surfaces of each of the at least two the semiconductor chips, over the active layer of each of the at least two semiconductor chips, and around the conductive stumps;

planarizing the first layer of encapsulant over the active layer of each of the at least two semiconductor chips to create a planar surface comprising exposed ends of the conductive stumps and an exposed encapsulant surface;

forming a first conductive layer and first vertical conductive contacts over the planar surface and configured to be electrically coupled with the conductive stumps of the at least two semiconductor chips;

disposing a second layer of encapsulant over the first layer of encapsulant, the first conductive layer and the first vertical conductive contacts;

forming a first photoresist over the second layer of encapsulant with openings formed through the first photoresist over the first vertical conductive contacts;

forming conductive pads in the form of land pads or bumps within the openings and then removing the first photoresist;

forming a second photoresist over the second layer of encapsulant with conductive pad openings formed through the second photoresist over the conductive pads;

forming a solderable metal system (SMS) or applying an organic solderability preservative (OSP) over the conductive pads to resist oxidation over at least a portion of the conductive pads; and

cutting through the second layer of encapsulant around at least one of the at least two semiconductor chips to form an outline of a package.

2. The method of claim 1, wherein forming the conductive pads comprises forming the conductive pads to include at least the second layer of encapsulant locked between the first conductive layer and the conductive pads.

3. The method of claim 1, wherein forming the first conductive layer comprises forming a redistribution layer directly upon an encapsulant surface, and wherein disposing a second layer of encapsulant over the first conductive layer includes disposing the second layer of encapsulant directly upon the redistribution layer, wherein the encapsulant surface and the second layer of encapsulant are of the same kind of encapsulant.

4. The method of claim 3, further comprising forming a flag, mounting pads, identifying mark, alignment marks, or other conductive structure over the at least two semiconductor chips and over the second layer of the encapsulant.

5. The method of claim 4, further comprising cutting through the second layer of encapsulant such that an edge or side of the conductive pad is inset from the resulting QFN, DFN or SON package edge.

6. The method of claim 2, further comprising forming the QFN, DFN or SON package without exposed copper.

7. A method of making a quad flat no-lead (QFN), dual flat no-lead (DFN) or small outline no-lead (SON) package without a leadframe, the method comprising:

disposing a semiconductor chip face-up on a temporary carrier, the semiconductor chip comprising conductive stumps over an active layer of the semiconductor chip;

disposing encapsulant in a single step around four side surfaces of the semiconductor chip, over the active layer of the semiconductor chip, and around at least a portion of sidewalls of the conductive stumps;

planarizing a surface of the encapsulant and conductive stumps;

forming conductive traces over the encapsulant;

forming conductive pads over the encapsulant in the form of land pads or bumps; and

forming a solderable metal system (SMS) or applying an organic solderability preservative (OSP) over the conductive pads to resist oxidation over at least a portion of the conductive pads;

wherein the QFN, DFN or SON package includes no solder balls.

8. The method of claim 7, wherein forming conductive traces on the encapsulant comprises forming a redistribution layer directly upon an encapsulant surface, and further comprising disposing encapsulant directly upon the redistribution layer, wherein the encapsulant disposed in the single step and the encapsulant disposed directly upon the redistribution layer are of the same kind of encapsulant.

9. The method of claim 7, wherein each conductive pad includes at least one layer of encapsulant locked between at least two layers of conductive material.

10. The method of claim 7, further comprising forming a flag, mounting pads, identifying mark, alignment marks, or other conductive structure over the semiconductor chip and over the second layer of the encapsulant.

11. The method of claim 7, wherein the conductive pads extend beyond the encapsulant's surface.

12. The method of claim 7, further comprising forming openings in a second photoresist layer around the conductive pads, the openings comprising an offset between the conductive pads and an edge of the second photoresist layer.

13. The method of claim 7, further comprising forming the QFN, DFN or SON package without exposed copper on a periphery of the QFN, DFN or SON package.

14. The method of claim 7, wherein the QFN, DFN or SON package includes no solder balls.

15. A quad flat no-lead (QFN) dual flat no-lead (DFN) or small outline no-lead (SON) package without a leadframe, comprising:

a semiconductor chip comprising conductive studs over an active layer of the semiconductor chip; wherein the conductive studs comprise a first end directly connected to the active layer and a second end opposite the first end wherein the second end is in a range of 1-50 micrometers (μm) from the first end;

encapsulant disposed in a single layer around four side surfaces of the semiconductor chip, over the active layer of the semiconductor chip, and around a portion of sidewalls of the conductive studs;

conductive traces formed over a planarized surface of the encapsulant and conductive studs; and

a plurality of conductive pads in the form of land pads or bumps formed over the encapsulant and in electrical contact with the conductive studs.

16. The QFN, DFN or SON package of claim 15, further comprising:

a solderable metal system (SMS) formed or an organic solderability preservative (OSP) applied over at least a portion of the plurality of conductive pads; and

wherein the SMS comprises a layer of conductive materials over the conductive pads formed by one or more of electroplating, electroless plating, immersion plating, physical

vapor deposition (PVD), and chemical vapor deposition (CVD).

17. The QFN, DFN or SON package of claim 15, wherein each conductive pad includes at least one layer of encapsulant locked between at least two layers of conductive material.

18. The QFN, DFN or SON package of claim 15, further comprising a redistribution layer formed directly upon an encapsulant surface, and encapsulant disposed directly upon the redistribution layer, wherein the encapsulant upon which the redistribution layer is formed and the encapsulant disposed directly upon the redistribution layer are of the same kind of encapsulant.

19. The QFN, DFN or SON package of claim 15, further comprising an offset between an edge or side of the conductive pad and the package edge.

20. The QFN, DFN or SON package of claim 15, wherein the QFN, DFN or SON package is formed without exposed copper on the QFN, DFN or SON package.

21. The QFN, DFN or SON package of claim 15, wherein the QFN, DFN or SON package includes no solder balls.