

GATE DIELECTRIC PROTECTION

ABSTRACT

Protecting a gate dielectric is achieved with a gate dielectric protection circuit coupled to a transistor at risk. The protection circuit is activated to reduce the voltage across the gate dielectric (V_{DIFF}) to below its breakdown voltage (V_{BD}). The protection circuit is activated when an ESD event is detected. The protection circuit provides a protection or ESD bias to reduce V_{DIFF} below V_{BD} .

Fig. 1