

FIG. 1

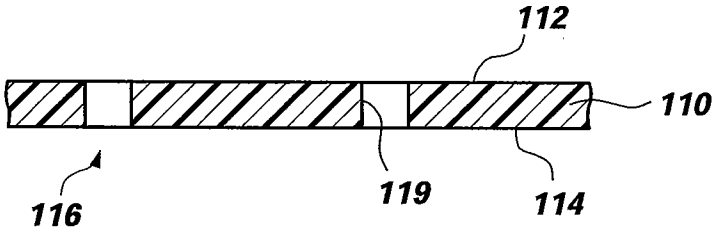


FIG. 1A

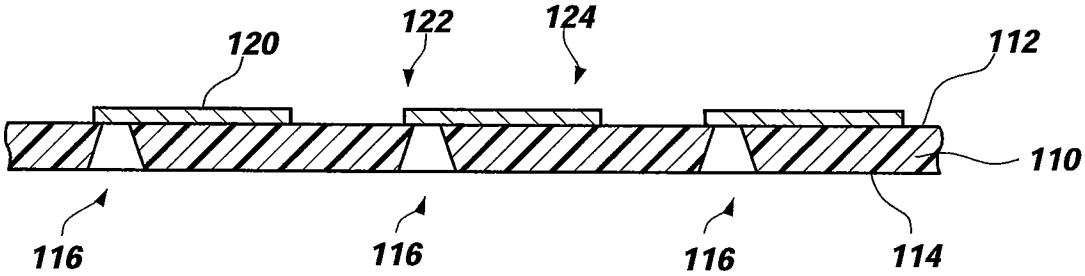


FIG. 2

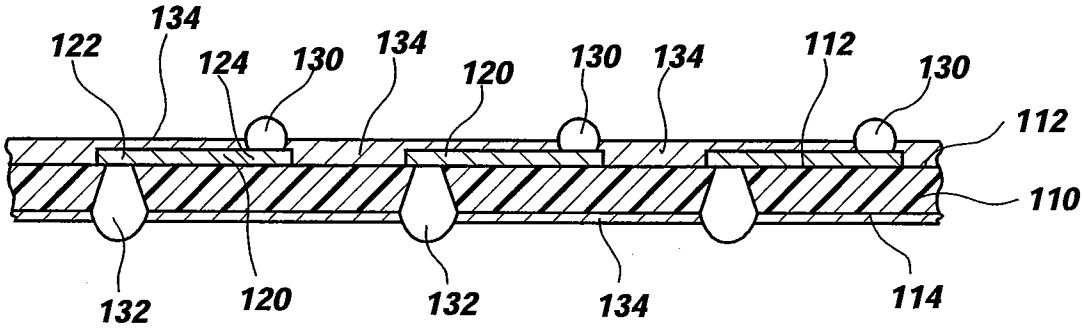

122
134
124
130
134
120
130
134
112
130
112
110
132
120
132
134
114

FIG. 3

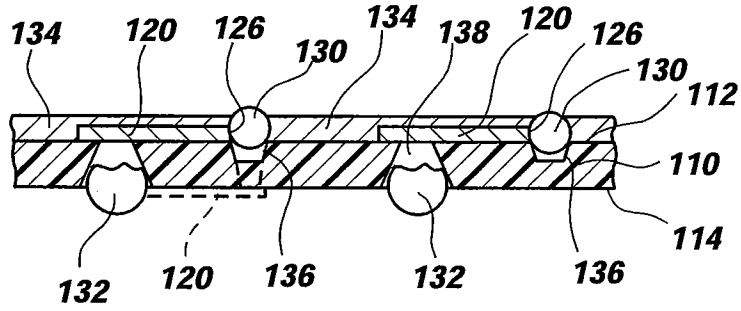

134
120
126
130
134
138
120
126
130
112
110
114
132
120
136
132
136

FIG. 3A

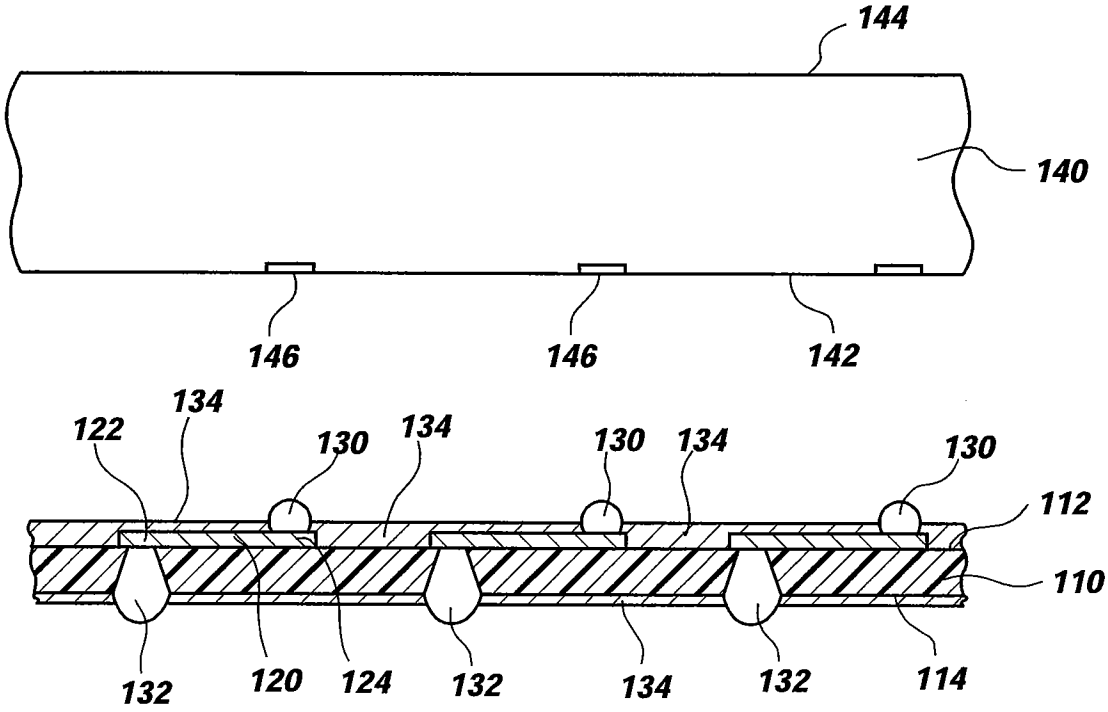

144
140
146
146
142
122
134
130
134
130
134
130
112
110
132
120
124
132
134
132
114

FIG. 4

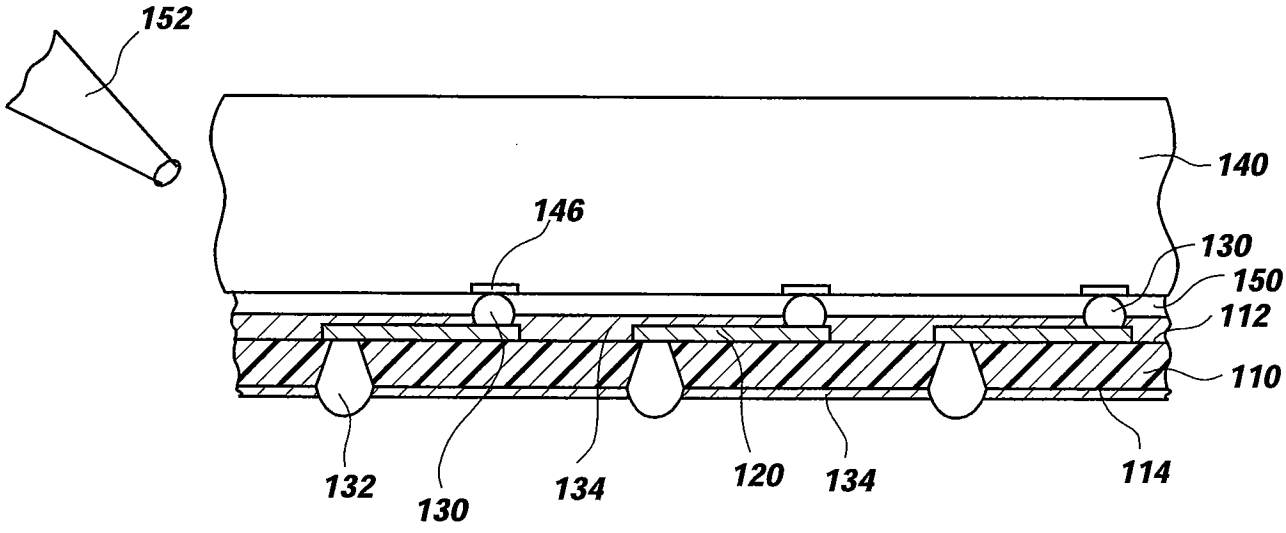

152
140
146
130
150
112
110
132
130
134
120
134
114

FIG. 5

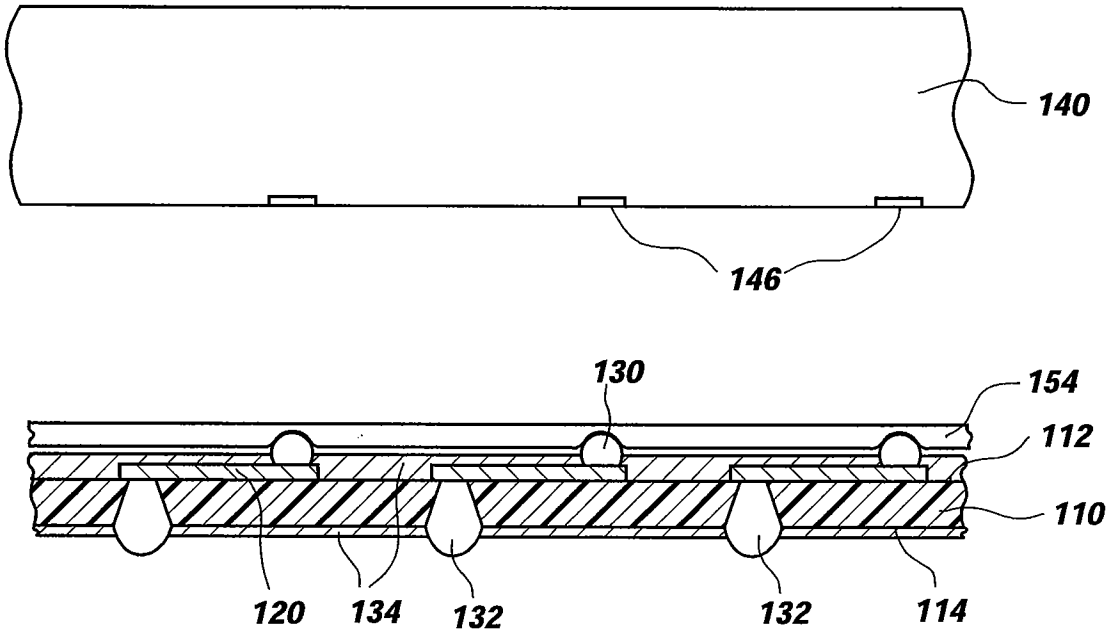

140
146
130
154
112
110
120
134
132
132
114

FIG. 6

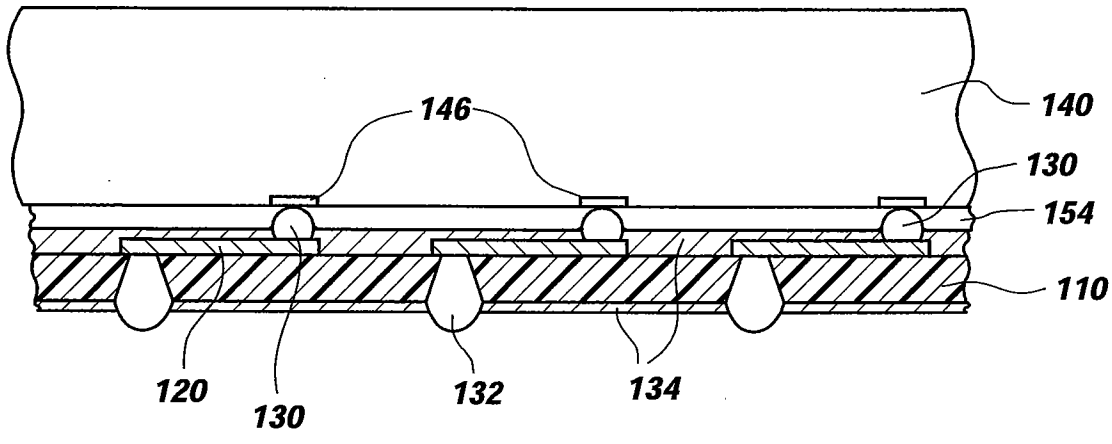

140
146
130
154
110
120
130
132
134

FIG. 7

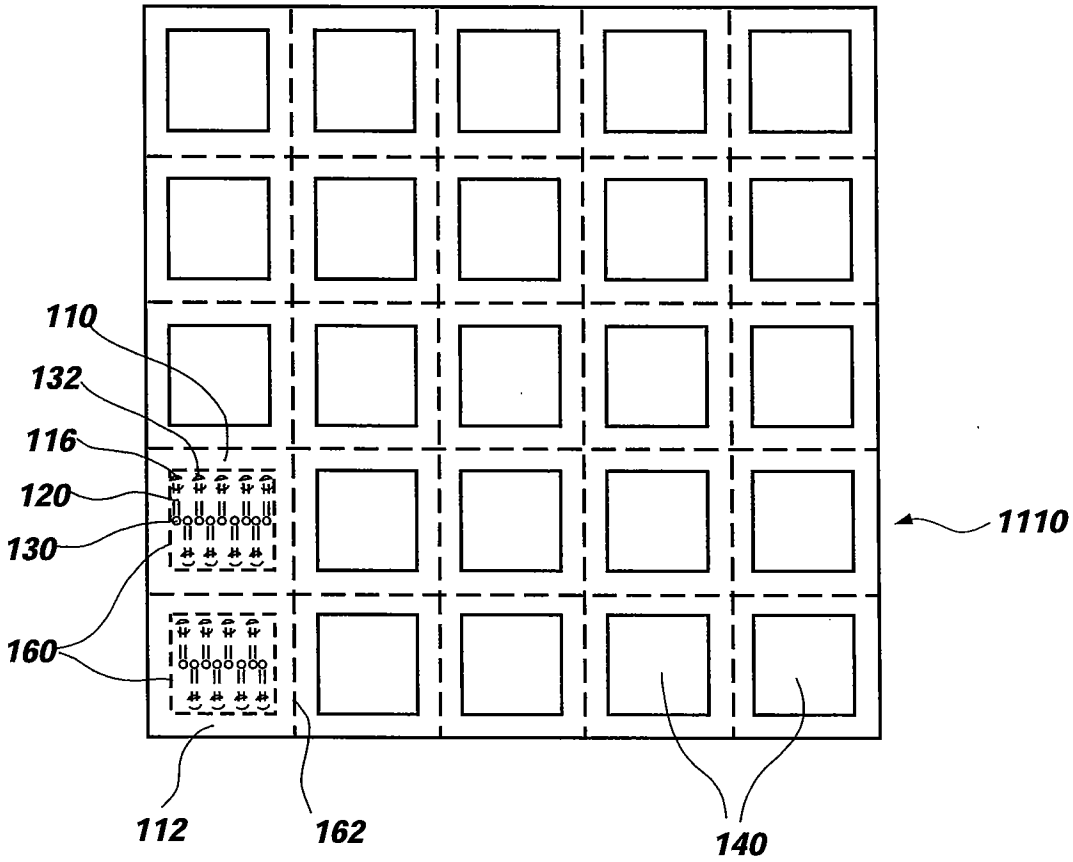

110
132
116
120
130
160
1110
112
162
140

FIG. 8

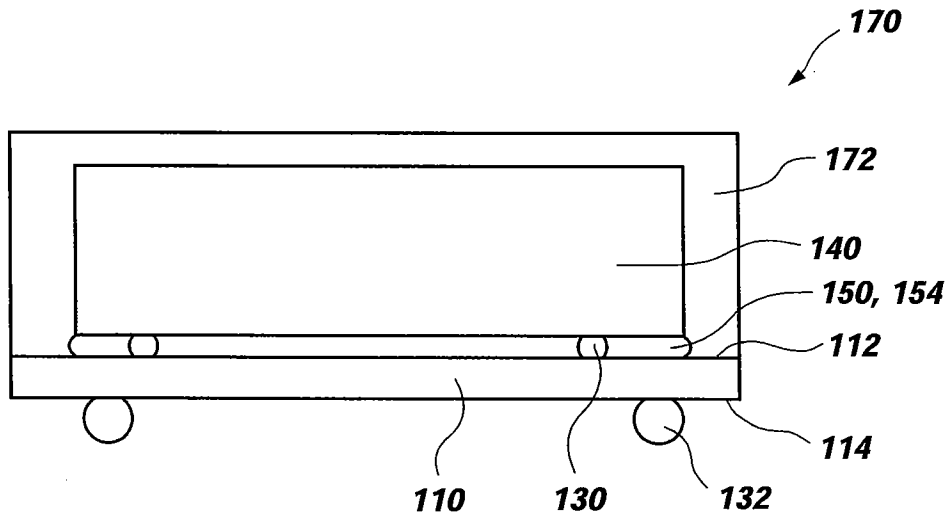

170
172
140
150, 154
112
114
110
130
132

FIG. 9

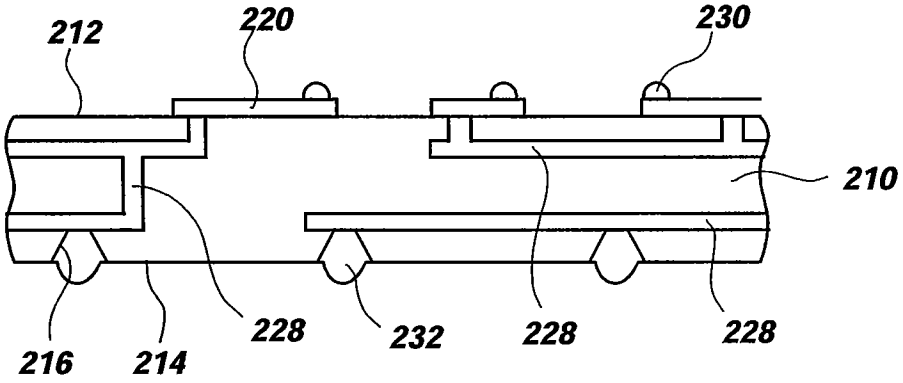

212
220
230
210
228
232
228
228
216
214

FIG. 10

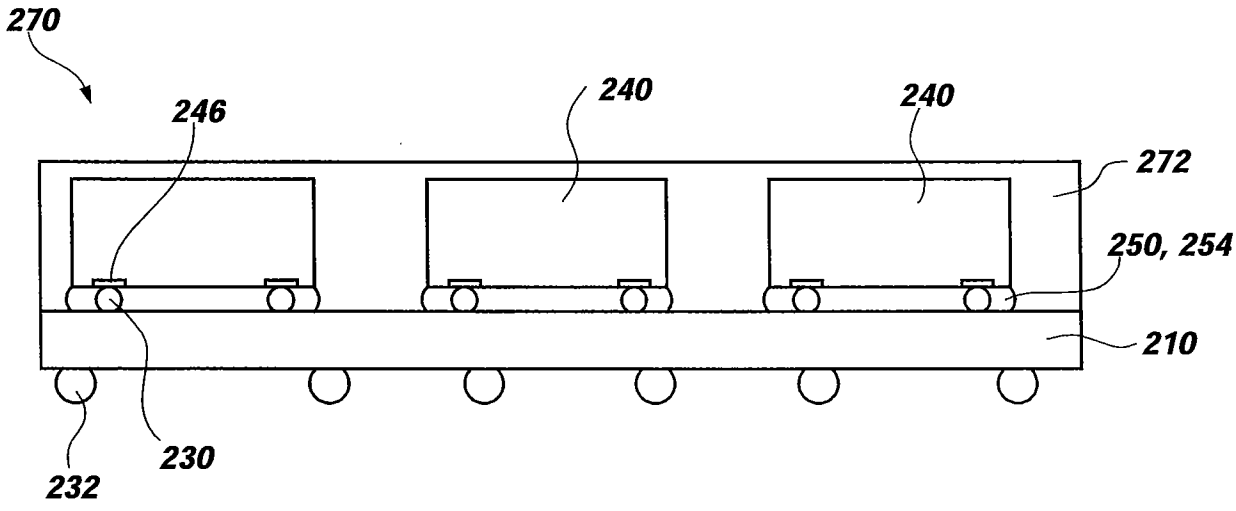

270
246
240
240
272
250, 254
210
230
232

FIG. 11

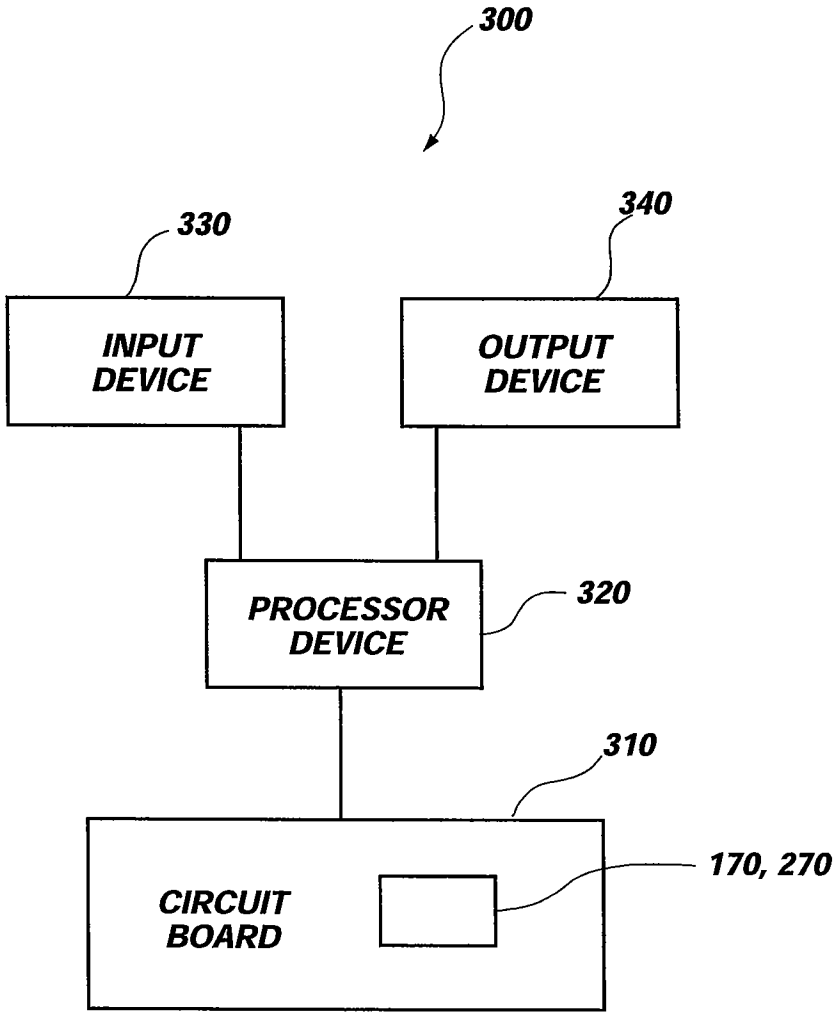

300
330
340
INPUT DEVICE
OUTPUT DEVICE
PROCESSOR DEVICE
320
310
CIRCUIT BOARD
170, 270

FIG. 12