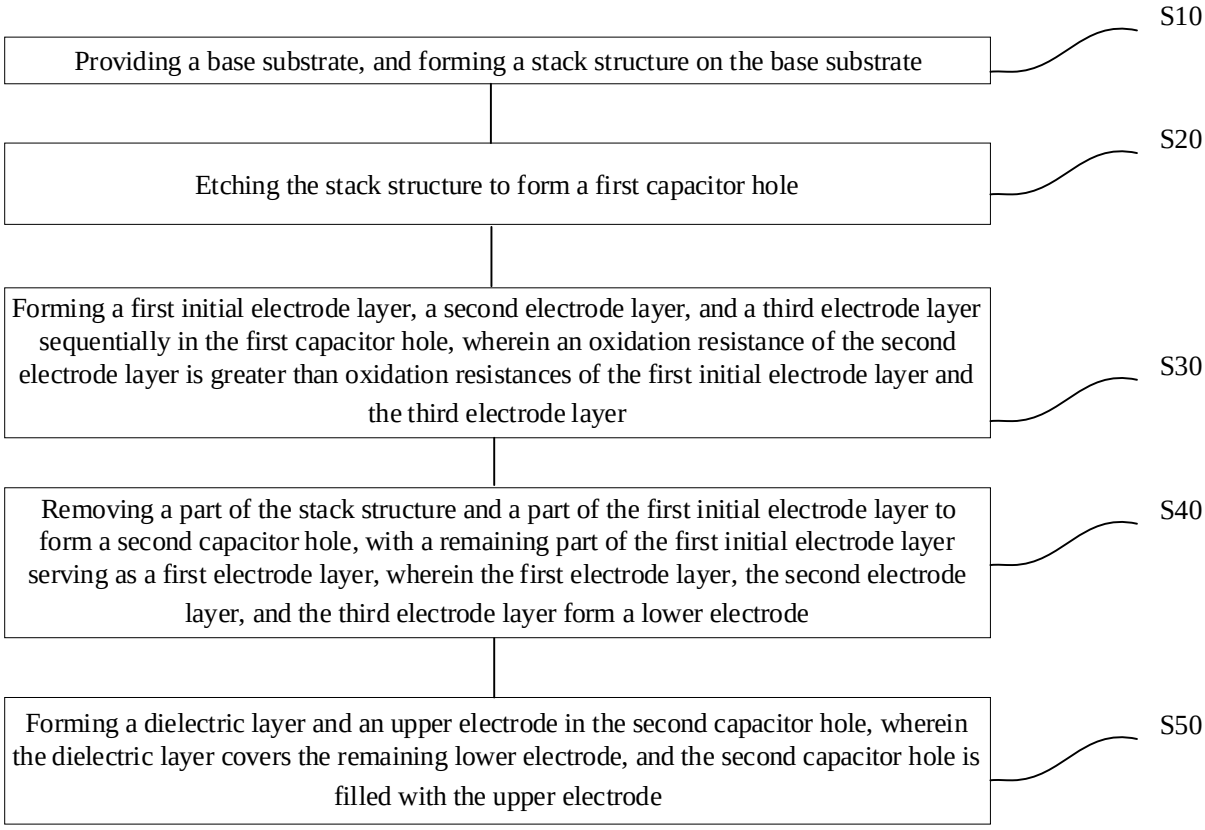

S10
Providing a base substrate, and forming a stack structure on the base substrate
S20
Etching the stack structure to form a first capacitor hole
S30
Forming a first initial electrode layer, a second electrode layer, and a third electrode layer sequentially in the first capacitor hole, wherein an oxidation resistance of the second electrode layer is greater than oxidation resistances of the first initial electrode layer and the third electrode layer
S40
Removing a part of the stack structure and a part of the first initial electrode layer to form a second capacitor hole, with a remaining part of the first initial electrode layer serving as a first electrode layer, wherein the first electrode layer, the second electrode layer, and the third electrode layer form a lower electrode
S50
Forming a dielectric layer and an upper electrode in the second capacitor hole, wherein the dielectric layer covers the remaining lower electrode, and the second capacitor hole is filled with the upper electrode

FIG. 1

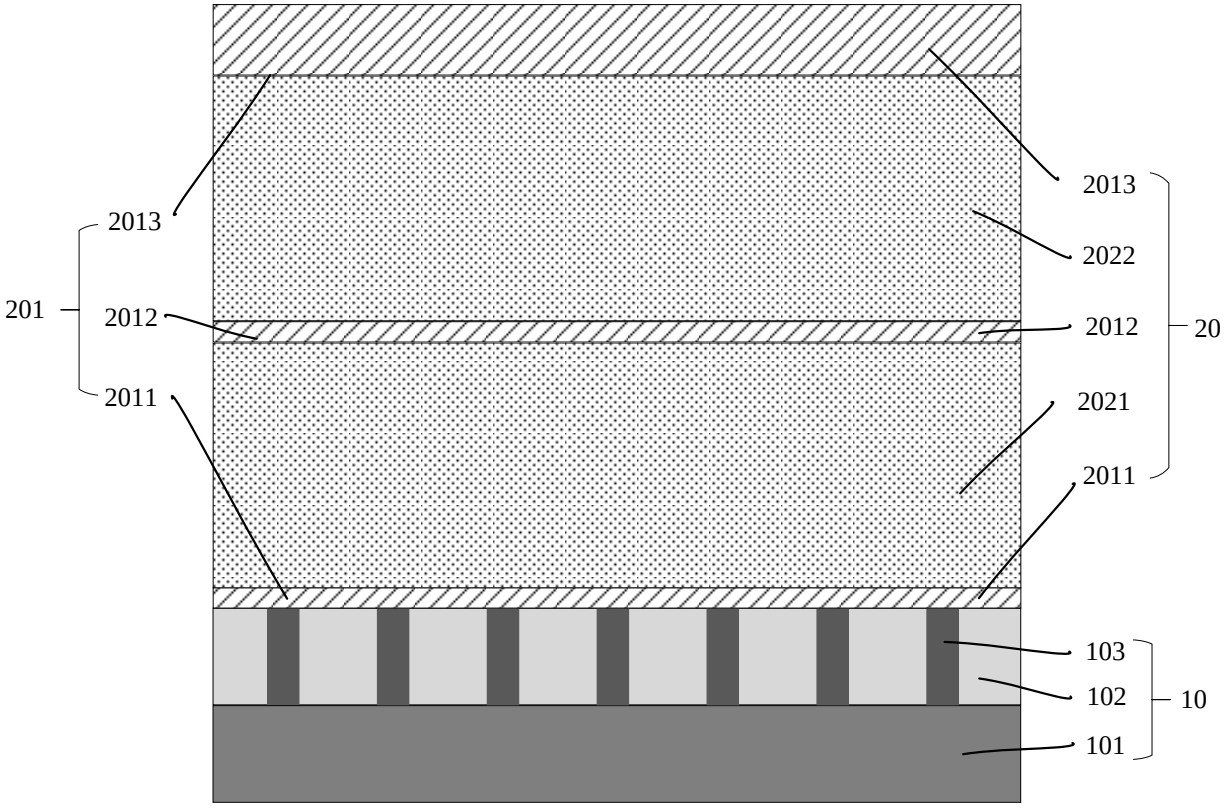

2013
2013
201
2012
2022
2012
20
2011
2021
2011
103
102
10
101

FIG. 2A

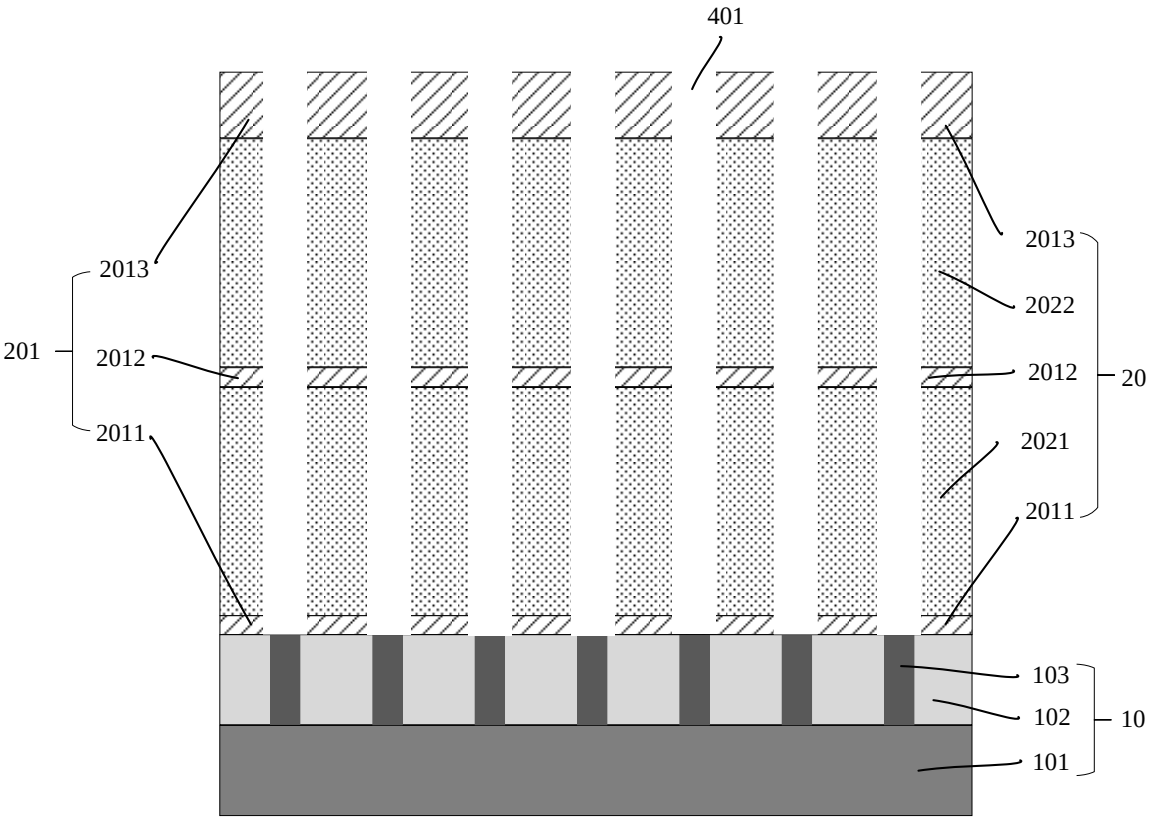

401
2013
201
2012
2011
2013
2022
2012
20
2021
2011
103
102
10
101

FIG. 2B

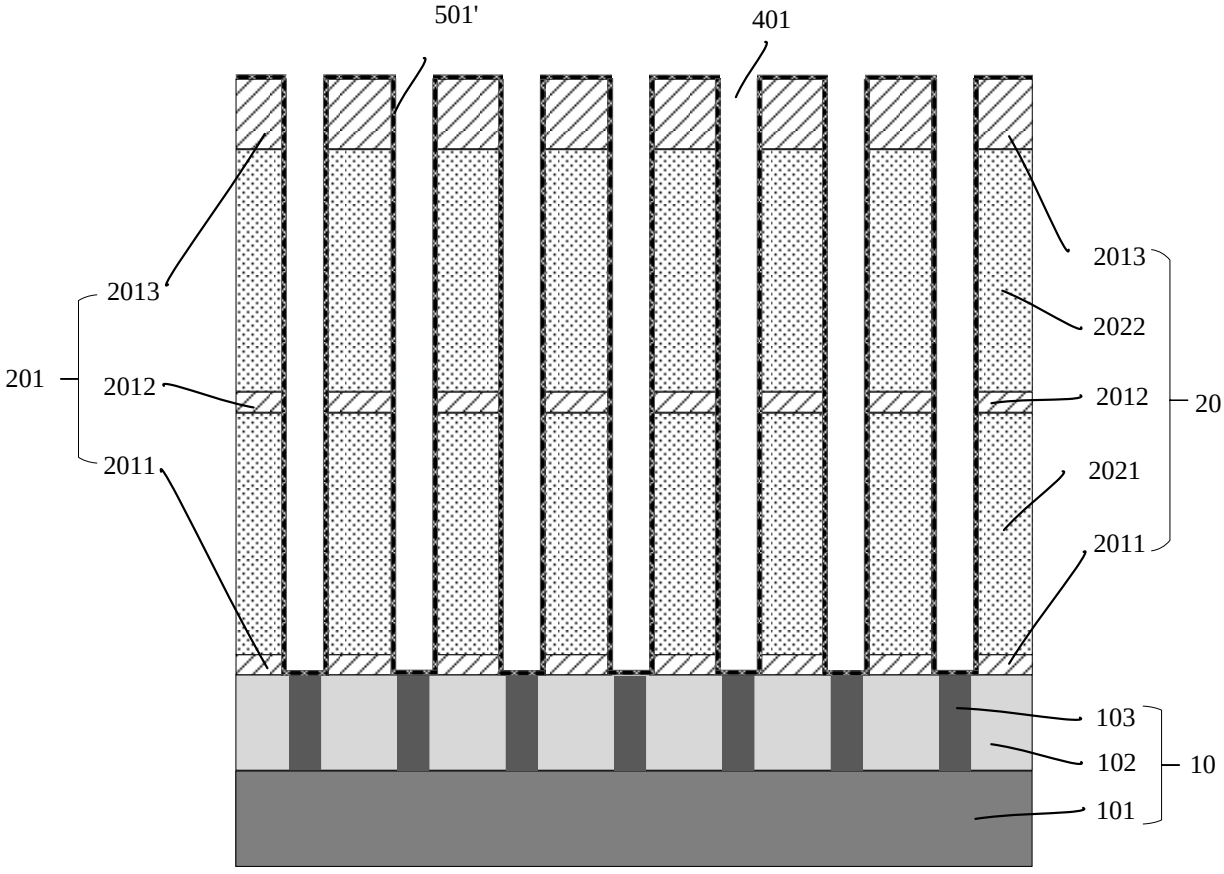

501'
401
2013
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2012
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2022
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2021
2011
103
102
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101

FIG. 2C

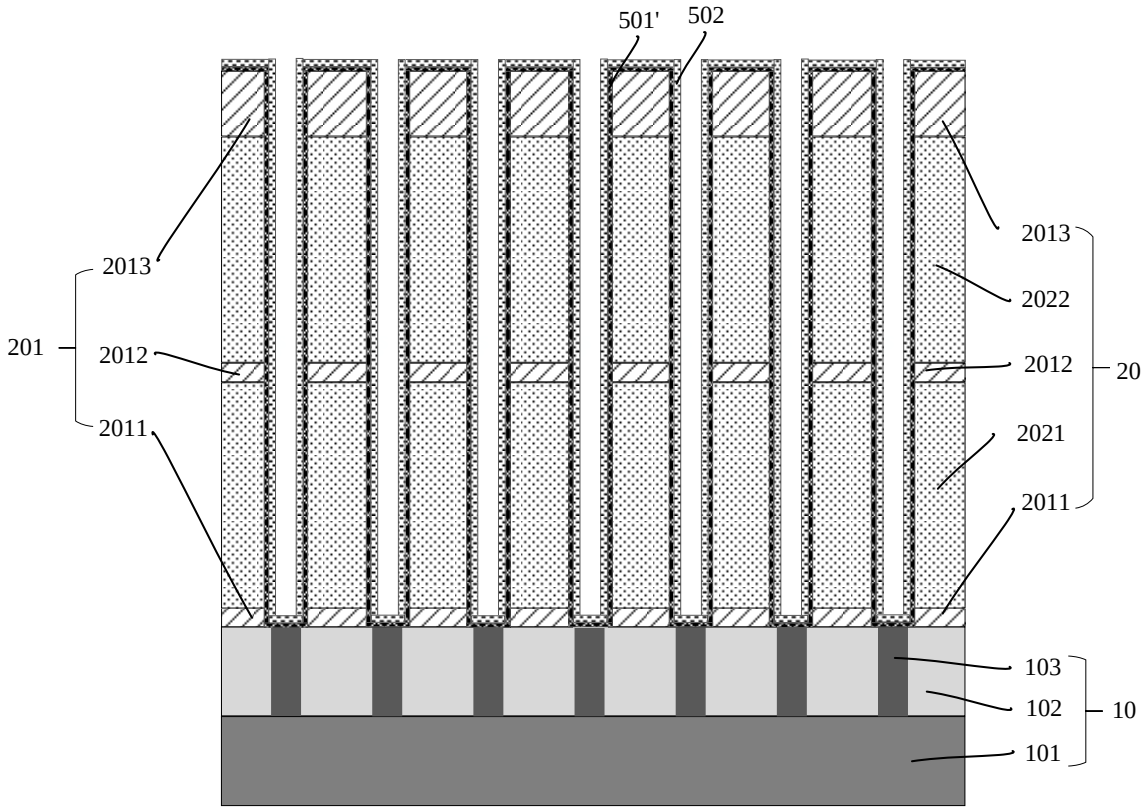

501'
502
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2022
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2012
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2011
2021
2011
103
102
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101

FIG. 2D

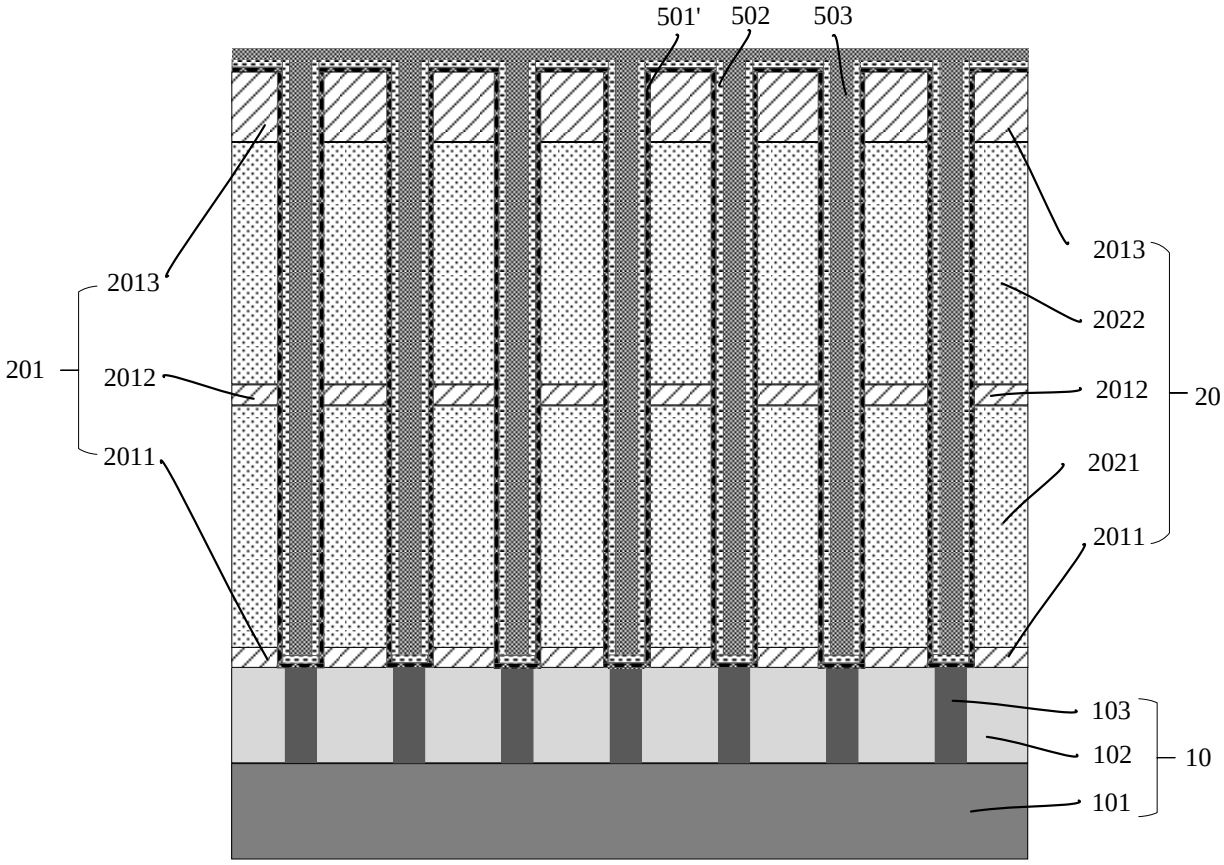

501'
502
503
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2013
2022
201
2012
2012
20
2011
2021
2011
103
102
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101

FIG. 2E

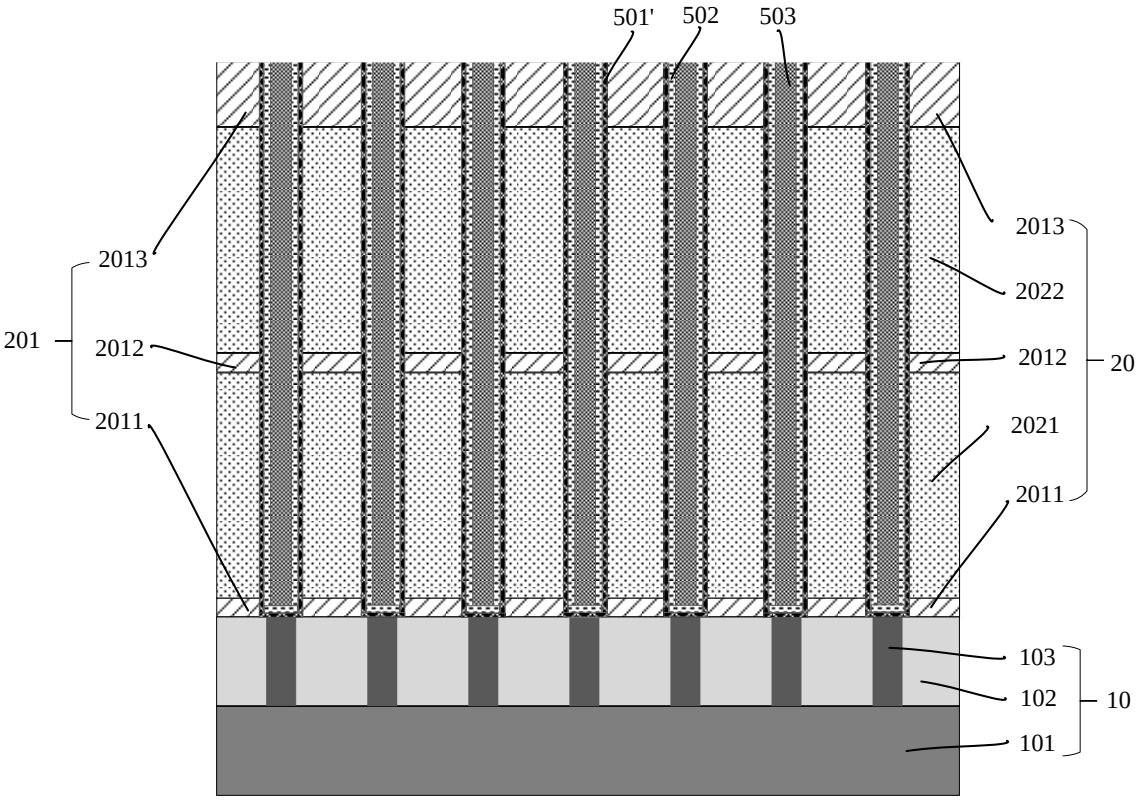

501'
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2013
2022
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2012
2012
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2011
2021
2011
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102
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101

FIG. 2F

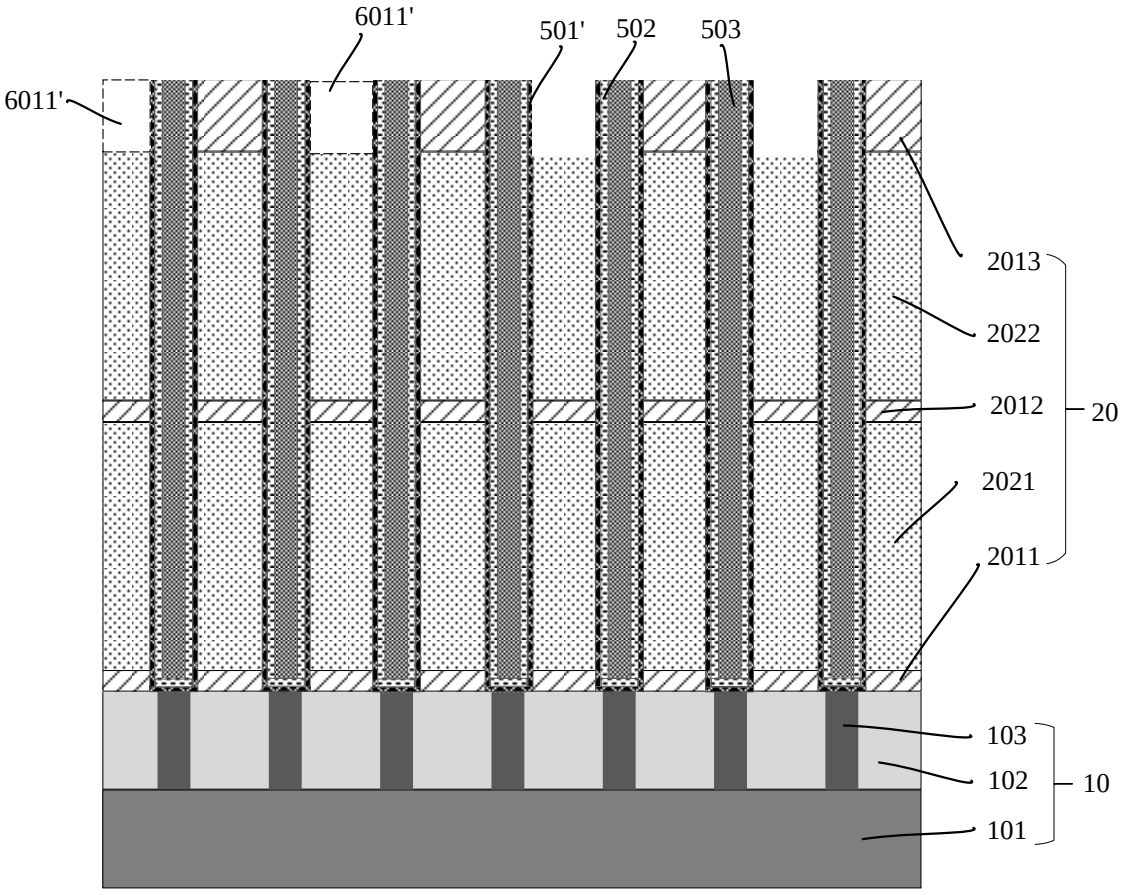

6011'
501'
502
503
6011'
2013
2022
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2021
2011
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102
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FIG. 2G

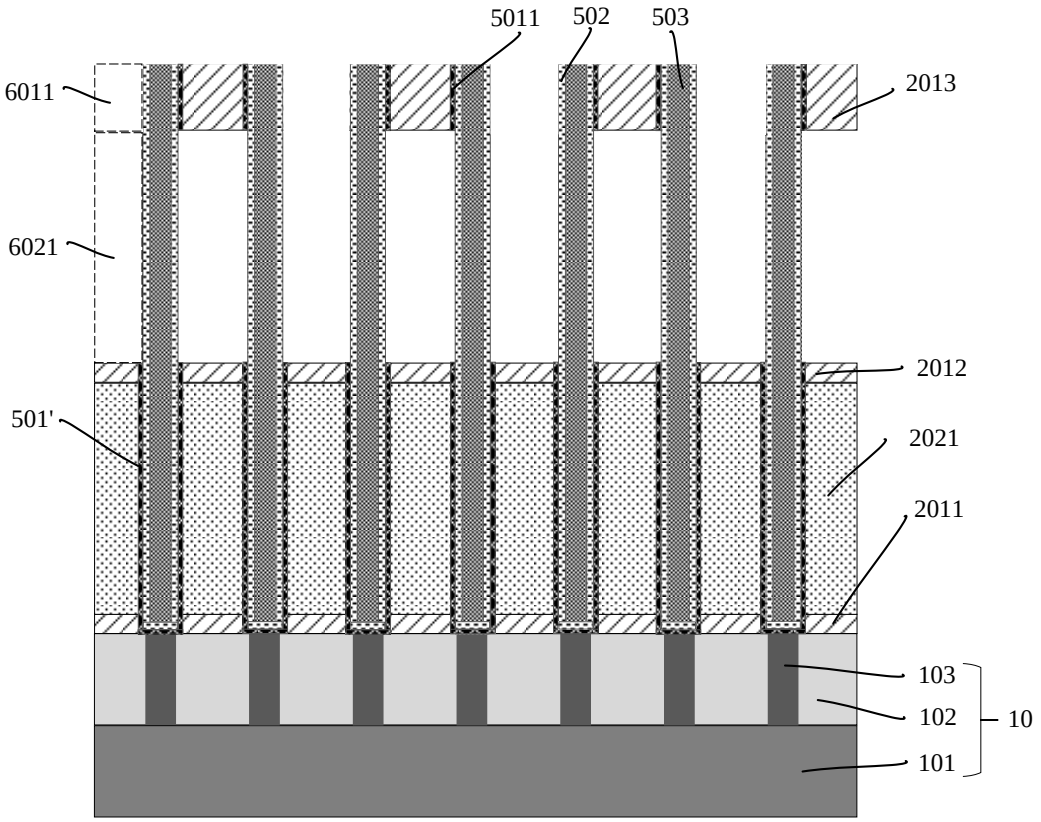

5011
502
503
6011
2013
6021
2012
501'
2021
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FIG. 2H

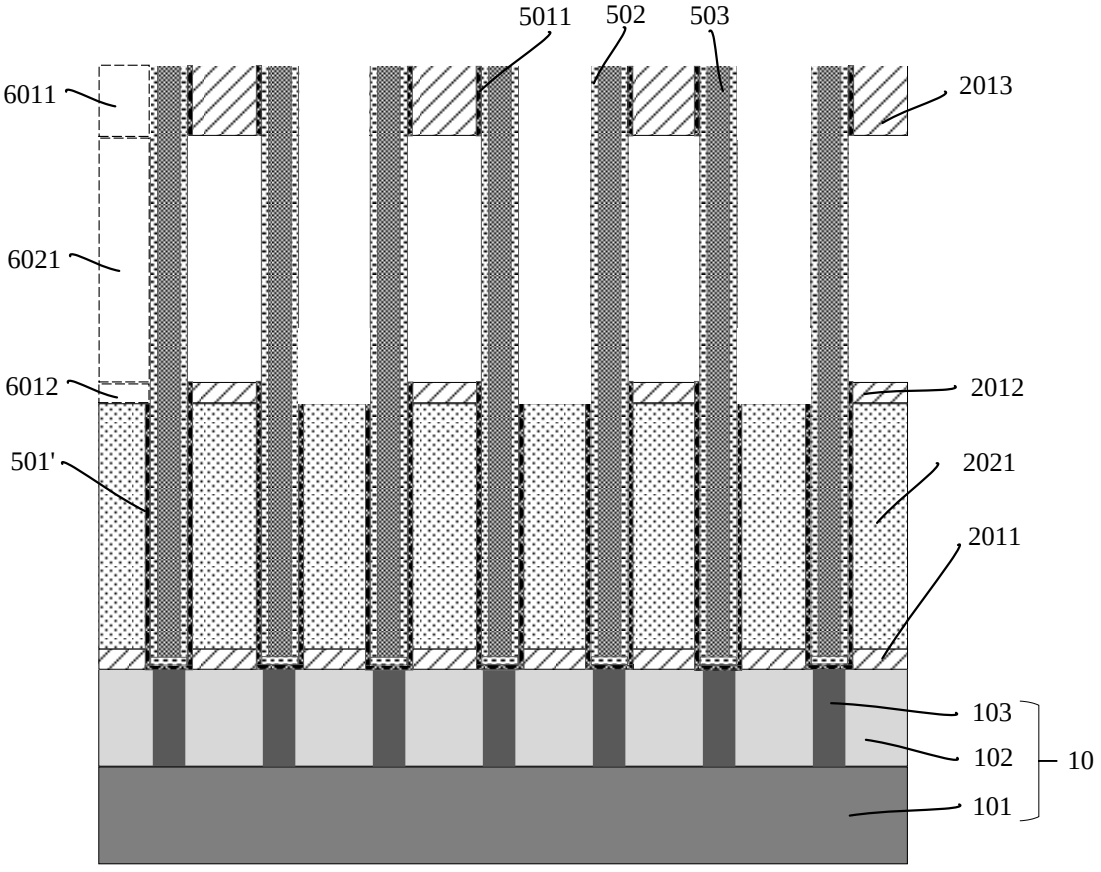

5011
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6011
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6021
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501'
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FIG. 2I

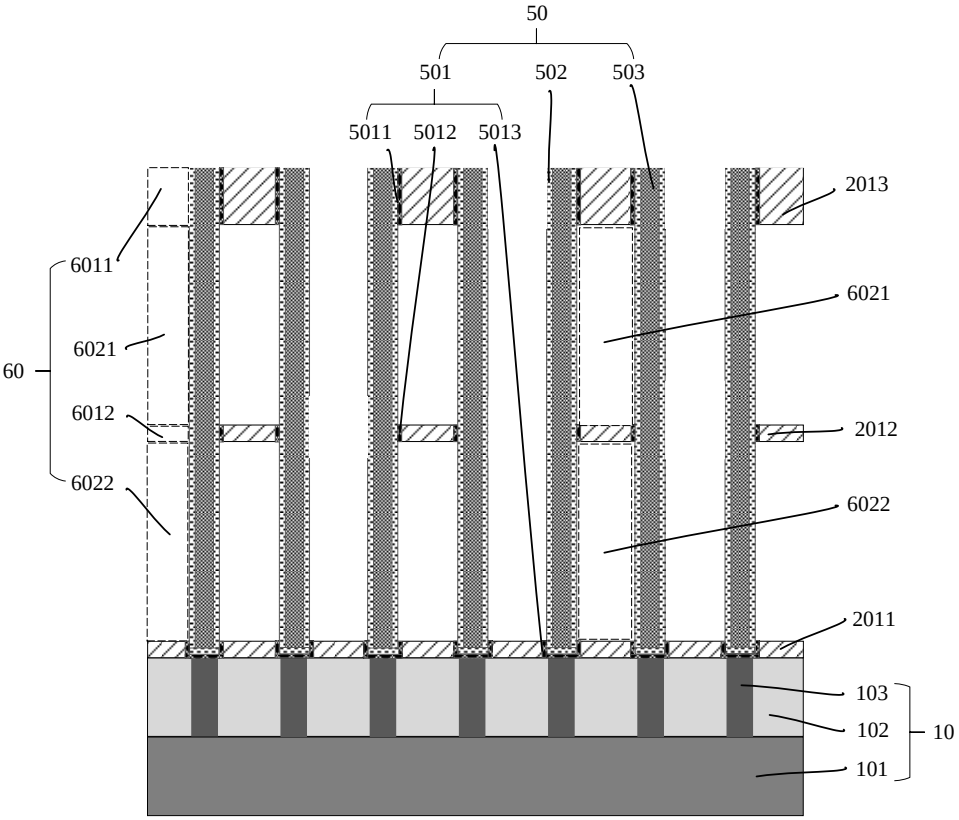

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FIG. 2J

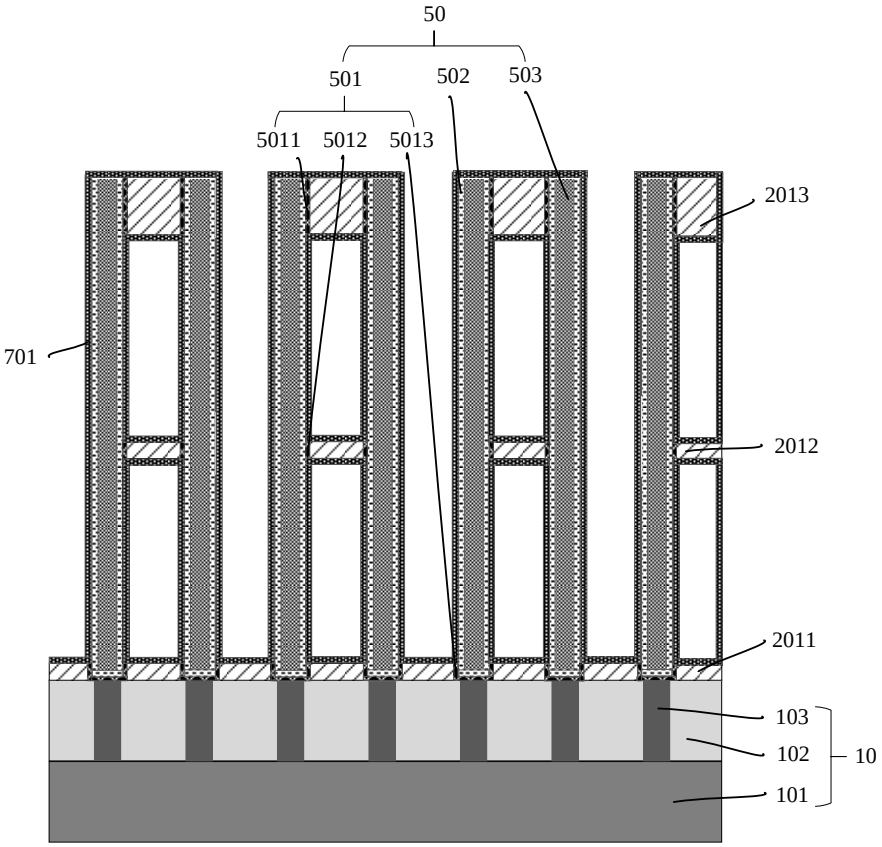

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FIG. 2K

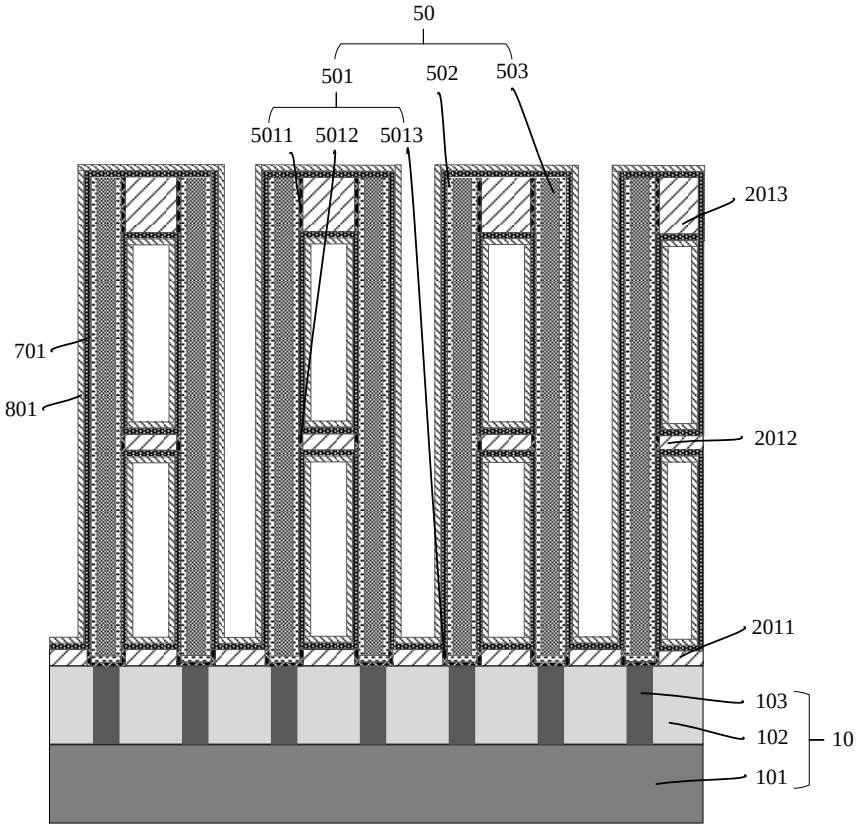

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101

FIG. 2L

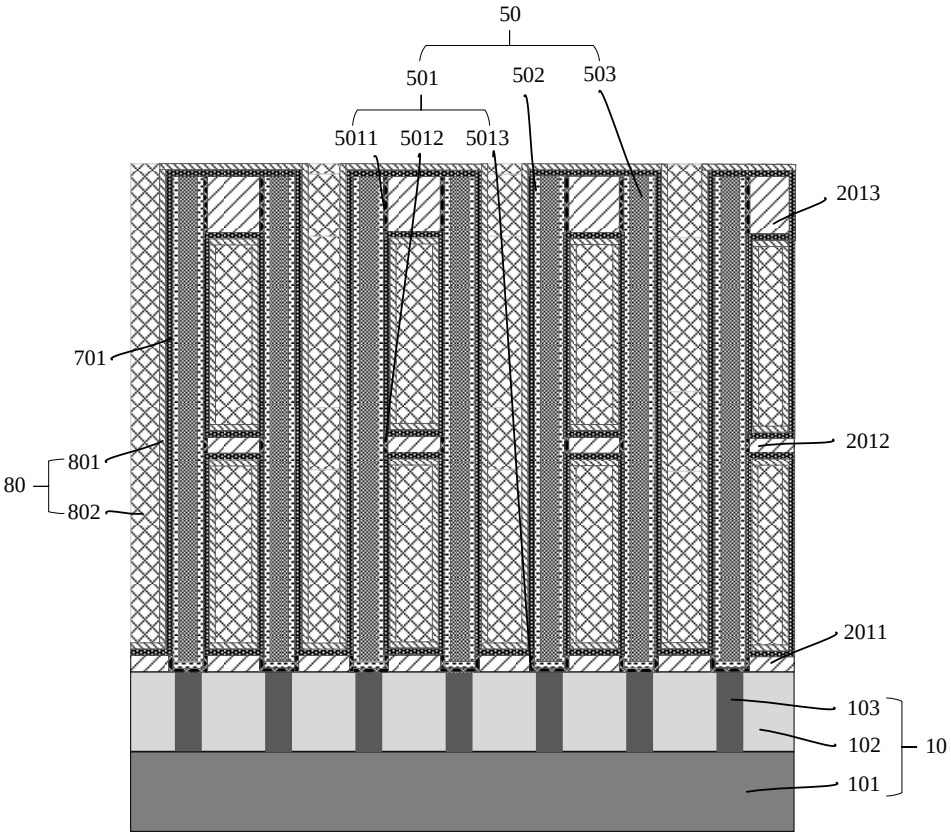

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FIG. 2M

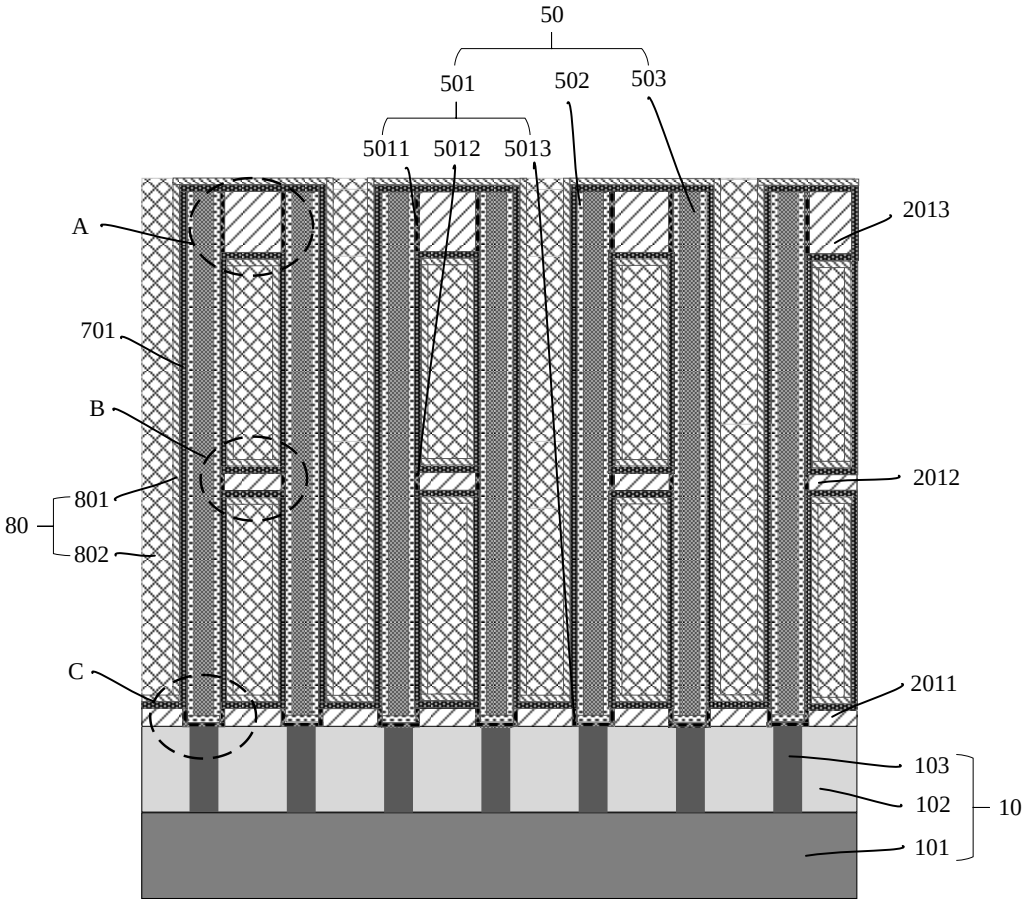

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C
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FIG. 3

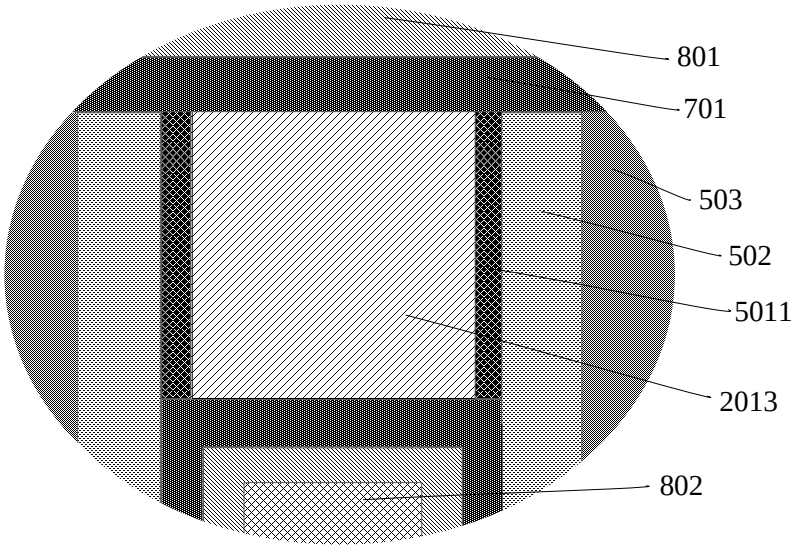

801
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FIG. 4

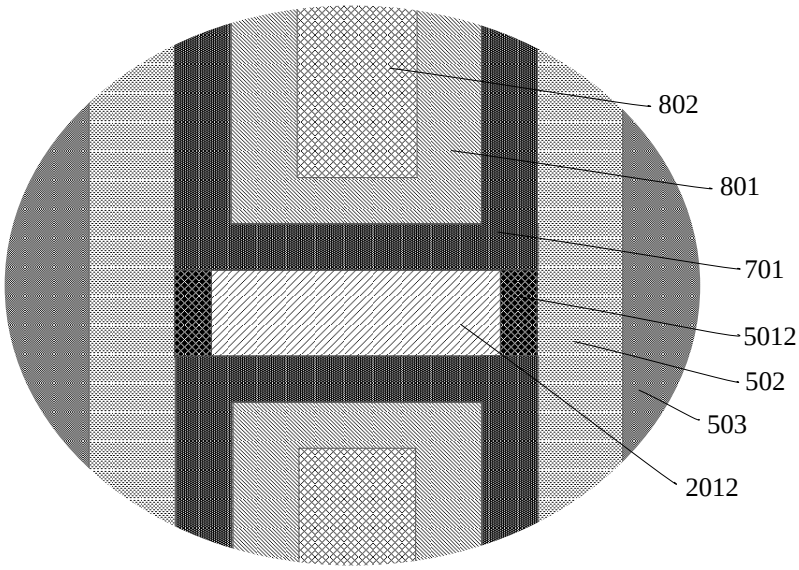

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FIG. 5

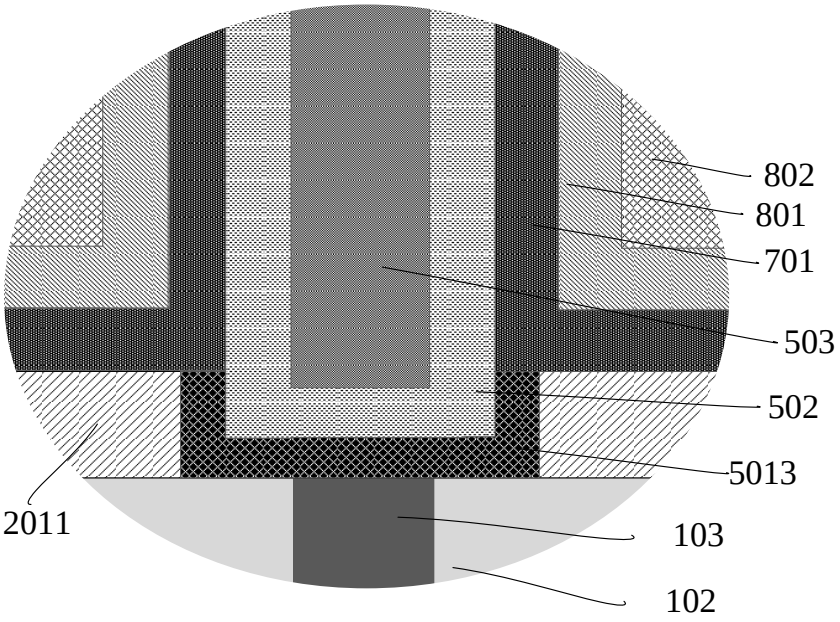

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FIG. 6