ABSTRACT

DATA READING CIRCUIT

There is provided a data reading circuit which is low in current consumption. In a read period, a signal (Φ2) is low, and hence an NMOS transistor (14) turns off. Accordingly, no current flows in the NMOS transistor (14). Further, data (D2) is high, and hence an output voltage of an inverter (23) becomes low, and an NMOS transistor (32) turns off. Accordingly, no current flows in the NMOS transistor (32). Further, in a PMOS transistor (31), a power supply voltage (VDD) is applied to a source and a drain thereof, and hence no current flows. As a result, no current flows in the data reading circuit during a read period after a data holding operation of a latch circuit (21) has been completed (after time (t4)), and hence the current consumption of the data reading circuit is reduced accordingly.

-Fig.1-