DESCRIPTION

MEMORY ARRAYS AND METHODS OF FABRICATING MEMORY ARRAYS

TECHNICAL FIELD

This invention relates to memory arrays and to methods of fabricating memory arrays.

BACKGROUND ART

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is typically fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or non-volatile. Non-volatile memory cells can store data for extended periods of time, and in many instances including when the computer is turned off. Volatile memory dissipates and therefore requires to be refreshed/rewritten, and in many instances including multiple times per second.

One example volatile semiconductor memory is dynamic random access memory (DRAM), with an exemplary prior art DRAM cell being shown in Fig. 1. Fig. 1 depicts an individual/single DRAM cell 10 comprising a field effect access transistor 12 and a storage capacitor 14. Field effect transistor 12 includes a pair of source/drain regions 15, 16, and a gate 17. Source/drain region 16 is depicted as connecting with storage capacitor 14, while source/drain region 15 electrically connects with a bit line 18. Gate 17 is typically in the form of an elongated word line forming gates of several field effect transistors formed in a "row". Bit line 18 typically connects with a plurality of source/drain regions 15 of field effect transistors formed in a "column" which is generally typically orthogonal to a gate/word line row. In many instances, pairs of immediately adjacent field effect transistors might share a common source/drain region 15 to which a bit line electrically connects.

Dual transistor DRAM cells utilizing capacitors have also been proposed, for example those disclosed in U.S. Patent No. 6,818,937.

While the invention was motivated in addressing the above identified issues, it is in no way so limited. The invention is only limited by the

accompanying claims as literally worded, without interpretative or other limiting reference to the specification, and in accordance with the doctrine of equivalents.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a schematic of a prior art DRAM cell.

Fig. 2 is a diagrammatic perspective cutaway view of a substrate fragment and partial schematic comprising a memory cell in accordance with various aspects of the invention.

Fig. 3 is a schematic of a single/individual memory cell in accordance with an aspect of the invention.

Fig. 4 is an expanded diagrammatic top plan view of a substrate fragment comprising memory cells such as that depicted in Fig. 2.

Fig. 5 is a diagrammatic sectional view taken through line 5-5 in Fig. 4.

Fig. 6 is a diagrammatic sectional view taken through line 6-6 in Fig. 4.

Fig. 7 is a further expanded diagrammatic top plan view of a substrate fragment in accordance with aspects of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Aspects of the invention encompass memory arrays and methods of fabricating memory arrays. Memory array constructions might be fabricated by any method, and not necessarily limited by the methods of fabricating a memory array as disclosed herein. Likewise, methods of fabricating a memory array are not necessarily limited by the memory array constructions as disclosed herein.

Exemplary aspects of memory array constructions are initially described with reference to Fig. 2. In various implementations, memory arrays fabricated in accordance with the invention comprise a plurality of memory cells formed on a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material,

including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Exemplary preferred semiconductor substrates include bulk semiconductor substrates, for example bulk monocrystalline silicon. Aspects of the invention might also, of course, be utilized in semiconductor-on-insulator substrates and any other substrate (whether existing or yet-to-be developed) within or upon which an operable memory array could be fabricated.

The memory array will comprise a plurality of memory cells, with an exemplary individual memory cell in accordance with various implementations of the invention being indicated generally with reference numeral 20 in Fig. 2. Not all memory cells of a memory array necessarily have identical construction, but may and typically include a plurality of substantially identically constructed individual memory cells. Regardless and by way of example only, Fig. 2 depicts a semiconductor substrate 22 comprising semiconductive material 23. Semiconductive material 23 might comprise bulk semiconductor material, for example bulk monocrystalline silicon which has been suitably background doped with a conductivity-enhancing impurity either globally or relative to smaller isolated regions and/or wells. Other semiconductor materials and substrates are, of course, contemplated. By way of example only, exemplary background doping of semiconductive material 23 is of p-type of a suitable dose/concentration such that channel regions of n-type field effect transistors can be formed upon gate activation.

Individual memory cell 20 includes a first field effect transistor 24 and a second field effect transistor 26. Each comprises a gate, a channel region, and a pair of source/drain regions. For example, first field effect transistor 24 is depicted as comprising a gate 28, and second field effect transistor 26 is depicted as comprising a gate 30. In the depicted and but one exemplary preferred embodiment, gates 28 and 30 are received within openings 29 and 31, respectively, formed within semiconductive material 23 of semiconductor substrate 22. In one implementation, openings 29 and 31

are in the form of elongated trenches, and conductive material received therewithin will form word lines/gates for multiple memory cells. By way of example only, exemplary open widths of openings 29, 31 and the spacing between the depicted adjacent openings are preferably less than or equal to 500 Angstroms. An exemplary depth for the depicted trench openings 29 and 31 from an outermost surface of semiconductive material 23 is from 100 Angstroms to 500 Angstroms. Exemplary preferred conductive materials for gates 28 and 30 are conductively doped semiconductive materials and/or metal. In the context of this document, "metal" defines any of an elemental metal, an alloy or mixture of elemental metals, or conductive metal compounds. By way of example only, one preferred conductive material for gates 28 and 30 is titanium nitride.

A gate dielectric 32 is depicted as lining openings 29 and 31. Any suitable existing or yet-to-be developed dielectric is usable, with silicon dioxide being but one example, and of an exemplary preferred thickness range of from 30 Angstroms to 80 Angstroms.

First field effect transistor 24 comprises a pair of source/drain regions 34 and 36, and second field effect transistor 26 comprises a pair of source/drain regions 38 and 40. Such can be formed by any of ion implanting, diffusion doping, etc., and any other process whether existing or yet to be developed. An exemplary preferred thickness of such source/drain regions 36, 36, 38 and 40 is less than or equal to 500 Angstroms from an outer surface of material 23. In the depicted exemplary preferred embodiment, one of the pair of source/drain regions is received laterally intermediate gates 28 and 30, and is shared by first and second transistors 24 and 26. In the depicted exemplary embodiment, source/drain region 36 of first field effect transistor 24 and source/drain region 40 of second field effect transistor 26 constitute the same source/drain region and which is shared by such first and second field effect transistors. In one implementation, and as shown, other source/drain region 34 of pair 34/36 is received laterally outward of gate 28, and other source/drain region 38 of pair 38/40 is received laterally outward of gate 30. In the depicted exemplary preferred embodiment, shared source/drain region 36/40 is received both laterally intermediate gates 28 and 30, and elevationally outward thereof. Further in the depicted preferred embodiment, each of

other source/drain regions 34 and 38 is received elevationally outward of gates 28 and 30, and with the depicted source/drain regions being formed in one preferred implementation within bulk semiconductive material 23. However, other constructions are of course contemplated, including, by way of example only, elevated source/drains.

First field effect transistor 24 comprises a channel region 42 and second field effect transistor 26 comprises a channel region 44. In combination, and it but one preferred embodiment, such form a general W-shape in the depicted cross section. Each channel region 42, 44 comprises a switchable current path 46 in at least one substrate cross-section which extends between shared source/drain region 36/40 and the respective other source/drain region 34 or 38. Preferably as shown, each current path 46 comprises interconnected first and second substantially vertical segments 48 and 50. In the depicted exemplary embodiment, first and second substantially vertical segments 48 and 50, respectively, can be considered as comprising elevationally inner end portions 52, and an interconnecting segment 56 received between first substantially vertical segment 48 and second substantially vertical segment 50 proximate elevationally inner end portions 52. In the depicted exemplary implementation, interconnecting segment 56 is substantially horizontally oriented relative to the depicted general substrate orientation.

Fig. 2 schematically depicts a conductive data line 60 electrically connecting with each of the other source/drain regions 34, 38 of source/drain region pair 34/36 and source/drain region pair 38/40. In one exemplary preferred embodiment, conductive data line 60 is received elevationally outward of gates 28 and 30. Fig. 2 also schematically depicts a charge storage device 62 electrically connecting with shared source/drain region 36/40. In the depicted exemplary preferred embodiment, charge storage device 62 comprises a capacitor.

Fig. 2 schematically depicts conductive data line 60 and charge storage device 62 electrically connecting with their respective source/drain regions, and such might occur in any manner or in any implementation. In one preferred aspect, charge storage device 62 is received elevationally outward of gates 28 and 30, and in one preferred aspect conductive data line 60 is received elevationally outward of gates 28 and 30. Further in one

preferred and exemplary aspect, charge storage device 62 is received elevationally outward of conductive data line 60, for example in one preferred implementation as will be exemplified in the continuing discussion. Further in one preferred implementation, individual memory cells 20 comprise DRAM cells, with conductive data line 60 comprising a bit line.

In one preferred implementation, conductive material electrically interconnects gates 28 and 30 of first and second transistors 24 and 26, respectively. For example, Fig. 2 diagrammatically depicts a conductive material region or segment 64 which electrically connects conductive gates 28 and 30. In one exemplary implementation, conductive material 64 which interconnects with gates 28 and 30 is received within a trench which has been formed within semiconductor substrate 22, and even more preferably within semiconductive material 23 of semiconductor substrate 22. Material 23 and likely peripheral insulative material 32 are not shown proximate conductive material 64 for clarity in the depicted diagrammatic perspective cut-away in Fig. 2.

One aspect of the invention includes a memory array which comprises a plurality of memory cells formed on a semiconductor substrate. Individual of the memory cells comprise first and second field effect transistors respectively comprising a gate, a channel region, and a pair of source/drain regions. The gates of the first and second field effect transistors are hardwired together. A conductive data line is hardwired to two of the source/drain regions, and a charge storage device is hardwired to at least one of the source/drain regions other than the two. For example, and by way of example only, Fig. 2 diagrammatically depicts an exemplary preferred construction of an individual memory cell of such a memory array, and Fig. 3 schematically depicts such an exemplary individual memory cell.

In one preferred implementation of such aspect, one of the source/drain regions is received laterally between the gates. In one preferred implementation, one of the source/drain regions is shared by the first and second field effect transistors, and in one preferred aspect the charge storage device is connected to the one shared source/drain region. In one preferred implementation of such aspect, the gates are hardwired together by conductive material received in at least one trench formed within semiconductive material of the semiconductor substrate and extending

between the gates. However, other aspects of electrically interconnecting gates are contemplated, for example by a separate interconnecting line or layer, or by any other manner whether existing or yet-to-be developed, and for any aspect of this disclosure. In one preferred implementation, each channel region comprises a current path in at least one cross-section extending between source/drain regions which comprises interconnected first and second substantially vertical segments. Any other exemplary attribute of the first-described Fig. 2 embodiment is also contemplated.

By way of example only, Figs. 4-6 depict but exemplary additional construction with respect to that of Fig. 2 incorporating conductive data line and charge storage device structures. Like numerals from Fig. 2 are utilized where appropriate, with additional structure being indicated with additional numerals. Insulative caps 70 are received over conductive gates 28, 30. An exemplary preferred material is silicon nitride. An interlevel dielectric 72 has been formed elevationally outward of semiconductive material 23. An exemplary material is silicon dioxide which might be doped or undoped. Conductive data line contact openings 74 have been formed therethrough to source/drain regions 34 and 38. Conductive material 75 has been deposited and patterned to form conductive data line 60. Such might be formed by a damascene-like process, or by a deposition and subtractive patterning and etch process, by way of examples only. One exemplary preferred method includes the deposition of one or more conductive materials 75, followed by subsequent patterning and subtractive etching thereof. An insulative material 76 might be deposited thereover prior or subsequent to patterning material 75, and the same or different insulative material 76 deposited and subsequently anisotropically etched to form insulative conductive data line sidewall spacers (not shown). Etching to form data line 60 might effectively recess material 75 within contact openings 74 as depicted in the Fig. 5 cross-section, and with some insulative spacer-forming material 76 subsequently being deposited therein over material 75 in the Fig. 5 cross-section.

Another interlevel dielectric layer 78 (Fig. 5) has been deposited. Exemplary preferred materials include doped or undoped silicon dioxide. A contact opening 80 has been etched through interlevel dielectric layer 78 and 72 to shared source/drain region 36/40. Conductive plugging

material(s) 81 is received therein. Charge storage device 62 is depicted as comprising a capacitor having a storage node electrode 82 electrically connecting with conductive plug 81 received within contact opening 80. A capacitor dielectric 84 is received outwardly and over storage node electrode 82, and an outer conductive cell plate electrode 86 has been formed thereover. Any exemplary or yet-to-be developed materials are, of course, contemplated for capacitor dielectric 84 and conductive capacitor electrodes 82 and 86.

The depicted Figs. 2 and Figs. 4-6 constructions are but exemplary depictions of an individual memory cell and of a memory array in accordance with various aspects of the invention. A person of skill in the art will readily appreciate that such might be manufactured in any of numerous manners, and whether existing or yet-to-be developed. By way of example only, exemplary inventive aspects of methods of fabricating memory arrays are described with reference to Fig. 7. Fig. 7 is a top view of a semiconductor substrate comprising, by way of example only, a memory array area 100. Alternating lines 101 of active area regions and lines 102 of trench isolation regions have been formed within a suitable semiconductor substrate, for example substrate 22 of the first-described embodiment. A series of race track-shaped trenches 104 have been etched into active area regions 101 and trench isolation regions 102 generally orthogonal to the alternating lines of active area regions 101 and trench isolation regions 102. By way of example only, such can be in the form of openings 29 and 31 of Fig. 2 for the fabrication of individual memory cells. Conductive material is formed within race track-shaped trenches 104 to form a pair of electrically connected word lines with respect to individual of the race track-shaped trenches. Exemplary preferred materials are those described above with respect to gates 28 and 30. Accordingly and also in one exemplary preferred embodiment, a gate dielectric (not shown for clarity in Fig. 7) would be formed to line the exemplary depicted race track-shaped trenches 104 prior to provision of gate material 28/30.

Source/drain regions could be formed within the active area regions laterally internal of race track-shaped trenches 104 and laterally external of race track-shaped trenches 104. By way of example only, and with reference to the Fig. 2 embodiment, an exemplary such laterally internal

source/drain region is designated with 36/40, and exemplary such laterally external source/drain regions are designated with numerals 34 and 38 in Fig. 7.

Conductive data lines (not shown for clarity in Fig. 7) are formed in electrical connection with the source/drain regions received laterally external of the race track-shaped trenches, for example to source/drain regions 34 and 38 of the exemplary Figs. 2 and 4-6 embodiments. A charge storage device (not shown for clarity in Fig. 7) is formed in electrical connection with respective of the source/drain regions received laterally internal of race track-shaped trenches 104. For example and by way of example only, capacitors or other devices might be formed relative to source/drain regions 36/40 of the Figs. 2 and 4-6 embodiments. Exemplary separate conductive contacts 110 are shown, by way of example only, received externally of memory array 100 for making electrical connection with respect to conductive material (i.e., conductive materials 28 and 30 with respect to each trench 104) for accessing/activating each word/gate line pair.

An aspect of the invention encompasses a method of fabricating a memory array which comprises forming alternating lines of active area regions and trench isolation regions within a semiconductor substrate. Exemplary such alternating lines are depicted in Fig. 7, and by way of example only. A series of pairs of trenches are etched into the active area regions and the trench isolation regions generally orthogonal to the alternating lines of active area regions and trench isolation regions. By way of example only, exemplary depicted trench openings 29 and 31 in Fig. 7 are exemplary such series of pairs of trenches, and independent of whether race track-shaped trenches are formed.

Regardless in one implementation, at least one interconnecting trench is etched somewhere within the semiconductor substrate which interconnects individual of the trenches of each pair. For example and by way of example only, each of the exemplary depicted half-circle/arch trench sections 112 are an exemplary such interconnecting trench which interconnects respective trench pairs 29 and 31. Only one of such trenches 112 might be fabricated or alternate shaped or configuration trenches might be etched. Further, the exemplary pairs of trenches might be

etched at the same time and/or using a common masking step, or separately with respect to masking step and/or etching.

Conductive material is formed within the pairs of trenches and the interconnecting trench to form a pair of electrically connected word lines with respect to individual of the pairs of trenches. Such might comprise depositing at least some conductive material within the pairs of trenches and the interconnecting trench at the same time, or at totally at different times. (Interconnecting material/region 64 in Fig. 2 corresponds to such interconnecting trench and conductive material)

Source/drain regions are formed within the active area regions intermediate individual of the trenches of each pair, and laterally external of individual of the trenches of each pair. Conductive data lines are formed in electrical connection with the source/drain regions received laterally external of individual of the trenches of each pair. A charge storage device is formed in electrical connection with respective of the source/drain regions received intermediate individual of the trenches of each pair. By way of example only, such is depicted with reference to the embodiments of Fig. 2 and Figs. 4-6.

The above-described exemplary Figs. 2, Figs. 4-6 and Fig. 7 embodiments might be manufactured by any of a number of existing or yet-to-be developed techniques. Further by way of example only, the depicted trench openings 29, 31 in Figs. 2, 4-6 and 7 might be manufactured to be sublithographic. For example and by way of example only, trench opening outlines might be fabricated to the minimum capable lithographic feature size in a first hard masking layer. Thereafter, additional suitably thin hardmasking material can be deposited thereover to line the sidewalls and bases of the trenches formed in the first hard masking layer(s). Such could be subjected to an anisotropic spacer-like etch, thereby reducing the open width of the trenches prior to etching trench openings 29 and 31 into substrate material 23, and thereby form the depicted trenches to be sublithographic. Further, the hardmasking blocks between trenches might also be fabricated to be sublithographic in an analogous manner by utilizing anisotropically etched hardmask spacers deposited to a lateral thickness less than that of the then-present minimum photolithographic feature dimension.

Further and regardless, peripheral circuitry gate material might be deposited prior to forming trench openings 29, 31, with trench openings 29, 31 then formed through the peripheral circuitry gate material within array area prior to patterning the peripheral gate material to form field effect transistor gates in peripheral circuitry area. Further by way of example only, the exemplary depicted gate dielectric 32 and gate material(s) 28, 30 might be deposited and planarized back relative to the peripheral conductive gate material within the array prior to removing peripheral gate material from the array. Further and by way of example only, the exemplary depicted recessing of conductive gate material 28, 30 within the memory array might occur commensurate with the etching of peripheral gate material. Further, by way of example only, insulative material 70 formed over conductive gate material 28, 30 might be formed commensurate with the fabrication of, and of the same material as, insulative spacers formed with respect to peripheral gate constructions. Any other existing or yet-to-be developed processing is, of course, contemplated with respect to fabricating any of the structures identified and claimed herein, as well as in connection with methods of fabricating a memory array as claimed and described herein.

Claims:

1. A method of fabricating a memory array, comprising:

forming alternating lines of active area regions and trench isolation regions within semiconductive material;

etching a series of racetrack-shaped trenches into the active area regions and the trench isolation regions generally orthogonal to the alternating lines of active area regions and trench isolation regions;

forming conductive material within the racetrack-shaped trenches to form a pair of electrically connected word lines in each of the racetrack-shaped trenches;

forming source/drain regions within the active area regions laterally internal of the racetrack-shaped trenches and laterally external of the racetrack-shaped trenches;

forming conductive data lines in electrical connection with the source/drain regions formed laterally external of the racetrack-shaped trenches; and

forming charge storage devices in electrical connection with the source/drain regions formed laterally internal of the racetrack-shaped trenches.

2. A method of fabricating a memory array, comprising:

forming alternating lines of active area regions and trench isolation regions within semiconductive material;

etching a series of pairs of trenches into the active area regions and the trench isolation regions generally orthogonal to the alternating lines of active area regions and trench isolation regions;

etching interconnecting trenches into the semiconductive material, each of the interconnecting trenches interconnecting individual of the trenches of each pair of trenches;

forming conductive material within the pairs of trenches and the interconnecting trenches to form a pair of electrically connected word lines in each of the pairs of trenches;

forming source/drain regions within the active area regions intermediate individual ones of the trenches of each pair of trenches and laterally external of individual ones of the trenches of each pair of trenches;

forming conductive data lines in electrical connection with the source/drain regions formed laterally external of individual ones of the trenches of each pair of trenches; and

forming charge storage devices in electrical connection with the source/drain regions formed intermediate individual ones of the trenches of each pair of trenches.

3. The method of claim 2 wherein etching the series of pairs of trenches and etching the interconnecting trenches comprises a common masking step.

4. The method of claim 2 wherein etching the series of pairs of trenches and etching the interconnecting trenches comprises a common etching step.

5. . . The method of claim 2 wherein forming the conductive material comprises depositing at least some conductive material within the pairs of trenches and the interconnecting trenches at the same time.

6. The method of claim 2 wherein etching the interconnecting trenches comprises etching only one interconnecting trench for each pair of trenches.

7. The method of claim 2 wherein etching the interconnecting trenches comprises etching only two interconnecting trenches for each pair of trenches.

8. The method of claim 2 wherein etching the interconnecting trenches comprises etching multiple interconnecting trenches for each pair of trenches.

9. A method of fabricating a memory array, comprising: forming alternating lines of active area regions and trench isolation regions within semiconductive material;

etching a series of pairs of trenches into the active area regions and the trench isolation regions generally orthogonal to the alternating lines of active area regions and trench isolation regions;

forming conductive material within the pairs of trenches to form a pair of word lines in each of the pairs of trenches;

forming source/drain regions within the active area regions intermediate individual ones of the trenches of each pair of trenches and laterally external of individual ones of the trenches of each pair of trenches;

forming conductive data lines in electrical connection with the source/drain regions formed laterally external of individual ones of the trenches of each pair of trenches; and

forming charge storage devices in electrical connection with the source/drain regions formed intermediate individual ones of the trenches of each pair, wherein individual memory cells of the memory array each comprise a respective one of the source/drain regions formed intermediate the respective pair of trenches within which the respective pair of word lines is formed, a respective two of the source/drain regions formed laterally external of the respective pair of trenches within which the respective pair of word lines is formed, and the charge storage device that is in electrical connection with the respective source/drain region formed intermediate the respective pair of trenches within which the respective pair of word lines is formed.

10. The method of claim 9 comprising:

etching interconnecting trenches into the semiconductive material, wherein each of the interconnecting trenches interconnects individual ones of the trenches of each respective pair of trenches; and

forming conductor material within the interconnecting trenches to electrically connect respective individual word lines within each respective pair of word lines.

11. The method of claim 9 comprising depositing peripheral circuitry gate material within memory array area and within peripheral circuitry area prior to the etching of the series of pairs of trenches, the etching of the series of pairs of trenches being conducted through the peripheral circuitry gate material that is within the memory array area prior to patterning the peripheral circuitry gate material to form transistor gates in the peripheral circuitry area.

12. The method of claim 9 wherein the forming of the conductive data lines comprises:

forming an interlevel dielectic and contact openings therethrough to the source/drain regions formed laterally external of individual ones of the trenches of each pair of trenches; and

depositing a conductor material within the contact openings and forming the conductive data lines from the conductor material.

13. The method of claim 12 wherein the forming of the conductive data lines from the conductor material comprises subtractive patterning and etch of the conductor material.

14. The method of claim 12 comprising depositing an insulative material over the conductor material prior to the forming of the conductive data lines from the conductor material.

15. The method of claim 12 comprising depositing an insulative material in physical touching contact with the conductor material after the forming of the conductive data lines from the conductor material.

16. The method of claim 12 wherein the forming of the conductive data lines from the conductor material comprises etching of the conductor material to recess the conductor material within the contact openings.

17. The method of claim 16 comprising forming insulative material within the contact openings over recessed conductor material.