



(51) International Patent Classification:
H01L 27/105 (2006.01) *H01L 21/8247* (2006.01)

(21) International Application Number:
PCT/US2011/000152

(22) International Filing Date:
27 January 2011 (27.01.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/701,885 8 February 2010 (08.02.2010) US

(71) Applicant (for all designated States except US): **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83716-9632 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SANDHU, Gurtej, S.** [US/US]; 2964 E Parkriver Drive, Boise, ID 83706 (US). **SMYTHE III, John, A.** [US/US]; 4546 S Riva Ridge Way, Boise, ID 83709 (US).

(74) Agents: **KERN, Jacob, T.** et al.; Brooks, Cameron & Huebsch, PLLC, 1221 Nicollet Avenue, Suite 500, Minneapolis, MN 55403 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(88) Date of publication of the international search report:
17 November 2011

(54) Title: RESISTIVE MEMORY AND METHODS OF PROCESSING RESISTIVE MEMORY

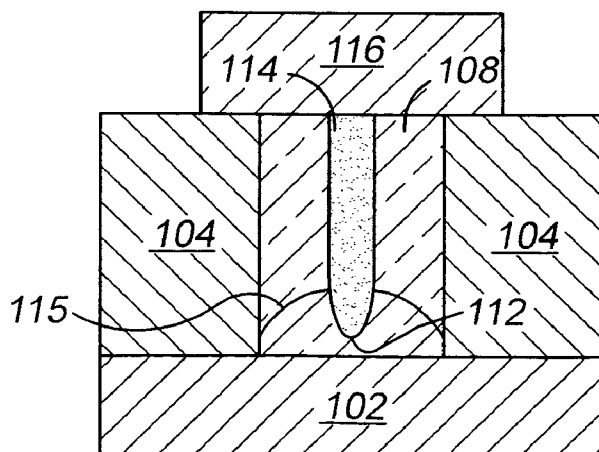


Fig. 1G

(57) Abstract: Resistive memory and methods of processing resistive memory are described herein. One or more method embodiments of processing resistive memory include conformally forming a cell material in an opening in an interlayer dielectric such that a seam is formed in the cell material, forming a conductive pathway by modifying the seam, and forming an electrode on the cell material and the seam.