Description

The present invention relates to a semiconductor device and a method of manufacturing the same, particularly, to a method of connecting multi-layered wiring layers.

In a semiconductor device using multi-wiring layers, connection of wiring layers is performed in general by making contact holes in an interlayer insulation layer. Figs. 3A and 3B collectively show an example of the conventional contact structure of a MOS type semiconductor device for connecting a first wiring layer formed of polycrystalline silicon, said first wiring layer providing a gate electrode, to a second wiring layer formed of a metal.

As seen from Fig. 3A, which is a cross sectional view along the channel region of the MOS transistor, a field oxide layer 2 is selectively formed on the surface of a p-type silicon substrate 1 such that the element region of the MOS transistor is surrounded by the field oxide layer 2. As seen from Fig. 3B, which is a plan view, N^+-type source and drain regions 3 and 4 are formed apart from each other within the element region with the channel region positioned therebetween. A gate electrode 6 formed of polycrystalline silicon is formed above the channel region with a gate oxide layer 5 interposed therebetween. The gate electrode 6 extends to cover partly the field oxide layer 2 and is covered with an interlayer insulation layer 7 formed of silicon dioxide by CVD. Further, an aluminum wiring layer is formed on the interlayer insulation layer 7. A contact hole 8 is formed in the interlayer insulation layer 7 for bringing the aluminum wiring layer into contact with the gate electrode 6. A reactive ion etching (RIE) is employed for forming the contact hole 8 in accordance with miniaturization of the element. In this case, it is necessary to provide an allowance A in the contact portion of the gate electrode 6 as shown in Fig. 3B in view of the deviation in the mask alignment in the step of PEP (photoetching process) for forming the contact hole. Naturally, the allowance A inhibits miniaturization of the semiconductor device.

Where the allowance A is not provided, it is possible for the contact hole 8 to extend beyond the gate electrode 6 because of the deviation in the mask alignment, as shown in Fig. 4. In this case, the field oxide layer 2 is also etched in the step of RIE, with the result that an aluminum wiring 11 is brought into electric contact with the silicon substrate 1. In other words, short-circuiting takes place.

EP-A-0 176 010 describes a procedure for improving the continuity of wiring layers when misalignment and overetching occurs therebetween as well as for limiting the contact width of a wiring layer at contact locations to an underlying wiring layer. Due to masking misalignment a part of the insulating layer adjacent to a wiring layer may be etched. An additional insulating layer is deposited over the contact location and anisotropically etched leaving a narrowed exposed contact area.

The Article in IBM Technical Disclosure Bulletin, Vol. 25, No. 9, February 1983, pages 4768 - 4772 entitled "Method to Realise Submicrometer-wide Images" by C.G. Jambotkar, an insulating layer is deposited in a recess in a semiconductor substrate. Using anisotropic etching, the semiconductor substrate is exposed at the base of the recess leaving insulating layers on the side walls.

An object of the present invention is to provide a semiconductor device having multi-wiring layers formed on a semiconductor substrate, which permits miniaturizing the device and, thus, improving the degree of integration without bringing about short-circuiting between the wiring layers and the semiconductor substrate.

According to the present invention, there is provided a semiconductor device according to Claim 1 and a method of manufacturing a semiconductor device according to Claim 5.

An allowance is certainly provided in the step of forming the contact hole in view of the deviation in the mask alignment. In the present invention, however, it is possible to minimize the allowance, leading to a miniaturization and an improved degree of integration of the device. To be more specific, deviation of the contact hole may possibly cause the field oxide layer to be etched to form a small groove in the field oxide layer such that the groove extends to reach the substrate. In the present invention, however, the groove, even if formed, is filled with the third insulation layer. It follows that a second wiring layer filling the contact hole is prevented from contacting the substrate, even if the contact hole is positioned beyond the edge of the first wiring layer. The particular construction permits minimizing the allowance of the contact hole, leading to miniaturization and improved integration degree of the semiconductor device.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A to 1C are cross sectional views collectively showing the process of manufacturing a semiconductor device according to one embodiment of the present invention;

Fig. 2 is a plan view showing the gist portion of the device shown in Fig. 1;

Fig. 3A is a cross sectional view showing a semiconductor device produced by a conventional method;

Fig. 3B is a plan view showing a semiconductor device produced by a conventional method; and

Fig. 4 is a cross sectional view showing a defect accompanying a semiconductor device produced by a conventional method.

A semiconductor device according to one em-

bodiment of the present invention is manufactured as shown in Figs. 1A to 1C. The device shown in these drawings corresponds to the conventional device shown in Fig. 3 and, thus, the reference numerals common with these drawings denote the same members of the device.

As shown in Fig. 1A, a field oxide layer 2 is formed on a P-type silicon substrate 1. Then, an N^+-type source region 3, an N^+-type drain region 4, and a gate oxide layer 5 are formed as shown in Fig. 2, which is a plan view, followed by forming a gate electrode 6 formed of polycrystalline silicon layer doped with an impurity. Further, an interlayer insulation layer 7 is deposited on the gate electrode 6, followed by forming a contact hole 8 in the insulation layer 7 by an anisotropic etching using a resist pattern. In forming the contact hole 8, an allowance A2 in the width of the contact portion with the gate electrode 6 is set small for miniaturizing the semiconductor device. Thus, if a deviation takes place in the mask alignment, the field insulation layer 2 is also etched near the periphery of the gate electrode 6 so as to form a groove 9 extending downward to reach the substrate 1.

In the next step, an insulation layer 10, e.g., a silicon nitride layer or a silicon dioxide layer, is deposited on the entire surface by means of low pressure CVD, as shown in Fig. 1B. If the thickness of the insulation layer 10 is at least half the width of the groove 9, the groove 9 is completely filled with the insulation layer 10. The insulation layer 10 is then removed by an isotropic etching, as shown in Fig. 1C. If the depth of the groove 9 is markedly larger than the width thereof, the insulation layer 10 is left unremoved selectively within the groove 9 in this etching step. Finally, an aluminum layer is formed on the entire surface, followed by patterning the aluminum layer so as to form an aluminum wiring 11.

In the embodiment described above, the groove 9 is filled with the insulation layer 10, e.g., a silicon nitride layer, with the result that the short-circuit between the aluminum wiring 11 and the silicon substrate 1 can be prevented. In addition, the allowance A2 in the contact portion of the gate wiring 6 can be diminished, leading to miniaturization and high integration degree of the semiconductor device.

The technical idea of the present invention can be applied not only to the semiconductor device described above but also to any type of devices requiring miniaturization and also requiring a measure for preventing short-circuit between the conductor within the contact hole and the semiconductor substrate.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device, comprising:

a semiconductor substrate (1);

a first insulating layer (2) formed on the substrate (1);

a first wiring layer (6) formed on the first insulating layer (2);

a second insulating layer (7) formed on the first wiring layer (6) and having a contact hole (8) the bottom of which is defined by the first wiring layer (6);

a second wiring layer (11) filling the contact hole (8) and connected to the first wiring layer (6) via the contact hole (8);

characterized by

an edge of the contact hole (8) being located at a distance beyond an edge of said first wiring layer (6) due to mask misalignment;

an insulating material (10), filling that hole portion (9) formed due to said mask misalignment directly under the bottom of the contact hole (8) and adjacent to the first wiring layer (6), the hole portion (9) passing through the first insulating layer (2) and reaching the substrate (1), for preventing the first and second wiring layers (6, 11) from contacting the substrate (1), wherein the insulating material (10) only extends from the substrate (1) to the bottom of the contact hole (8).

2. The semiconductor device according to claim 1, characterised in that the first insulating layer (2) is a field oxide layer interposed between the substrate (1) and the second insulation layer (7).

3. The semiconductor device according to claim 1, characterized in that the substrate (1) is of P-type.

4. The semiconductor device according to claim 1, characterized in that the insulating material (10) is silicon nitride.

5. A method of manufacturing a semiconductor device, comprising

a first step of forming a first insulation layer (2) on a substrate (1);

a second step of forming a first wiring layer (6) on the first insulation layer (2);

a third step of forming a second insulation layer (7) on the first wiring layer (6);

a fourth step of forming a contact hole (8) in the second insulation layer (7) above the first wiring layer (6) ;

a fifth step of forming a third insulation layer (10) on the entire surface of the substrate (1) including the contact hole (8);

a sixth step of selectively removing the third insulation layer (10) by isotropic etching to leave a portion of the third insulation layer in any hole portion (9) formed due to mask misalignment

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bodiment of the present invention is manufactured as shown in Figs. 1A to 1C. The device shown in these drawings corresponds to the conventional device shown in Fig. 3 and, thus, the reference numerals common with these drawings denote the same members of the device.

As shown in Fig. 1A, a field oxide layer 2 is formed on a P-type silicon substrate 1. Then, an N^+-type source region 3, an N^+-type drain region 4, and a gate oxide layer 5 are formed as shown in Fig. 2, which is a plan view, followed by forming a gate electrode 6 formed of polycrystalline silicon layer doped with an impurity. Further, an interlayer insulation layer 7 is deposited on the gate electrode 6, followed by forming a contact hole 8 in the insulation layer 7 by an anisotropic etching using a resist pattern. In forming the contact hole 8, an allowance A2 in the width of the contact portion with the gate electrode 6 is set small for miniaturizing the semiconductor device. Thus, if a deviation takes place in the mask alignment, the field insulation layer 2 is also etched near the periphery of the gate electrode 6 so as to form a groove 9 extending downward to reach the substrate 1.

In the next step, an insulation layer 10, e.g., a silicon nitride layer or a silicon dioxide layer, is deposited on the entire surface by means of low pressure CVD, as shown in Fig. 1B. If the thickness of the insulation layer 10 is at least half the width of the groove 9, the groove 9 is completely filled with the insulation layer 10. The insulation layer 10 is then removed by an isotropic etching, as shown in Fig. 1C. If the depth of the groove 9 is markedly larger than the width thereof, the insulation layer 10 is left unremoved selectively within the groove 9 in this etching step. Finally, an aluminum layer is formed on the entire surface, followed by patterning the aluminum layer so as to form an aluminum wiring 11.

In the embodiment described above, the groove 9 is filled with the insulation layer 10, e.g., a silicon nitride layer, with the result that the short-circuit between the aluminum wiring 11 and the silicon substrate 1 can be prevented. In addition, the allowance A2 in the contact portion of the gate wiring 6 can be diminished, leading to miniaturization and high integration degree of the semiconductor device.

The technical idea of the present invention can be applied not only to the semiconductor device described above but also to any type of devices requiring miniaturization and also requiring a measure for preventing short-circuit between the conductor within the contact hole and the semiconductor substrate.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device, comprising:

a semiconductor substrate (1);

a first insulating layer (2) formed on the substrate (1);

a first wiring layer (6) formed on the first insulating layer (2);

a second insulating layer (7) formed on the first wiring layer (6) and having a contact hole (8) the bottom of which is defined by the first wiring layer (6);

a second wiring layer (11) filling the contact hole (8) and connected to the first wiring layer (6) via the contact hole (8);

characterized by

an edge of the contact hole (8) being located at a distance beyond an edge of said first wiring layer (6) due to mask misalignment;

an insulating material (10), filling that hole portion (9) formed due to said mask misalignment directly under the bottom of the contact hole (8) and adjacent to the first wiring layer (6), the hole portion (9) passing through the first insulating layer (2) and reaching the substrate (1), for preventing the first and second wiring layers (6, 11) from contacting the substrate (1), wherein the insulating material (10) only extends from the substrate (1) to the bottom of the contact hole (8).

2. The semiconductor device according to claim 1, characterised in that the first insulating layer (2) is a field oxide layer interposed between the substrate (1) and the second insulation layer (7).

3. The semiconductor device according to claim 1, characterized in that the substrate (1) is of P-type.

4. The semiconductor device according to claim 1, characterized in that the insulating material (10) is silicon nitride.

5. A method of manufacturing a semiconductor device, comprising

a first step of forming a first insulation layer (2) on a substrate (1);

a second step of forming a first wiring layer (6) on the first insulation layer (2);

a third step of forming a second insulation layer (7) on the first wiring layer (6);

a fourth step of forming a contact hole (8) in the second insulation layer (7) above the first wiring layer (6) ;

a fifth step of forming a third insulation layer (10) on the entire surface of the substrate (1) including the contact hole (8);

a sixth step of selectively removing the third insulation layer (10) by isotropic etching to leave a portion of the third insulation layer in any hole portion (9) formed due to mask misalignment

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in the first insulation layer (2) adjacent to the first wiring layer (6) and extending to said semiconductor substrate (1); and

a seventh step of forming a second wiring layer (11) to fill said contact hole (8), said portion of the third insulation layer (10) preventing the second wiring layer (11) from contacting the semiconductor substrate (1).

6. The method according to claim 5, wherein the first insulation layer (2) is a field oxide layer interposed between the substrate (1) and the second insulation layer (7).

7. The method according to claim 5, wherein the substrate (1) is of P-type.

8. The method according to claim 5, wherein the first wiring layer (6) is formed by anisotropic etching using a resist pattern.

9. The method according to claim 5, wherein the contact hole (8) is formed by anisotropic etching using a resist pattern.

10. The method according to claim 5, wherein the third insulation layer (10) is a silicon nitride layer formed by low pressure CVD.

11. The method according to claim 5, wherein the third insulation layer (10) has a thickness not smaller than half the width of any said hole portion (9).

Patentansprüche

1. Halbleitervorrichtung mit:
einem Halbleitersubstrat (1);
einer ersten Isolierschicht (2), die auf dem Substrat (1) vorgesehen ist;
einer ersten Verdrahtungsschicht (6), die auf der ersten Isolierschicht (2) vorgesehen ist;
einer zweiten Isolierschicht (7), die auf der ersten Verdrahtungsschicht (6) vorgesehen ist und ein Kontaktloch (8) aufweist, dessen Boden durch die erste Verdrahtungsschicht (6) bestimmt wird; und einer zweiten Verdrahtungsschicht (11), welche das Kontaktloch (8) ausfüllt und mit der ersten Verdrahtungsschicht (6) über das Kontaktloch (8) verbunden ist;
dadurch **gekennzeichnet**, daß
eine Kante des Kontaktloches (8) in einer Entfernung jenseits einer Kante der ersten Verdrahtungsschicht (6) infolge einer Masken-Fehlausrichtung angeordnet ist;
ein Isoliermaterial (10) vorgesehen ist, welches den Lochabschnitt (9) ausfüllt, der infolge der Masken-Fehlausrichtung direkt unter dem Boden des Kontaktloches (8) und neben der ersten Verdrahtungsschicht (6) angeordnet ist, wobei der Lochabschnitt (9) durch die erste Isolierschicht (2) ragt und das Substrat (1) erreicht, um zu verhindern, daß die erste und zweite Verdrahtungsschicht (6, 11) in Kontakt mit dem Substrat (1) gelangen, wobei sich das Isoliermaterial (10) nur von dem Substrat (1) bis zum Boden des Kontaktloches (8) erstreckt.

2. Halbleitervorrichtung nach Anspruch 1, dadurch **gekennzeichnet**, daß die erste Isolierschicht (2) eine Feldoxidschicht ist, die zwischen dem Substrat (1) und der zweiten Isolierschicht (7) angeordnet ist.

3. Halbleitervorrichtung nach Anspruch 1, dadurch **gekennzeichnet**, daß das Substrat (1) vom P-Typ ist.

4. Halbleitervorrichtung nach Anspruch 1, dadurch **gekennzeichnet**, daß das Isoliermaterial Siliziumnitrid ist.

5. Verfahren zur Herstellung einer Halbleitervorrichtung, mit folgenden Schritten:
einem ersten Schritt zur Ausbildung einer ersten Isolierschicht (2) auf einem Substrat (1);
einem zweiten Schritt zur Ausbildung einer ersten Verdrahtungsschicht (6) auf der ersten Isolierschicht (2);
einem dritten Schritt zur Ausbildung einer zweiten Isolierschicht (7) auf der ersten Verdrahtungsschicht (6);
einem vierten Schritt zur Ausbildung eines Kontaktloches (8) in der zweiten Isolierschicht (7) oberhalb der ersten Verdrahtungsschicht (6);
einem fünften Schritt zur Ausbildung einer dritten Isolierschicht (10) auf der gesamten Oberfläche des Substrats (1) einschließlich des Kontaktloches (8);
einem sechsten Schritt zum selektiven Entfernen der dritten Isolierschicht (10) durch isotropes Ätzen, so daß ein Abschnitt der dritten Isolierschicht in jedem Lochabschnitt (9) verbleibt, der infolge einer Masken-Fehlausrichtung in der ersten Isolierschicht (2) neben der ersten Verdrahtungsschicht (6) ausgebildet wird und sich bis zum Halbleitersubstrat (1) erstreckt; und
einem siebten Schritt zur Ausbildung einer zweiten Verdrahtungsschicht (11) zum Füllen des Kontaktloches (8), wobei der Abschnitt der dritten Isolierschicht (10) verhindert, daß die zweite Verdrahtungsschicht (11) in Kontakt mit dem Halbleitersubstrat (1) gelangt.

6. Verfahren nach Anspruch 5,

bei welchem die erste Isolierschicht (2) eine Feldoxidschicht ist, die zwischen dem Substrat (1) und der zweiten Isolierschicht (7) angeordnet ist.

7. Verfahren nach Anspruch 5, bei welchem das Substrat (1) vom P-Typ ist.

8. Verfahren nach Anspruch 5, bei welchem die erste Verdrahtungsschicht (6) durch anisotropes Ätzen unter Verwendung eines Photolackmusters gebildet wird.

9. Verfahren nach Anspruch 5, bei welchem das Kontaktloch (8) durch anisotropes Ätzen unter Verwendung eines Photolackmusters gebildet wird.

10. Verfahren nach Anspruch 5, bei welchem die dritte Isolierschicht (10) eine Siliziumnitridschicht ist, die durch Niederdruck-CVD gebildet wird.

11. Verfahren nach Anspruch 5, bei welchem die dritte Isolierschicht (10) eine Dicke aufweist, die nicht geringer ist als die halbe Breite jedes Lochabschnitts (9).

Revendications

1. Dispositif à semi-conducteur comprenant :
un substrat semi-conducteur (1) ;
une première couche d'isolation (2) formée sur le substrat (1) ;
une première couche de câblage (6) formée sur la première couche d'isolation (2) ;
une deuxième couche d'isolation (7) formée sur la première couche de câblage (6) et comportant un trou de contact (8) dont le fond est défini par la première couche de câblage (6) ;
une seconde couche de câblage (11) remplissant le trou de contact (8) et connectée à la première couche de câblage (6) par l'intermédiaire du trou de contact (8) ;
caractérisé par :
le fait qu'un bord du trou de contact (8) est situé à une certaine distance au-delà d'un bord de ladite première couche de câblage (6) en raison d'un défaut d'alignement de masque ;
une matière d'isolation (10) remplissant la partie de trou (9) formée, en raison dudit défaut d'alignement de masque, directement sous le fond du trou de montage (8) et adjacente à la première couche de câblage (6), cette partie de trou (9) passant à travers la première couche d'isolation (2) et atteignant le substrat (1), pour empêcher les première et seconde couches de câblage (6, 11) de contacter le substrat, la matière d'isolation (10) s'étendant seulement depuis le substrat (1) jusqu'au fond du trou de contact (8).

2. Dispositif à dispositif semi-conducteur selon la revendication 1, caractérisé en ce que la première couche d'isolation (2) est une couche d'oxyde épais interposée entre le substrat (1) et la deuxième couche d'isolation (7).

3. Dispositif à dispositif semi-conducteur selon la revendication 1, caractérisé en ce que le substrat (1) est de type P.

4. Dispositif à dispositif semi-conducteur selon la revendication 1 caractérisé en ce que la matière d'isolation (10) est du nitrure de silicium.

5. Procédé de fabrication d'un dispositif à semi-conducteur comprenant :
une première étape de formation d'une première couche d'isolation (2) sur un substrat (1) ;
une deuxième étape de formation d'une première couche de câblage (6) sur la première couche d'isolation (2) ;
une troisième étape de formation d'une deuxième couche d'isolation (7) sur la première couche de câblage (6) ;
une quatrième étape de formation d'un trou de contact (8) dans la deuxième couche d'isolation (7) au-dessus de la première couche de câblage (6) ;
une cinquième étape de formation d'une troisième couche d'isolation (10) sur toute la surface du substrat (1) y compris le trou de contact (8) ;
une sixième étape d'élimination de manière sélective de la troisième couche d'isolation (10), par attaque isotropique, pour laisser une partie de la troisième couche d'isolation dans une certaine partie de trou (9) formée, en raison d'un défaut d'alignement de masque, dans la première couche d'isolation (2) adjacente à la première couche de câblage (6) et s'étendant jusqu'au substrat conducteur (1) ; et
une septième étape de formation d'une seconde couche de câblage (11) pour remplir ledit trou de contact (8), ladite partie de la troisième couche d'isolation (10) empêchant la seconde couche de câblage (11) de contacter le substrat semi-conducteur (1).

6. Procédé selon la revendication selon la revendication 5, dans lequel la première couche d'isolation (2) est une couche d'oxyde épais interposée entre le substrat (1) et la deuxième couche d'isolation (7).

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7. Procédé selon la revendication 5, dans lequel le substrat (1) est de type P.

8. Procédé selon la revendication 5, dans lequel la première couche de câblage (6) est formée par attaque anisotropique en utilisant un motif de résist.

9. Procédé selon la revendication 5, dans lequel le trou de contact (8) est formé par attaque anisotropique en utilisant un motif de résist.

10. Procédé selon la revendication 5, dans lequel la troisième couche d'isolation (10) est une couche de nitrure de silicium formée par CVD (dépôt chimique en phase vapeur) à basse pression.

11. Procédé selon la revendication 5, dans lequel la troisième couche d'isolation (10) a une épaisseur qui n'est pas inférieure à la moitié de la largeur que peut avoir ladite partie de trou (9).