Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a ~~carrier;~~

~~forming a first interconnect structure over the carrier;~~

~~testing the first interconnect structure;~~

~~disposing a semiconductor die over the first interconnect structure after testing the first interconnect structure~~ first interconnect structure by,

(a) providing a first insulating layer, and

(b) forming a first conductive layer over the first insulating layer;

testing the first interconnect structure at a wafer-level;

after testing the first interconnect structure, disposing a semiconductor die over the first interconnect structure at the same wafer-level as the testing of the first interconnect structure;

forming a vertical interconnect structure over the first interconnect structure, the vertical interconnect structure including an inner conductive bump in contact with the first interconnect structure and protective layer disposed over the inner conductive bump;

depositing an encapsulant over the semiconductor die, first interconnect structure, and vertical interconnect structure;

removing a portion of the encapsulant and a portion of the protective layer to expose the inner conductive bump;

forming a second interconnect structure over the encapsulant;~~and~~

~~forming a second interconnect structure over the encapsulant and electrically coupled to the vertical interconnect structure~~ and

removing a portion of the first insulating layer after forming the second interconnect structure.

2. The method of claim 1, further including disposing a discrete semiconductor device over the first interconnect structure or the second interconnect structure.

~~3. The method of claim 1, further including removing a portion of the encapsulant to expose the vertical interconnect structure.~~

~~4~~3. The method of claim 1, wherein the first ~~interconnect structure or second interconnect structure includes an~~ insulating layer ~~with~~ includes an embedded glass cloth, glass cross, filler, or fiber.

4. The method of claim 1, further including testing the second interconnect structure.

5. The method of claim 1, further including forming the second interconnect structure including a second insulating layer comprising an embedded glass cloth, glass cross, filler, or fiber.

6. The method of claim 1, wherein forming the second interconnect structure further includes:

providing a second insulating layer in contact with the encapsulant; and

forming a second conductive layer over the insulating layer.

~~5~~7. A method of making a semiconductor device, comprising:

~~forming a first known good interconnect structure;~~

~~disposing a semiconductor die over the first known good interconnect structure;~~

~~depositing an encapsulant over the semiconductor die and first known good interconnect structure; and~~

~~forming a second interconnect structure over the encapsulant~~providing a first interconnect structure;

testing the first interconnect structure at a wafer-level;

after testing the first interconnect structure, disposing a semiconductor die over the first interconnect structure at the same wafer-level as the testing of the first interconnect structure;

forming a vertical interconnect structure over the first interconnect structure with a protective layer disposed over the vertical interconnect structure;

depositing an encapsulant over the semiconductor die and first interconnect structure;

removing a portion of the encapsulant and a portion of the protective layer to expose the vertical interconnect structure; and

forming a second interconnect structure over the semiconductor die.

~~6. The method of claim 5, further including forming a vertical interconnect structure electrically coupled to the first known good interconnect structure and the second interconnect structure.~~

~~7. The method of claim 5, further including removing a portion of the encapsulant to expose the vertical interconnect structure~~.

~~8~~9. The method of claim ~~5~~7, further including disposing a discrete semiconductor device over the first interconnect structure or the second interconnect structure.

~~9~~10. The method of claim ~~5~~7, wherein the first ~~known good~~ interconnect structure or second interconnect structure includes an insulating layer with an embedded glass cloth, glass cross, filler, or fiber.

~~10. A semiconductor device, comprising:~~

~~a first known good first interconnect structure;~~

~~a semiconductor die disposed over the first known good interconnect structure;~~

~~an encapsulant deposited over the semiconductor die and first known good interconnect structure; and~~

~~a second interconnect structure formed over the encapsulant.~~

~~11. The semiconductor device of claim 10, further including a vertical interconnect structure electrically coupled to the first interconnect structure and second interconnect structure.~~

~~12~~8. The ~~semiconductor device~~ method of claim ~~10~~7, wherein the semiconductor die is a known good die.

~~13. The semiconductor device of claim 10, further including a discrete semiconductor device disposed over the first known good interconnect structure or the second interconnect structure.~~

~~14. The semiconductor device of claim 10, wherein the first known good interconnect structure or the second interconnect structure includes an insulating layer with an embedded glass cloth, glass cross, filler, or fiber.~~

~~15~~11. The ~~semiconductor device~~ method of claim ~~10~~7, wherein the vertical interconnect structure includes a bump or stud bump.

12. The method of claim 7, wherein providing the first interconnect structure further includes:

providing an insulating layer; and

forming a conductive layer over the insulating layer.

13. The method of claim 12, further including removing a portion of the insulating layer after forming the second interconnect structure

14. The method of claim 7, wherein forming the second interconnect structure further includes:

providing an insulating layer in contact with the encapsulant; and

forming a conductive layer over the insulating layer.

15. The method of claim 14, wherein the conductive layer contacts the vertical interconnect structure.

16. A method of making a semiconductor device, comprising:

providing a first interconnect structure testable during interim stages of making the semiconductor device;

forming a vertical interconnect structure over the first interconnect structure with a protective layer disposed over the vertical interconnect structure;

providing a second interconnect structure;

testing the second interconnect structure at a wafer-level;

disposing the first interconnect structure over the second interconnect structure to bring the vertical interconnect structure into contact with the second interconnect structure;

disposing a first semiconductor die over the first interconnect structure or second interconnect structure; and

cutting through the second interconnect structure to singulate the semiconductor device.

17. The method of claim 16, further including disposing a discrete semiconductor device over the first interconnect structure or the second interconnect structure.

18. The method of claim 16, further including testing the first interconnect structure.

19. The method of claim 16, further including disposing a second semiconductor die over the second interconnect structure.

20. The method of claim 16, wherein the vertical interconnect structure includes a bump or stud bump.

21. The method of claim 16, wherein the first interconnect structure or second interconnect structure includes an insulating layer comprising an embedded glass cloth, glass cross, filler, or fiber.

22. The method of claim 16, wherein forming the second interconnect structure further includes:
providing an insulating layer; and
forming a conductive layer over the insulating layer.

23. The method of claim 22, wherein the conductive layer contacts the vertical interconnect structure.

24. A method of making a semiconductor device, comprising:
providing a first interconnect structure;
testing the first interconnect structure at a wafer-level;
after testing the first interconnect structure, disposing a semiconductor die over the first interconnect structure at the

same wafer-level as the testing of the first interconnect structure;

forming a vertical interconnect structure over the first interconnect structure with a protective layer disposed over the vertical interconnect structure;

depositing an encapsulant over the semiconductor die and first interconnect structure; and

removing a portion of the encapsulant and a portion of the protective layer to expose the vertical interconnect structure.

25. The method of claim 24, further including forming a second interconnect structure over the semiconductor die and encapsulant.

26. The method of claim 24, wherein the vertical interconnect structure includes a bump or stud bump.

27. The method of claim 24, wherein the first interconnect structure includes an insulating layer comprising an embedded glass cloth, glass cross, filler, or fiber.

28. The method of claim 24, further including disposing a discrete device over the first interconnect structure.

29. The method of claim 25, wherein providing the second interconnect structure further includes:

providing an insulating layer; and

forming a conductive layer over the insulating layer.

30. The method of claim 29, wherein the conductive layer contacts the vertical interconnect structure.