APPLICATION FOR UNITED STATES

LETTERS PATENT

TITLE: BRIDGELESS SWITCHLESS PCIe EXPANSION

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BRIDGELESS SWITCHLESS PCIe EXPANSION

FIELD OF THE INVENTION

[0001] The present invention relates to expansion of high speed bus data communications over a serial link including PCI Express, commonly referred to as PCIe.

DEFINITIONS

[0002] Peripheral card shall refer to a card that plugs into a data bus. Examples include, but are not limited to: SCSI controller, video cards, sound cards, USB cards, etc.

[0003] An "Expansion unit" shall refer to any device that extends or expands a bus outside of its normal physical environment. An expansion unit is intended for normal use of a peripheral card(s).

[0004] "Extension card" shall refer to a card or short cable that does not expand a bus outside of its environment, but allows for the bus to be more easily accessed for debug while in its environment. It is not intended for normal use. Catalyst (www.getcatalyst.com) makes several extension cards that fall into this category.

[0005] Bridging device (chip) shall refer to a chip which interfaces data signals from one bus to another bus. Examples of a bridge chip include, but are not limited to: 41210 (Intel), PEX8111 (PLX), XIO2000 (TI).

[0006] Switch device (chip) is a logical bridge device. It is the PCIe equivalent of a PCI bridge. Examples of this are the uPD720401(NEC), PEX8508 (PLX), XIO3130 (TI).

BACKGROUND OF INVENTION

[0007] Figure 1 shows at 10 the general concept of expanding or extending a host parallel data bus over a serial link to make the PCI / PCIe bus (PCIe is an derivative of the PCI bus) available on an expansion system. Using this system, the host BIOS / OS will see at least one bridge or switch device 12 in a device manager (or similar program) regardless of whether or not any host expansion slots are populated with peripheral cards. If peripheral cards are present, they will also show up. Under normal conditions, the peripheral card will (should) always be visible to the host system regardless of whether a unit is in the host system, hanging on an extension card, or in an expansion unit. One such technology is the Split Bridge™ expansion technology sold by Mobility Electronics, Inc. of Scottsdale, AZ, the teachings of which are incorporated herein by reference.

[0008] The conventional expansion bridge or switch 12 uses such techniques as clock recovery or external clock generation and alignment to ensure the correct clock-data protocol is maintained. The bridge / switch 12 also handles such things as reset, wake, and other side band signals used to ensure proper peripheral card functioning.

SUMMARY OF INVENTION

[0009] In accordance with a first aspect of the present invention, there is provided a PCI Express (PCIe) communication system comprising: a host receiving bus data and power, configured to serially transmit PCIe compliant signals; a serial link electrically coupled to the host; a receiver electrically coupled to the host a serial link electrically coupled to the link and configured to receive the serially transmitted PCIe signals; a driver electrically coupled to the host and configured to amplify the transmitted PCIe signals, whereby the PCIe signals sent by the host do not meet the PCIe Specification requirements, but which PCIe signals do meet the PCIe Specification at the receiver; and the host including an interface processing a sideband signal such that the side band signal is passed after the power has stabilized.

[0009a] In accordance with a second aspect of the present invention, there is provided a driver adapted to couple to a data bus having power and amplify received PCIe compliant signals, whereby the PCIe compliant signals sent by the driver do not meet the PCIe Specification requirements, which said received signals do meet the PCIe Specification requirements without the driver, and further including an interface processing a sideband signal such that the sideband signal is sent after the power has stabilized.

[0009b] In accordance with a third aspect of the present invention, there is provided a PCI Express (PCIe) communication system comprising: a host receiving bus data and power, configured to serially transmit PCIe compliant signals; a serial link electrically coupled to the host; a receiver electrically coupled to the host a serial link electrically coupled to the link and configured to receive the serially transmitted PCIe signals; a driver electrically coupled to the host and configured to amplify the transmitted PCIe signals, whereby the PCIe signals sent by the host do not meet the PCIe Specification requirements, but which PCIe signals do meet the PCIe Specification at the receiver; and processing means for processing a sideband signal such that the side band signal is passed after the power has stabilized.

[0009c] In accordance with a fourth aspect of the present invention, there is provided a driver adapted to couple to a data bus having power and amplify received PCIe compliant signals, comprising: driver means for sending signals that do not meet the PCIe Specification requirements, which said received signals do meet the PCIe Specification requirements without the driver, and further including an means for processing a sideband signal such that the sideband signal is sent after the power has stabilized.

[0009d] Embodiments of the present invention can achieve technical advantages as a device, system and method adapted to expand a high speed data bus, such as a PCI Express (PCIe) bus, over a serial link with an expansion unit having a high speed data bus, such as a PCIe bus, without using a bridging or switching device. One primary advantage of not using a bridge or switch is that the expansion interface can be completely transparent to the BIOS, processor, CPU, OS, or any other component(s) on the host motherboard be they hardware, firmware, or software. The embodiments may not require additional protocols such as TCP/IP, Serial ATA, Gigabit Ethernet, etc. There may also be no implicit hardware or device driver latency resulting from a bridge or switch.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 depicts a block diagram of a legacy parallel data bus expanded by a serial cable to an expansion system using a prior art bridging or switching device;

[0011] Figure 2 depicts one embodiment of the invention providing serial expansion of a host serial data bus to an expansion system without using a bridging or switching device;

[0012] Figure 3 depicts a data and clock buffer adapted to buffer signals communicated from one end of the serial link to the other end;

[0013] Figure 4 depicts an interface circuit configured to process sideband signals; and

[0014] Figure 5 depicts a waveform diagram of the host expansion slot power and a processed sideband signal according to the invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0015] Figure 2 depicts one embodiment of the invention at 20 comprising a host 22 having a host data bus 24 and an interface 26 that extends the host bus 24 to an expansion system data, data bus 28 of expansion system 30 over a serial data cable 32 using a very transparent method. The interface 26 includes a data and clock buffer that conditions data and clock signals, such as those available from Pericom, Maxim, and National Semiconductor and all sideband interface circuits that control WAKE# and PERST#.

[0016] According to the invention, these buffers 22 strengthen the PCIe clock and/or data signals to levels outside of what is called for in the PCI Express Specification to compensate for cable loss of the signals. Using this interface and method, the BIOS/OS will not see any device in the expansion system until the expansion slot is populated with an add-in card. This is because the buffers 22 do not interact with the signals other than to condition them to levels to compensate for subsequent cable loss. The data being transmitted and received is not changed or delayed, or wrapped in a secondary protocol, such as TCP/IP, by this invention, unlike a bridge or switch. This buffer 22 may be a PI2EQX4 driver manufactured by Pericom Semiconductor Corporation, shown in Figure 3.

[0017] Advantageously, this invention provides sideband signal processing in the interface 26 on either or both of the host and expansion that also processes side band signals, such as PERST# (reset) and WAKE# (system wake up), etc., which side band signals are handled in such a way as to not interfere with the power-on sequence of the peripheral card 22 when the host system is off, or not yet attached.

[0018] Referring to Figure 4, there is shown an electrical schematic diagram of an signal processing module 40 that is integrated in interface 26 and that processes a sideband signal such that the signal is passed on to the expansion interface after power at the expansion interface is stable. In one embodiment, a power-on reset monitor circuit 42 ensures power V_{DD} is stable a finite period of time that meets the PCIe specification, before passing on the sideband signal, such as PERST# or WAKE#. Other signals, such as PRSNT# (peripheral card present), are handled in such a way as to ensure the host system understands how many lanes (connections to) the expansion system it has available, which aids in link training right after power up regardless of the lanes the peripheral card may have available.

[0019] Basically, what can happen in a laptop is as the PCIe slot power in the laptop comes up as shown in Figure 5, (not to be confused with main power but the +3.3V and +1.5V V_{DD} power in the Express slot), the slot power can go up and down/glitch before stabilizing, as shown at 'A'. This glitch causes problems initiating sideband signal, such as PERST#, since the glitch does violate the PCIe specification. The add-in card in the expansion system will usually not behave properly if it even comes out of reset at this point, because the system power (for the host card) was not stable before PERST# was deasserted, shown at point 'D.' This embodiment of the invention incorporates the small reset monitor

chip 42 that ensures Power V_{DD} to be good for some finite determined amount of time that meets the PCIe specification before it passes the sideband signal, such as System PERST#, through. This time is shown at 'B.' The add-in card sees PERST# for time 'C', which time 'C' meets the PCIe specification and ensure that spikes in the power do not lock up or fowl the system.

[0020] Sideband signal WAKE# is handled much easier and in a conventional method, it is passed through. The invention lets WAKE# float and the host system pulls this line high. Since it is active low, it is never asserted. This may seem odd, but as the system powers up, spikes and noise on this line can cause erratic behavior. Furthermore, in using adapter cards that allow PCIe E-cards to be used in Desktop host computers, the desktop PC turns on (from being powered off) when these cards are plugged in. In most cases, this is attributed it to the presence of the WAKE# signal as the inserted card is plugged in, it is detected before it has been able to pull WAKE# after its power on sequence.

[0021] This present invention is superior and unique because it does not require a bridge (or switching device), additional drivers, or any resources to be allocated for this type of high speed serial expansion system. In contrast, any peripheral card drivers / resources required in the case of Figure 1, caching or other bridge / switch attributes will decrease performance because there will always be some latency in distributing the packets through a bridge or switch. The invention is faster for a single slot expansion than a similar system (for a single slot) using a bridge or switch device.

[0022] This invention differs from an extension card in that it offers the ability to use the peripheral card under normal or even better conditions juxtaposed to the ability of an extension card which would usually require

removal of the host system cover and an unorthodox method of securing the peripheral card in place.

[0023] Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

CLAIMS

What is claimed is:

1. A PCI Express (PCIe) communication system comprising:

a host receiving bus data and power, configured to serially transmit PCIe compliant signals;

a serial link electrically coupled to the host;

a receiver electrically coupled to the host a serial link electrically coupled to the link and configured to receive the serially transmitted PCIe signals;

a driver electrically coupled to the host and configured to amplify the transmitted PCIe signals, whereby the PCIe signals sent by the host do not meet the PCIe Specification requirements, but which PCIe signals do meet the PCIe Specification at the receiver; and

the host including an interface processing a sideband signal such that the side band signal is passed after the power has stabilized.

2. The PCIe communication system as specified in Claim 1 wherein the serial link can be, but is not required to be, a PCIe Specification compliant cable.

3. The PCIe communication system as specified in Claim 1 wherein the interface is synchronized with the host power and is adapted to process a PERST# sideband signal.

4. The PCIe communication system as specified in Claim 3 wherein the interface delays the PERST# signal until the power is stable a predetermined time period.

5. A driver adapted to couple to a data bus having power and amplify received PCIe compliant signals, whereby the PCIe compliant signals sent by the driver do not meet the PCIe Specification requirements, which said received signals do meet the PCIe Specification requirements without the driver, and further including an interface processing a sideband signal such that the sideband signal is sent after the power has stabilized.

6. The driver as specified in Claim 5 wherein the driver is configured to deliver the PCIe signals that meet the PCIe Specification at a receiver when sent over the cable which cable may not be compliant with the PCIe Specification.

7. A PCI Express (PCIe) communication system comprising:

a host receiving bus data and power, configured to serially transmit PCIe compliant signals;

a serial link electrically coupled to the host;

a receiver electrically coupled to the host a serial link electrically coupled to the link and configured to receive the serially transmitted PCIe signals;

a driver electrically coupled to the host and configured to amplify the transmitted PCIe signals, whereby the PCIe signals sent by the host do not meet the PCIe Specification requirements, but which PCIe signals do meet the PCIe Specification at the receiver; and

processing means for processing a sideband signal such that the side band signal is passed after the power has stabilized.

8. The PCIe communication system as specified in Claim 7 wherein the serial link can be, but is not required to be, a PCIe Specification compliant cable.

9. The PCIe communication system as specified in Claim 7 wherein the processing means is synchronized with the host power and is adapted to process a PERST# sideband signal.

10. The PCIe communication system as specified in Claim 9 wherein the processing means delays the PERST# signal until the power is stable a predetermined time period.

11. A driver adapted to couple to a data bus having power and amplify received PCIe compliant signals, comprising:

driver means for sending signals that do not meet the PCIe Specification requirements, which said received signals do meet the PCIe Specification requirements without the driver, and further including an means for processing a sideband signal such that the sideband signal is sent after the power has stabilized.

12. The driver as specified in Claim 11 wherein the driver means is configured to deliver the signals that meet the PCIe Specification at a receiver when sent over the cable which said cable may not be compliant with the PCIe Specification.