(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2002 (27.12.2002)

PCT

(10) International Publication Number
WO 02/103518 A1

(51) International Patent Classification[7]: G06F 9/455, 15/00, 15/76

(21) International Application Number: PCT/US02/11870

(22) International Filing Date: 2 May 2002 (02.05.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/288,298 2 May 2001 (02.05.2001) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 60/288,298 (CIP)
Filed on 2 May 2001 (02.05.2001)

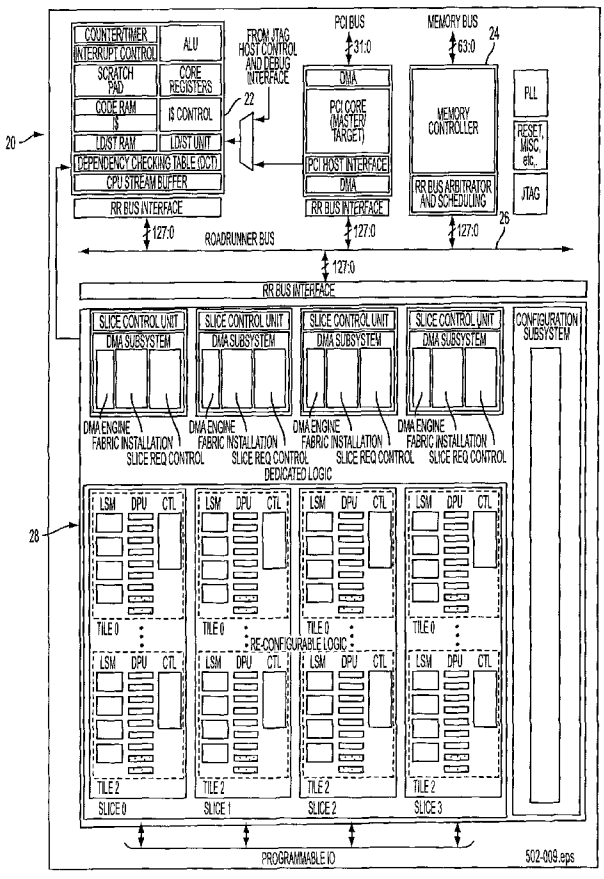
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[Continued on next page]

(54) Title: EFFICIENT HIGH PERFORMANCE DATA OPERATION ELEMENT FOR USE IN A RECONFIGURABLE LOGIC ENVIRONMENT



(57) Abstract: A reconfigurable chip (20) is taught having reconfigurable functional units including a shift register, arithmetic logic, and multiplexers. The data paths are interconnected to other data path units. Interconnection is provided by transferring word length data. The shifter allows for the word length data to be adjusted for use in the arithmetic logic unit. Reconfigurable functional units are controlled by reconfigurable functional unit instructions. The reconfigurable unit instructions are stored in a reconfigurable functional unit instruction memory, which is addressed by a state machine on the chip.

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

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