

ABSTRACT

5 SEMICONDUCTOR MEMORY HAVING STAGGERED SENSE AMPLIFIERS
 ASSOCIATED WITH A LOCAL COLUMN DECODER

10 The invention relates to a semiconductor memory, comprising:
 – bit lines,
 – a memory cell array and,
 – at least one pair of sense amplifier banks, wherein each sense amplifier is
 connected to a corresponding bit line according to an interleaved arrangement
15 resulting in interconnect spaces available in each sense amplifier bank of the pair
 parallel to the bit lines,
 characterized in that each sense amplifier bank further comprises at least one local
 column decoder for selecting at least one sense amplifier of the sense amplifier
 bank, the local column decoder being coupled to the at least one sense amplifier of
20 the sense amplifier bank by means of an output line running in an available
 interconnect space parallel to the bit lines.

FIGURE 3