Claims

What is claimed:

1. A semiconductor device, comprising:

a first semiconductor die including a plurality of bumps formed ~~over~~on a surface of the first semiconductor die;

a penetrable adhesive layer disposed ~~over~~ directly on the surface of the first semiconductor die with the bumps ~~at least partially disposed in~~ completely embedded within the penetrable adhesive layer to displace the penetrable adhesive layer;

an encapsulant deposited over the first semiconductor die; and

an interconnect structure formed over the first semiconductor die and electrically connected to the bumps.

2. The semiconductor device of claim 1, wherein the bumps completely embedded within the penetrable adhesive layer ~~are at least partially disposed in the penetrable adhesive layer~~ reduce shifting of the first semiconductor die.

3. The semiconductor device of claim 1, wherein the interconnect structure includes:

a conductive layer; and

an insulating layer formed around the conductive layer.

~~4. The semiconductor device of claim 1, further including a gap between the surface of the first semiconductor die and the penetrable adhesive layer.~~

~~5~~4. The semiconductor device of claim 1, further including a plurality of electrically isolated bumps formed over the surface of the first semiconductor die.

~~6~~5. The semiconductor device of claim 1, further including a second semiconductor die or component disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die.

~~7~~6. A semiconductor device, comprising:

a first semiconductor die including a ~~plurality of~~ first bump~~s~~ formed over a surface of the first semiconductor die;

an adhesive layer disposed over the first semiconductor die with the first bump~~s~~ embedded within ~~disposed in~~ the adhesive layer to displace the adhesive layer; and

an encapsulant deposited over the first semiconductor die.

~~8~~7. The semiconductor device of claim ~~7~~6, wherein the first bump~~s~~ embedded within ~~disposed in~~ the adhesive layer reduces shifting of the first semiconductor die.

~~9~~8. The semiconductor device of claim ~~7~~6, further including an interconnect structure formed over the first semiconductor die and electrically connected to the first bump~~s~~.

~~10~~9. The semiconductor device of claim ~~7~~6, further including a second bump disposed over the semiconductor die, the second bump ~~having~~including a cross-sectional area larger than the first bump~~s~~.

1~~1~~0. The semiconductor device of claim ~~7~~6, further including a plurality of openings formed in the adhesive layer.

1~~2~~1. The semiconductor device of claim ~~7~~8, further including:

a thermally conductive via formed in the interconnect structure; and

a heat sink disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die and connected to the thermally conductive via.

1~~3~~2. The semiconductor device of claim ~~7~~8, further including a second semiconductor die or component disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die.

1~~4~~3. A semiconductor device, comprising:

a first semiconductor die including first bumps formed on a surface of the semiconductor die;

an adhesive layer disposed over the first semiconductor die to embed the bumps; and

an encapsulant deposited over the first semiconductor die.

1~~5~~4. The semiconductor device of claim 1~~4~~3, further including a plurality of second bumps formed over ~~a~~the surface of the first semiconductor die and at least partially embedded in the adhesive layer to reduce shifting of the first semiconductor die.

1~~6~~5. The semiconductor device of claim 1~~4~~3, further including an interconnect structure formed over the first semiconductor die.

1~~7~~6. The semiconductor device of claim 1~~4~~3, further including a plurality of openings formed in the adhesive layer.

1~~8~~7. The semiconductor device of claim 1~~4~~5, further including a thermally conductive via formed in the interconnect structure.

198. The semiconductor device of claim 145, further including a heat sink disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die.

~~20~~19. The semiconductor device of claim 145, further including a second semiconductor die or component disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die.

210. A semiconductor device, comprising:

a first semiconductor die including ~~a plurality of~~ bumps formed over a surface of the first semiconductor die;

an adhesive layer disposed over the surface of the first semiconductor die with the bumps at least partially embedded into the adhesive layer to reduce shifting of the first semiconductor die; and

an encapsulant deposited over the first semiconductor die.

221. The semiconductor device of claim 210, further including an interconnect structure formed over the first semiconductor die and electrically connected to the bumps.

232. The semiconductor device of claim 21, further including a thermally conductive via formed in the interconnect structure.

243. The semiconductor device of claim 21, further including a heat sink disposed over ~~mounted to~~ a surface of the interconnect structure opposite the first semiconductor die.

254. The semiconductor device of claim 21, further including a second semiconductor die or component disposed over ~~mounted to~~ a

surface of the interconnect structure opposite the first semiconductor die.