

A B S T R A C T

A memory cell array having memory cell which are arranged and which is capable of holding N-bit data; and a sense amplifier having a first latch (SEN) capable of
5 holding information on a threshold distribution, a second latch (SDL) holding write data, and a third latch (LDL) capable of lower information of the 2-bit data, and a sense amplifier supplying a first to a fourth voltages to the memory cell to write the data to the memory cell using the
10 first to fourth voltages are comprised, wherein the sense amplifier supplies the first to third voltages (VSS, VDD and VQPWL) to the memory cell based on information held by the second latch and the third latch, and then, based on a result of transfer of the information held by the first
15 latch to the second latch, supplies the fourth voltage(VQPWH) or the first voltage (VSS) to the memory cell.