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(19)

(54) SYSTEM FOR ELIMINATING SUBSTRATE BIAS EFFECT IN FIELD EFFECT TRANSISTOR CIRCUITS

(71) We RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention is directed to monolithic field effect integrated circuits operated with two or more power supplies.

It is often necessary and/or desirable to operate different parts of an electronic system at different voltage levels. At the places where the different parts are to be electrically coupled, the signals at the interfaces are not necessarily compatible. It is, therefore, necessary to provide some means, e.g., interface and level shift circuits, which can render one part of the system compatible with the other. The design of interface circuits, however, is made more difficult when the active devices of the electronics system are formed on a single monolithic substrate.

Circuits embodying the invention are formed on a common substrate and a different well region is provided for each different operating potential applied to the circuit. Transistors having their source electrodes connected to a given potential are formed in a well or in the common substrate having the same given potential applied thereto. Circuits can thereby be formed in which all the active components have zero reverse bias between their source and substrate .

In the accompanying drawings like reference numerals denote like components; and

FIGURE 1 is a schematic diagram of a prior art circuit known to the Applicants;

FIGURE 2 is a schematic diagram of a circuit embodying the invention; and

FIGURE 3 is a cross section of a portion of the circuit of FIGURE 2.

Some of the difficulties mentioned previously may be seen by referring to the circuit of FIGURE 1 which shows an integrated complementary metal oxide semiconductor (CMOS) circuit. FIGURE 1 illustrates that transistors in an interface circuit may be subjected to a considerable reverse bias between their source electrodes and their substrates, giving rise to serious problems.

In FIGURE 1 the output of a first logic circuit 120 operated from a 3 volt power supply is coupled by means of a circuit comprised of inverters 11, 12 and 13 to a second logic circuit 140 operated from a 15 volt power supply. The operating potential for inverter 11 is the same 3 volt source as for circuit 120. Inverter 11 inverts the output from circuit 120 and applies it to the input of inverter 12 (gate of transistor N2). The operating potential for inverters 12 and 13 is the same 15 volt source as for circuit 140. Inverters 12 and 13 are cross-coupled and supply a signal varying between ground and 15 volts to circuit 140 in response to the complementary 3 volt level signals applied to their inputs (gates of transistors N2 and N3).

FIGURE 1 shows schematically that all the P-type transistors (P1, P2 and P3) share the same substrate 150 to which is applied the highest system potential (15 volts), and that the substrates of all the N-type transistors (N1, N2 and N3) are returned to the lowest system potential (ground). Note, however, that the source of a transistor may be operated at a different potential than its substrate region. Specifically, transistor P1 has its source connected to 3 volts while its substrate is at 15 volts.

Operating the source electrodes of transistors at one potential while connecting their substrate to a different potential creates

serious problems. The threshold voltage (V_T) of a field effect transistor is defined as the gate to source potential which must be exceeded to turn the transistor on. The V_T is dependent on the potential applied between the source and the substrate of the transistor. A reverse bias applied between the source and the substrate increases the V_T of the transistor. Depending on the resistivity of the substrate material, the V_T may increase above its nominal value at zero source to substrate bias by an amount varying from 0.2 volts per volt of reverse bias to 1 volt per volt of reverse bias.

The V_T of transistor P1 may be, for example 2 volts when the source and the substrate are connected in common (i.e. zero reverse bias). However, with a reverse bias of 12.0 volts applied between the source and the substrate, as in FIGURE 1, the V_T increases to a value which may range from 4 volts to more than 10 volts. Clearly, if the V_T of transistor P1 is 4 volts the gate to source potential necessary to turn it "on" must be equal to or greater than 4 volts. However, transistor P1 is part of a circuit operated from the 3 volt power supply. Also, the signals applied to the gate of transistor P1 are derived from circuits operated from the 3 volt power supply and will also vary from zero volts to a maximum of 3 volts. Accordingly, transistor P1 cannot be turned on and the circuit is thereby rendered partly or wholly inoperative.

The problem of increasing V_T is even more acute in circuits where the transistors are designed to operate at very low voltages such as 1.5 volts or less. Another problem is that even where the V_T of the transistor is not increased beyond the operating range, a reverse bias increases the "on" impedance of the transistor thereby altering the turn on and turn off time of the circuit.

In FIGURE 2, the circuit 12 is connected across a first power supply of V1 volts and produces output signals at terminal 19 which vary between V1 volts and V_{DD} volts. Circuit 12 may be any one of a number of known logic or analog circuits whose output signals are to be coupled to another circuit 14 which may also be a logic or analog circuit or a display device or other type of load device. Circuit 14 is connected across a second power supply of V2 volts and requires input signals of an amplitude varying between V_{DD} volts and V2 volts. By way of example, V_{DD} volts is ground potential, V1 volts is -1.5 volts and V2 volts is -20 volts.

The output of circuit 12 is level shifted by means of inverters 10, 20 and 30 for producing signals suitable to drive circuit 14. Each inverter includes a P-type transistor and an N-type transistor denoted by a P and an N, respectively, with a numerical subscript corresponding to its associated inverter. The gates of transistors P10 and N10 are connected to terminal 19 to which the output of circuit 12 is applied. The substrate 60 and the source of transistor P10 are connected to a terminal 13 to which is applied a potential of $+V_{DD}$ volts. The drain of transistor P10 is connected to the drain of transistor N10 at terminal 14. The source and substrate, 67, of transistor N10 are connected to a terminal 15 to which is applied a potential of V1 volts.

The sources and the substrate, 60, of transistors P20 and P30 are connected to terminal 13. The gates of transistors P20 and P30 are connected to terminals 14 and 19, respectively. The drains of transistors P20 and N20 are connected to the gate of the transistor N30 at output terminal 16 and the drains of transistors P30 and N30 are connected to the gate of transistor N20 at output terminal 18. The sources and the substrate, 70, of transistors N20 and N30 are connected to terminal 17 to which is applied a potential of V2 volts. Output terminal 18 is connected to circuit 14. Obviously output 16 could, similarly to terminal 18, be used to drive an output circuit.

The circuit of FIGURE 2 may be formed as shown, in part, in FIGURE 3. The common substrate, 60, is a body of semiconductor of N-conductivity type material in which are diffused regions (61, 62, 63, 64, 67 and 70) of P-conductivity type. P-regions 61 and 62 form the source and drain regions of P-conductivity type transistor P10 and P-regions 63 and 64 form the source and drain regions of P-conductivity type transistor P20. The N-conductivity type transistors are formed in P-regions 67 and 70, denoted P-well No. 1 and No. 2, respectively. N-regions 65 and 66 diffused in P-region 67 form the source and drain regions of transistor N10, and N regions 68 and 69 form the source and drain regions of transistor N20. Transistor N30 (not shown in FIGURE 3) would preferably have its source and drain formed in the same P-well as transistor N20.

Overlying the path between the source and drain regions is an insulator layer such as silicon dioxide over which is formed a gate electrode. The potential applied to the gate electrode controls the conductivity of the channel region. The gate region of transistor N10 is shown connected to the gate of transistor P10; the two gates being connected in common to terminal 19.

Region 65 defined as the source of transistor N10 is connected to P-region (which is the local substrate of transistor N10) and to the source of potential V1. The drain 61 of transistor P10 is connected to the drain 66 of transistor N10 and to the gate of transistor P20 at terminal 14. The source 68

of transistor N20 is connected to P-region 70 (which is the local substrate of transistor N20) to the potential V2. The gate electrode of transistor N20 is connected to terminal 18. Drain region 69 of transistor N20 is connected to drain region 63 of transistor P20 at terminal 16. The source regions 62 and 64 of transistors P10 and P20 are connected to the semiconductor body 60 (which is the local substrate of these transistors) and to the potential V_{DD}.

As indicated in FIGURES 2 and 3, all the P-type transistors (P10, P20, P30) have their sources and their common substrate 60 connected to a common point of potential (V_{DD}). Transistor N10 has its source and its local substrate, P-well region 67, connected to a potential (V1) and transistors N20 and N30 have their sources and their local substrate, P-well region 70, connected to a potential V2. Thus, each transistor has its source connected to the same potential as its well or substrate. Operating the transistors with zero volts between their sources and substrates ensures that the threshold voltage of the devices is not increased above its nominal value at zero reverse bias. This permits the design of circuits and their reliable operation at values of operating potential which are nearly equal to the value of the threshold voltage. That is, a device with a V_T of 1 volt can be operated from a 1.3 volt or 1.5 volt supply. It also permits the design of interface circuits between circuits operating at widely different potentials. This technique is also extremely valuable for use in conjunction with circuits operating at extremely low voltages (e.g. 1.5 volts) where a small increase in V_T may render the circuit inoperable or marginally operable.

In contrast to the Figure 1 circuit, each transistor, in circuits embodying the invention, has its source connected to the same potential as its substrate.

Also, the common substrate is maintained at a fixed potential and the well-regions are designed to receive the different voltage levels applied to the circuit. These features enable, in part, the design of circuits in which no transistor is subjected to a reverse bias between its source and substrate.

In circuits where transistors formed on a common substrate are operated at different potentials it is possible for the source region of some transistors to be forward biased with respect to their substrate, resulting in catastrophic failure. For example, in FIGURE 1, if a V_{D1} of 3 volts is applied to the source of transistor P1 while V_{D2} is at ground, the source-to-substrate region of transistor P1 has 3 volts connected across. The source-to-substrate region so biased presents a low impedance, forward baised junction between two power supplies (V_{D1} and V_{D2}), allowing a large current to pass therethrough. The current may be so high that the region burns out or the metal connected thereto melts. In contrast thereto, in circuits embodying the invention, the sources of the transistors are at the same potential as their substrate, and regions at different potentials are isolated from each other. As a result, there cannot be a condition of forward bias between a source region and a substrate. Accordingly, the possible destruct condition is eliminated.

Returning to FIGURE 2, the operation of the circuit is best explained by assuming that $+V_{DD}$ volts is ground potential (0 volts), that V1 is -1.5 volts, and that V2 is -20 volt. In addition, assume that the V_T of the P type and the N type transistors with zero source to substrate bias is 1.0 volts. Assume, also, that the input signals present at terminal 19 vary between 0 volts (V_{DD}) and -1.5 volts (V1).

A signal of zero volts applied to terminal 19 turns off transistor P10 while causing transistor N10 to conduct, thereby clamping terminal 14 to -1.5 volts. Under this condition, -1.5 volts is applied to the gate of transistor P20 while zero volts is applied to the gate of transistor P30. Transistor P20, with 1.5 volts between its gate and source, conducts causing terminal 16 to rise in potential towards zero volts. The rising potential at terminal 16 turns on transistor N30, which clamps terminal 18 to -20 volts. Thus, the zero volt level signal present at terminal 19 results in the production of a zero volt level signal at terminal 16 and a signal level of -20 volts at terminal 18.

In response to the presence of a -1.5 volt level signal at terminal 19, transistor P10 is turned on and transistor N10 is turned off. In the circuit of FIGURE 2 the V_T of P10 remains at its low value of 1.0 volt since the source and the substrate are tied in common to zero volts. Therefore, when -1.5 volts is applied to its gate, transistor P10 is turned fully on. With transistor P10 turned on, zero volts is applied to terminal 14 which cuts off transistor P20. Concurrently, the -1.5 volts applied to input terminal 19 turns on transistor P30. Transistor P30 when turned on applies zero volts to terminal 18 which turns on transistor N20 to clamp terminal 16 to -20 volts. With output terminal 16 clamped to -20 volts, transistor N30 is cut off. Therefore, terminal 16 is at -20 volts while terminal 18 is at zero volts in response to the -1.5 volt level at terminal 19.

The signals at terminals 16 and 18 are thus -20 volts and 0 volts, respectively, when the signal at terminal 19 is -1.5 volts and the signals at terminals 16 and 18 are zero volts and -20 volts, respectively,

when the signal at terminal 19 is zero volts.

It has thus been shown that in circuits embodying the invention, a low level input signal may be level shifted to produce a much larger output signal with little power dissipation and with very few components. The low power dissipation results both from the type of circuit (complementary symmetry) and from the fact that the input signals may be low level signals obtained from a low power circuit.

WHAT WE CLAIM IS:

1. A field effect integrated circuit having a semiconductor body of first conductivity type in which there are regions of second conductivity type for forming the sources and the drains of transistors of second conductivity type, and at least two well-regions of said second conductivity type also within said semi-conductor body with regions of first conductivity type within said well-regions for forming the sources and the drains of transistors of first conductivity type; means for applying a reference potential to said semiconductor body; means for applying a first voltage level to one of said well-regions; means for applying a second voltage level, different from the first, to a second one of said well-regions; and means for applying to the source of each transistor the same potential as is applied to the semiconductor body or well region (as the case may be) in which it is formed, thereby to eliminate any reverse bias between the transistor's source and the semiconductor body or well-region in which the transistor is formed.

2. The integrated circuit as claimed in claim 1 wherein at least one transistor of first conductivity type from each of said well-regions has its drain electrode connected to the drain of a transistor of second conductivity type formed in said semiconductor body for forming a complementary inverter.

3. The integrated circuit as claimed in claim 2 wherein said transistors are insulated-gate field-effect transistors and wherein said first conductivity type is N-type conductivity and said second conductivity type is P-type conductivity.

4. An integrated circuit as claimed in claim 1 including means connecting the drain region of one transistor of first conductivity type from said one well region to the drain region of one transistor of said second conductivity type for forming a first complementary inverter and means connecting the drain region of one transistor of first conductivity type from said second well region to the drain region of one transistor of said second conductivity type for forming a second complementary inverter, said first complementary inverter being receptive to signals varying between said first voltage level and said reference potential for producing output signals applied to said second inverter, said output signals varying between said first voltage level and said reference potential and said second complementary inverter producing in response to the output signals of said first complementary inverter signals varying between said second voltage level and said reference potential.

5. An integrated sircuit as claimed in any preceding claim having a direct connection between the source of each transistor and the semiconductor body or well region (as the case may be) in which the transistor is formed.

6. An integrated circuit substantially as hereinbefore described with reference to Figures 2 and 3 of the accompanying drawing.

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London. W1Y 8EU
Agent for the Applicant.

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when the signal at terminal 19 is zero volts.

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2. The integrated circuit as claimed in claim 1 wherein at least one transistor of first conductivity type from each of said well-regions has its drain electrode connected to the drain of a transistor of second conductivity type formed in said semiconductor body for forming a complementary inverter.

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Chartered Patent Agent,
50 Curzon Street,
London. W1Y 8EU
Agent for the Applicant.

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