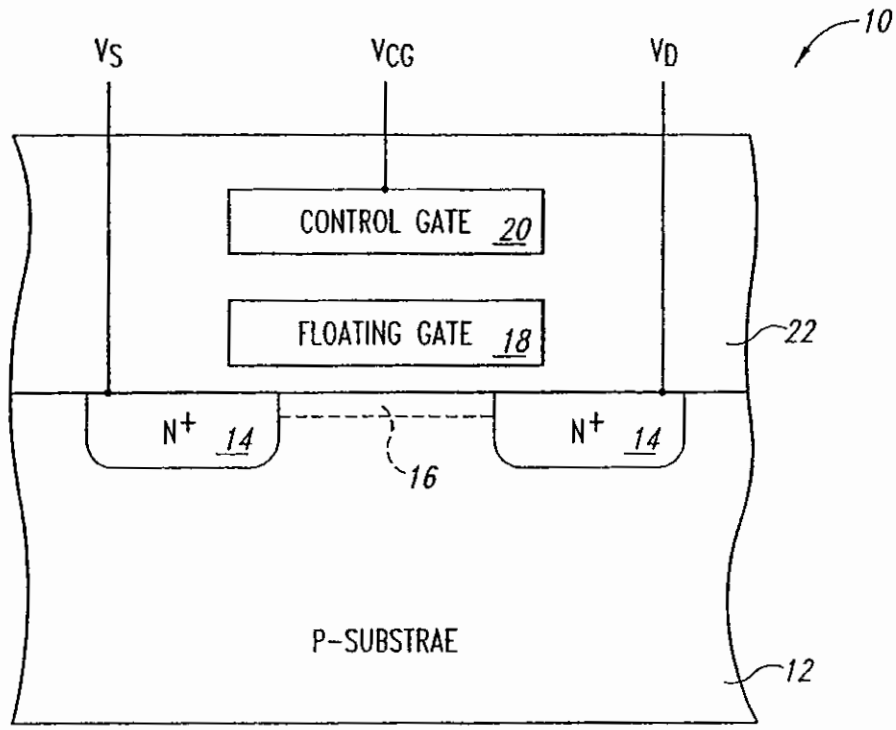


Fig. 1
(Prior Art)

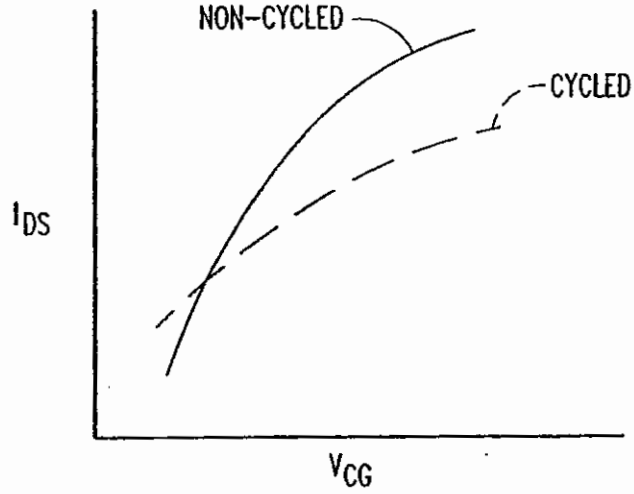


Fig. 2
(Prior Art)

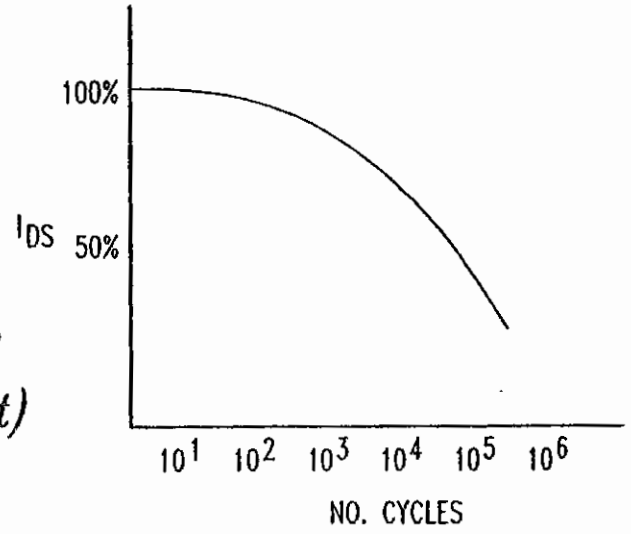


Fig. 3
(Prior Art)

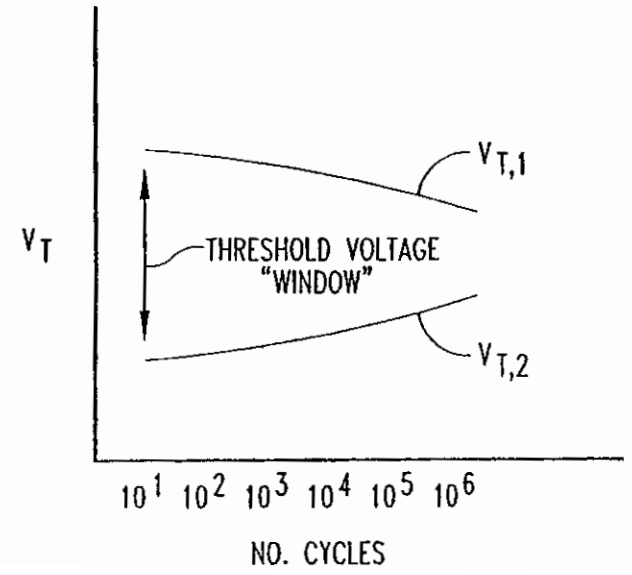


Fig. 4
(Prior Art)

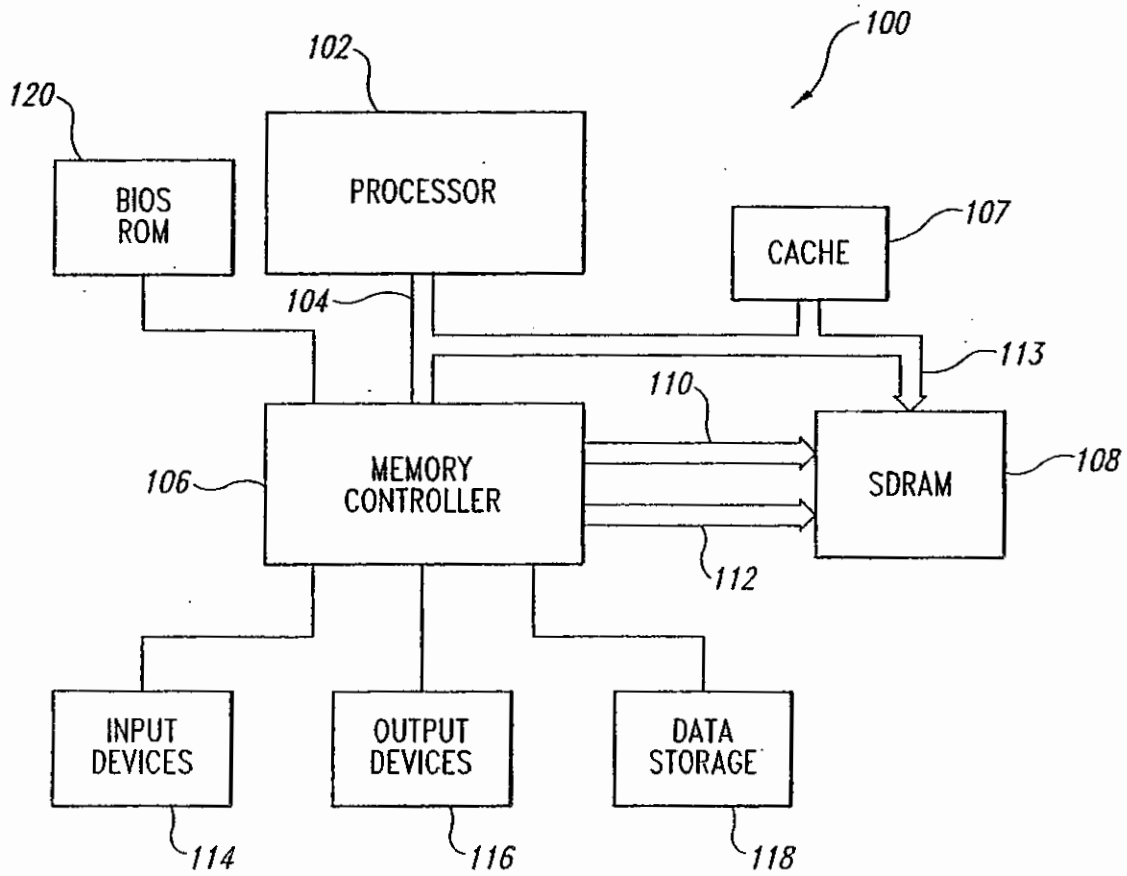

100
102
120
BIOS ROM
PROCESSOR
CACHE
107
104
113
110
106
MEMORY CONTROLLER
SDRAM
108
112
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
114
116
118

Fig. 5

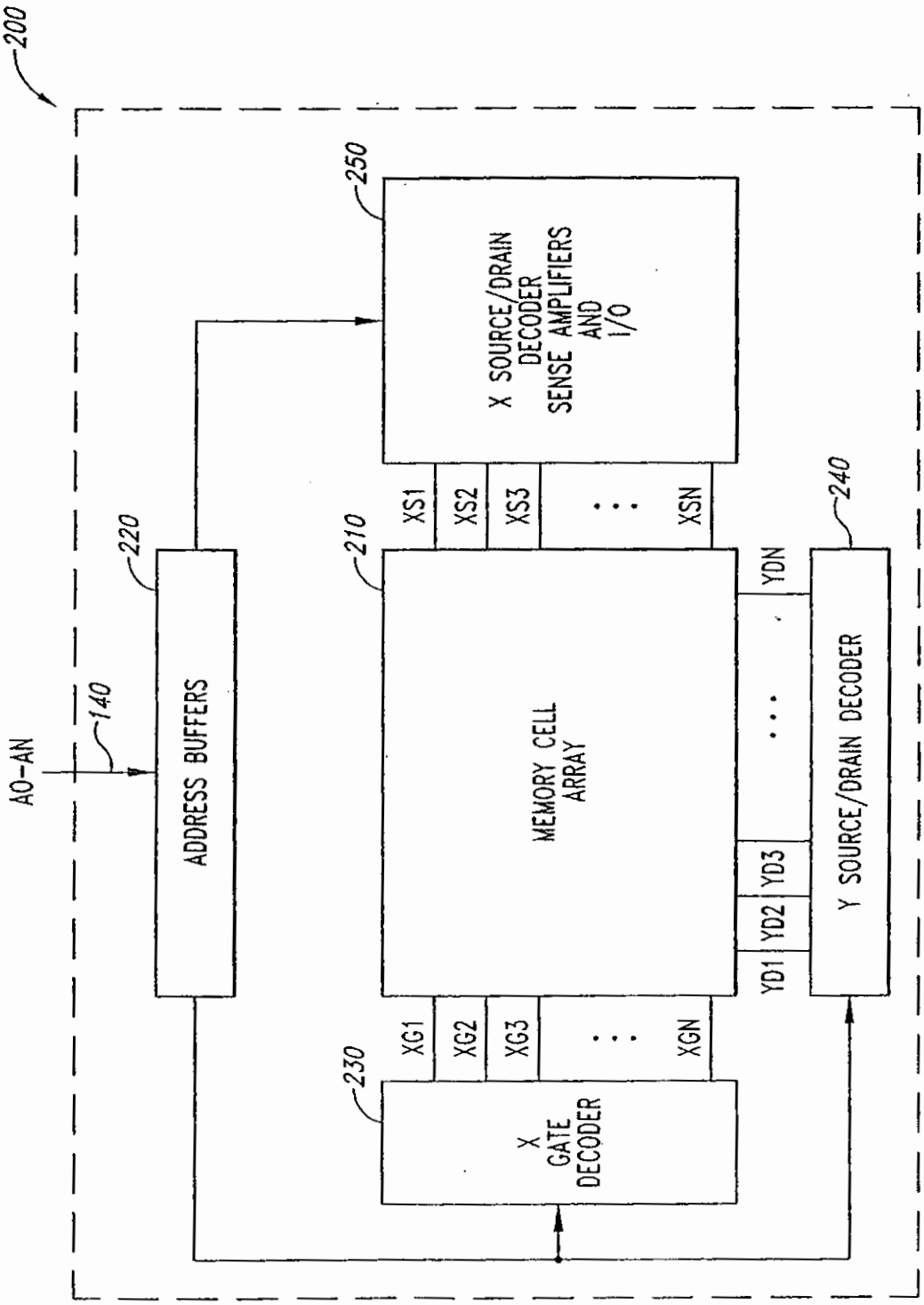
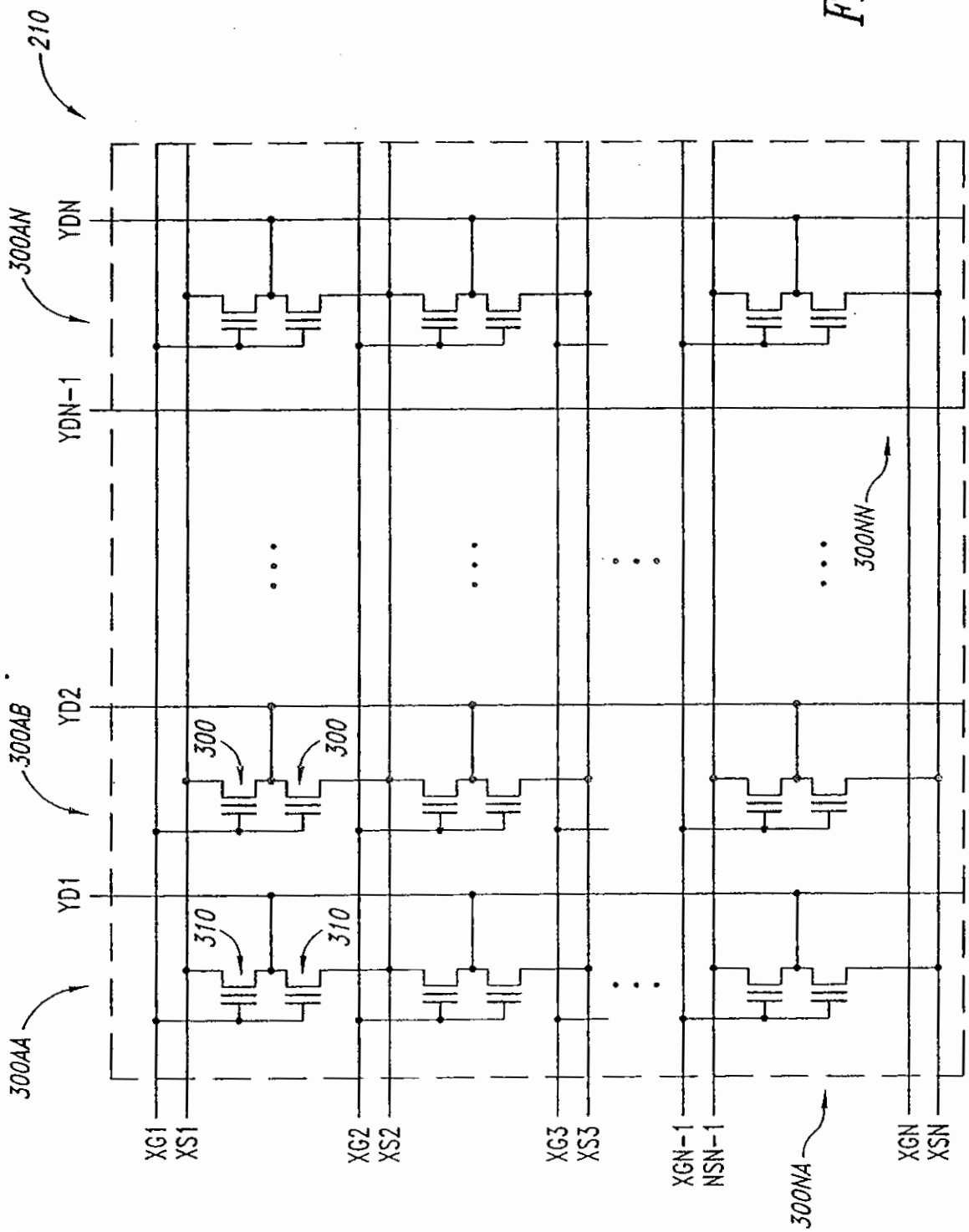

200
250
X SOURCE/DRAIN DECODER SENSE AMPLIFIERS AND I/O
XS1
XS2
XS3
XSN
220
210
240
YDN
ADDRESS BUFFERS
MEMORY CELL ARRAY
Y SOURCE/DRAIN DECODER
140
A0-AN
YD3
YD2
YD1
XG1
XG2
XG3
XGN
230
X GATE DECODER

Fig. 6

Fig. 7


210
300AN
YDN
YDN-1
300AB
YD2
YD1
300AA
300
300
310
310
300NN
300NA
XG1
XS1
XG2
XS2
XG3
XS3
XGN-1
NSN-1
XGN
XSN

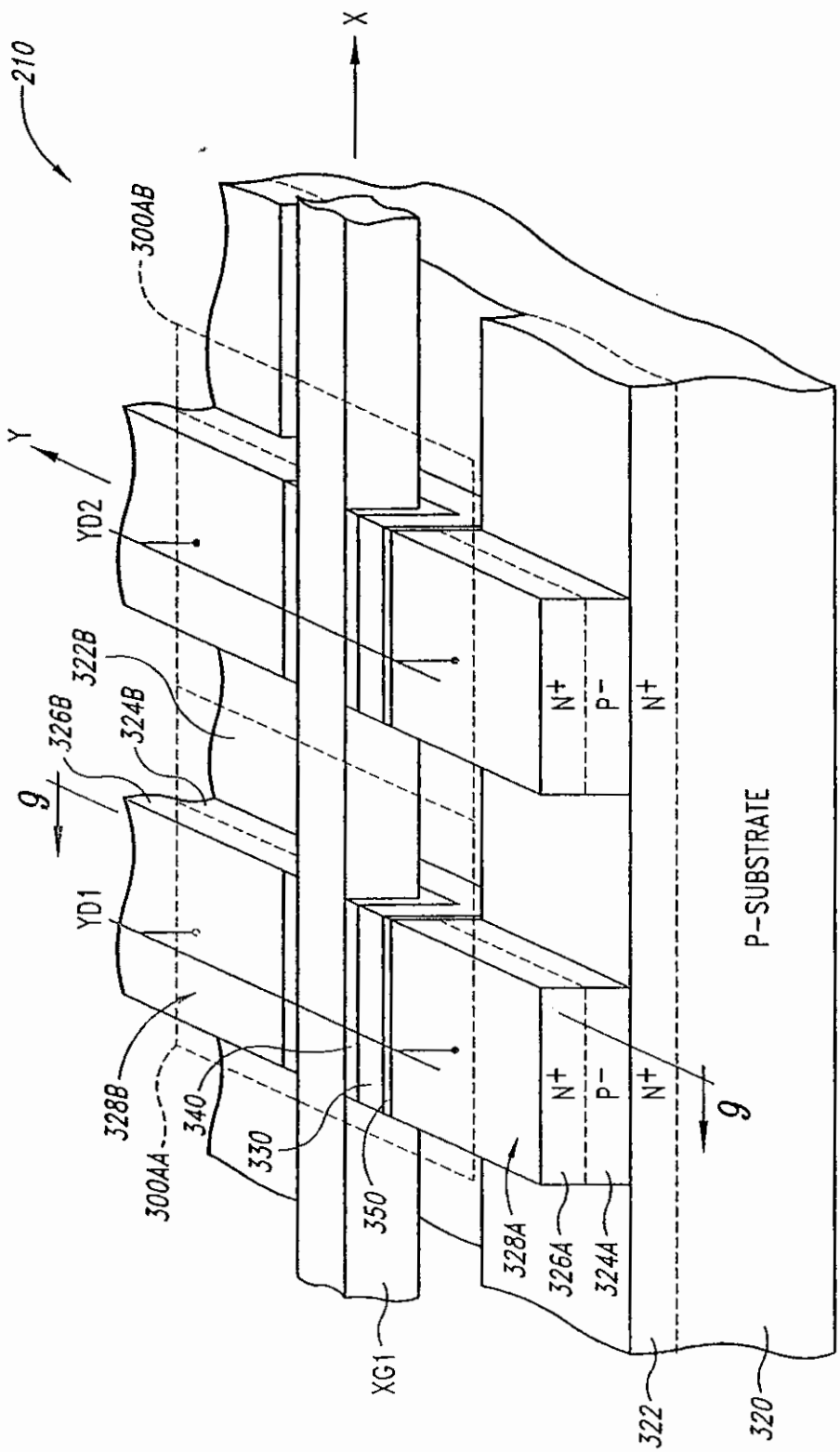

210
X
Y
300AB
YD2
322B
326B
324B
9
YD1
328B
340
300AA
330
350
XG1
328A
326A
324A
N+
P-
N+
P-SUBSTRATE
322
320

Fig. 8

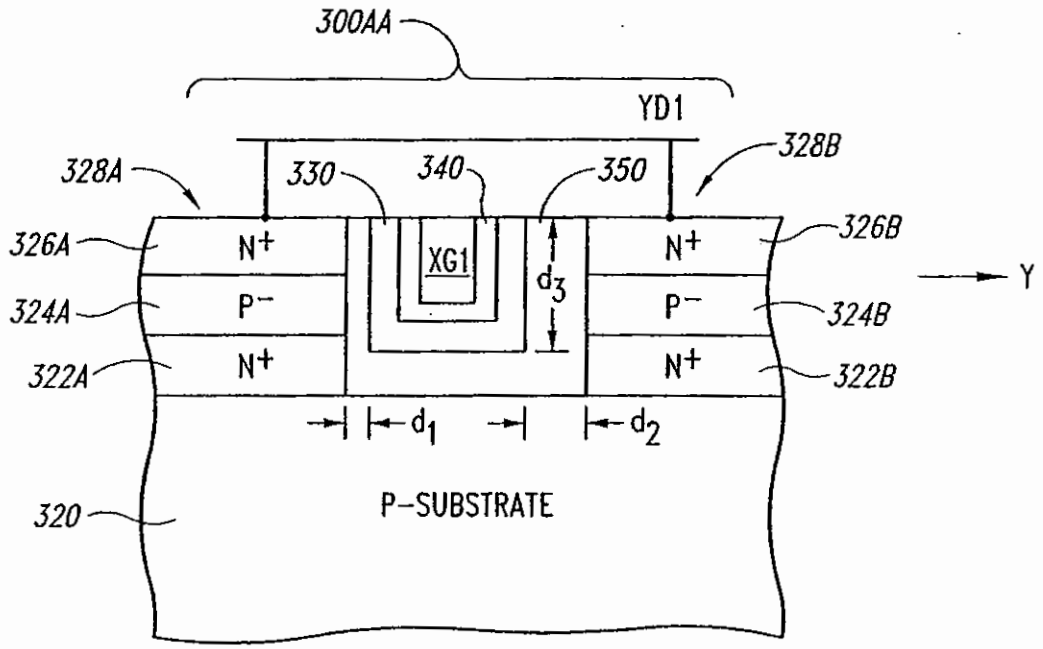

300AA
YD1
328A
330
340
350
328B
326A
N+
XG1
d3
N+
326B
Y
324A
P−
P−
324B
322A
N+
N+
322B
d1
d2
320
P−SUBSTRATE

Fig. 9

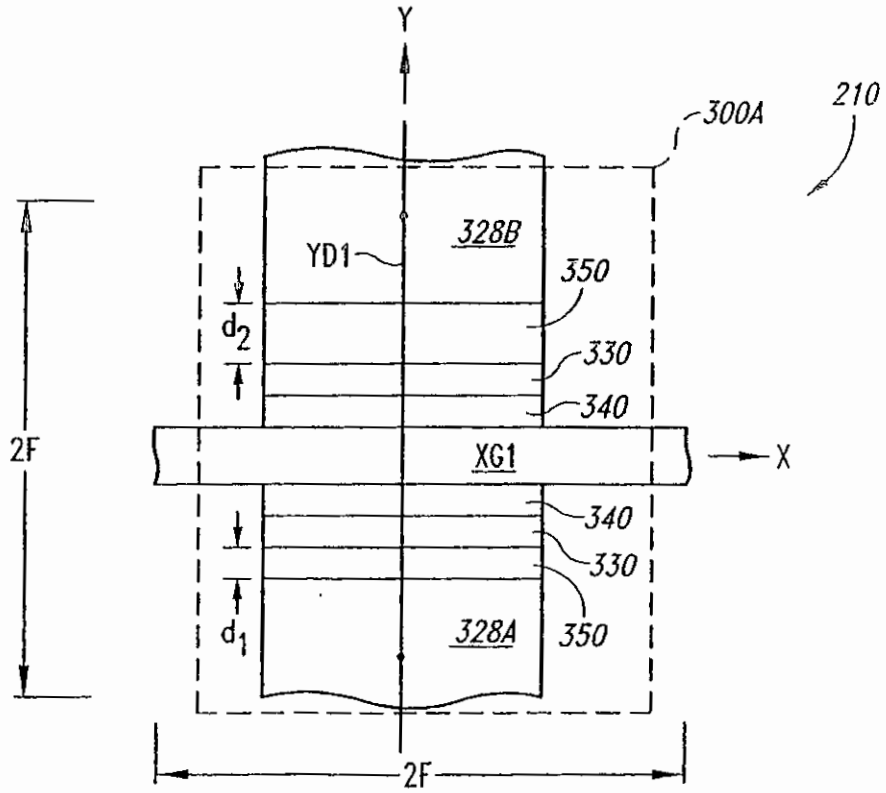

Y
300A
210
328B
YD1
350
d2
330
340
2F
XG1
X
340
330
d1
328A
350
2F

Fig. 10

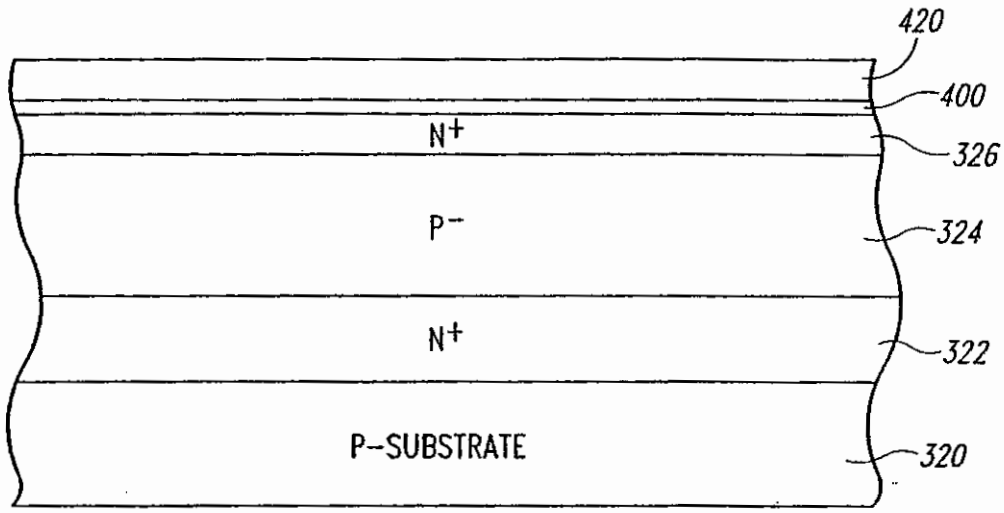

420
400
N+
326
P−
324
N+
322
P−SUBSTRATE
320

Fig. 11

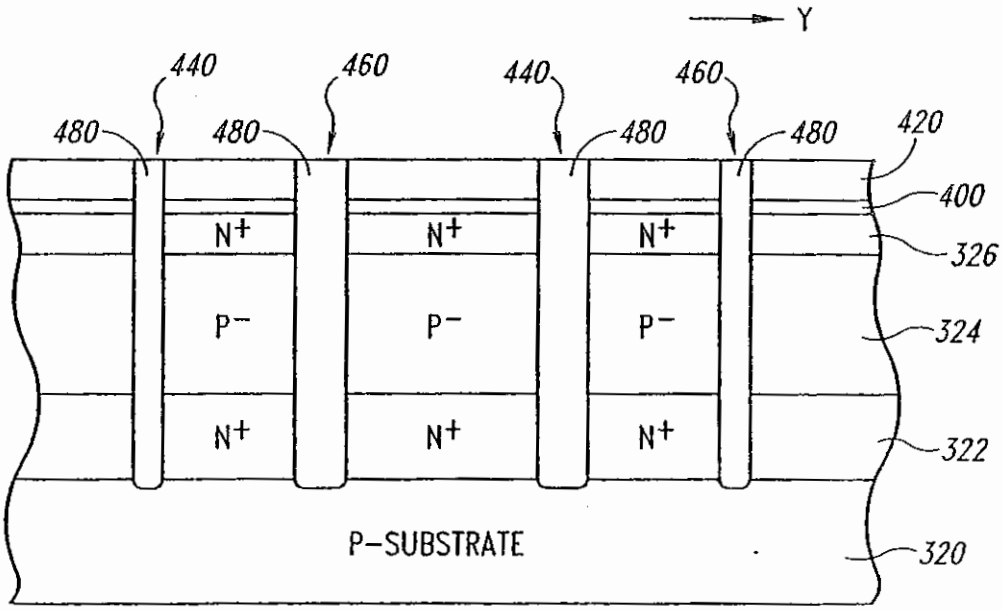

Y
440
460
440
460
480
480
480
480
420
400
N+
N+
N+
326
P−
P−
P−
324
N+
N+
N+
322
P−SUBSTRATE
320

Fig. 12

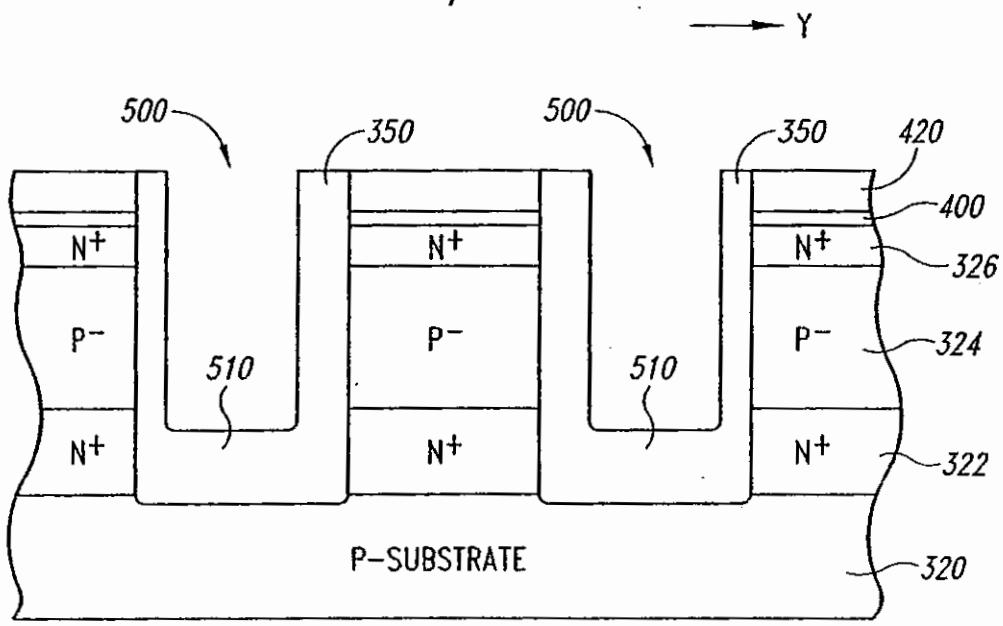

Y
500
350
500
350
420
400
N+
N+
N+
326
P−
P−
P−
324
510
510
N+
N+
N+
322
P−SUBSTRATE
320

Fig. 13

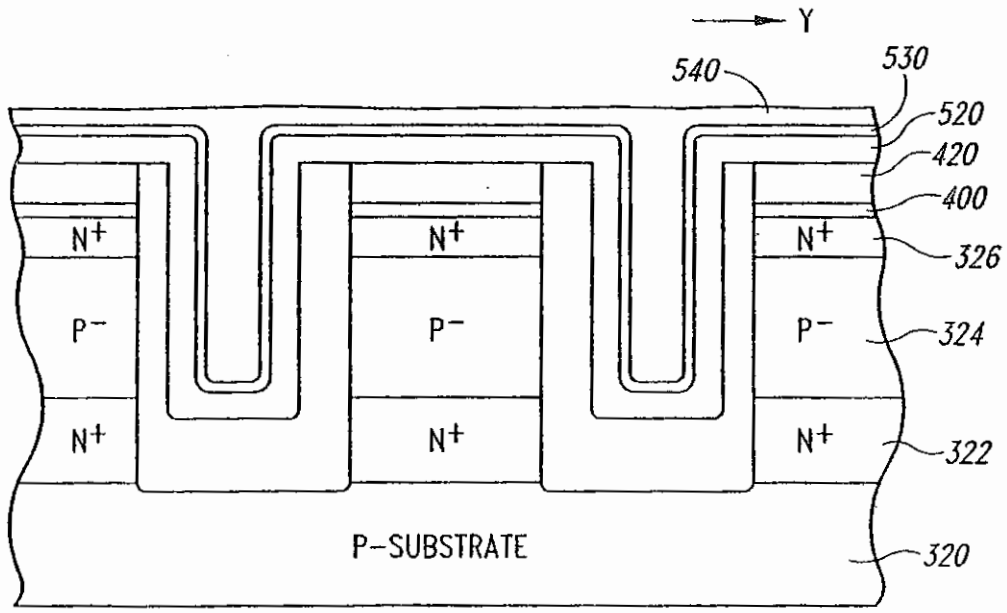

Y
540
530
520
420
400
N+
N+
N+
326
P−
P−
P−
324
N+
N+
N+
322
P−SUBSTRATE
320

Fig. 14

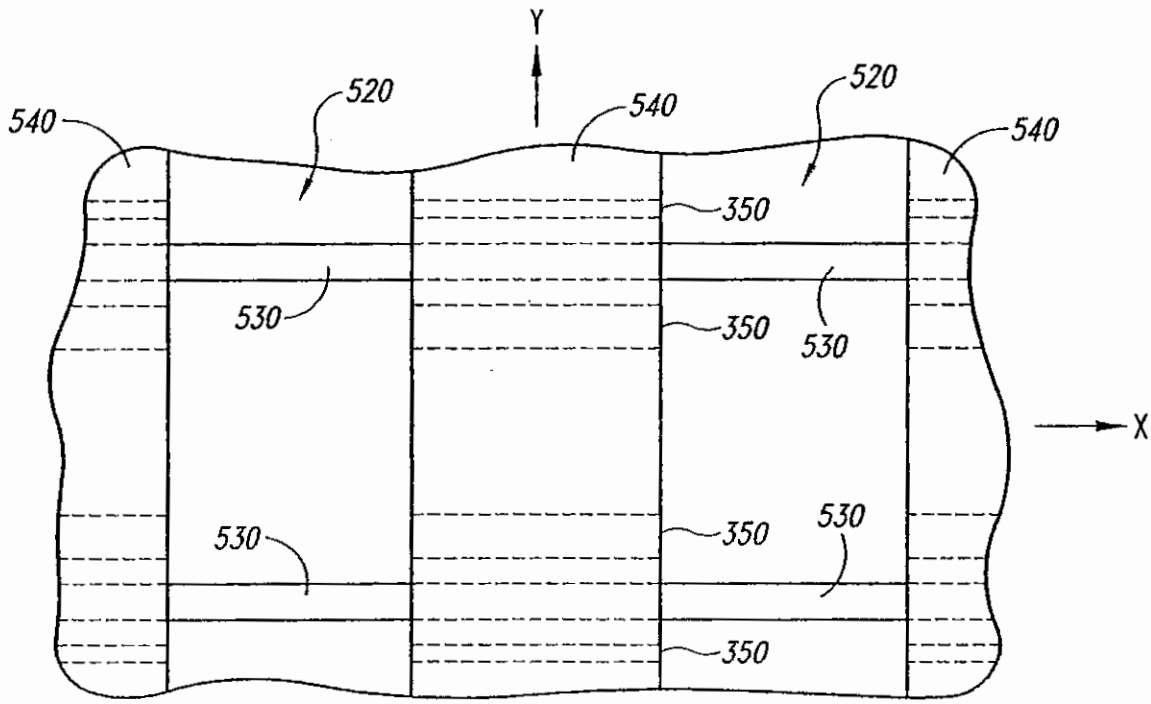


Fig. 15

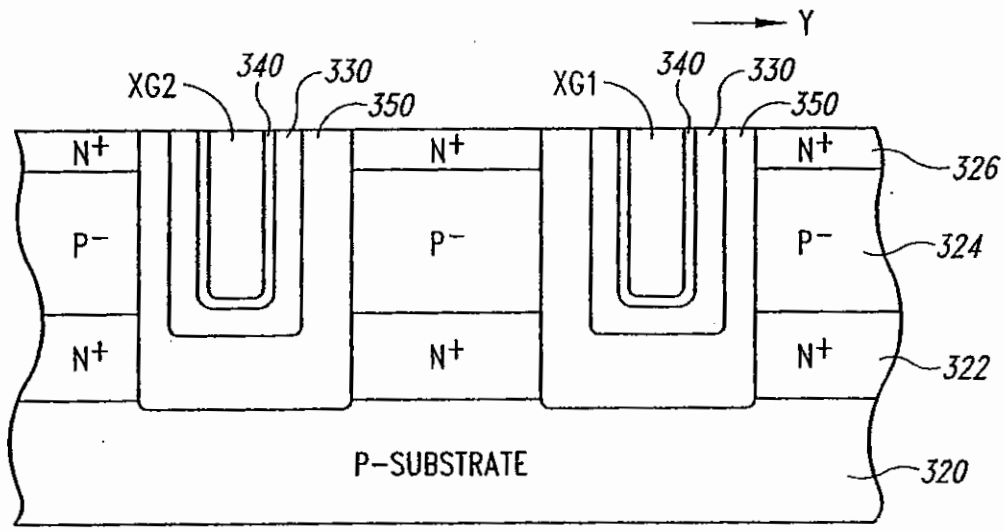

Y
XG2
340
330
350
XG1
340
330
350
N+
P−
N+
N+
P−
N+
N+
P−
N+
326
324
322
P−SUBSTRATE
320

Fig. 16

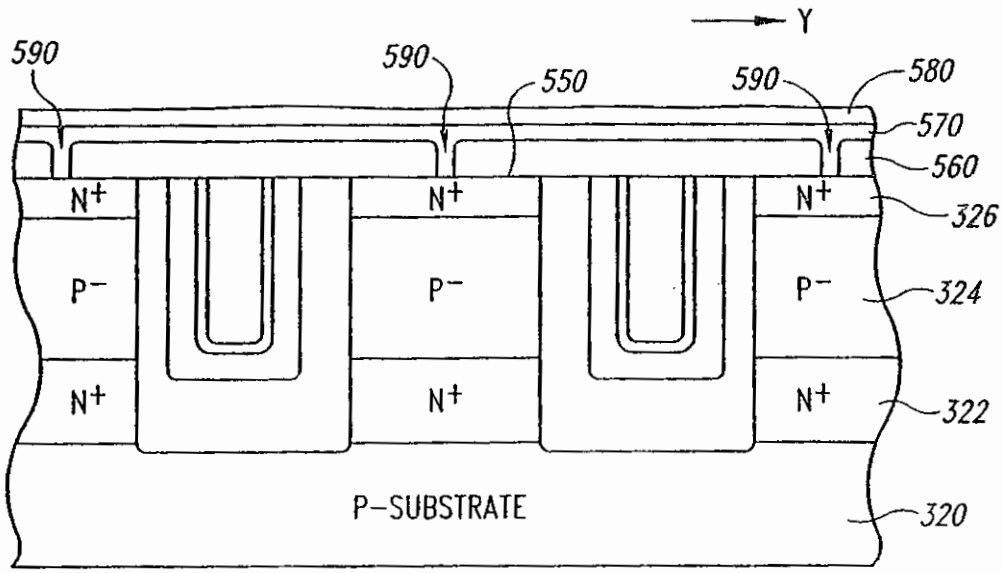

Y
590
590
550
590
580
570
560
N+
P−
N+
N+
P−
N+
N+
P−
N+
326
324
322
P−SUBSTRATE
320

Fig. 17