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(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPOSED OF INSULATED GATE FIELD-EFFECT TRANSISTORS

(71) We, HITACHI LIMITED of 1—5—1 Marunouchi, Chiyoda-Ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an integrated circuit device including insulated gate field-effect transistors (hereinafter referred to as "MOSIC") and also to a method of manufacturing such an integrated circuit.

In general, a MOSIC uses aluminium or silicon as the material of a gate electrode. On the other hand, there are known integrated circuits (hereinafter referred to as ICs) in which, in an inverter stage forming one internal circuit thereof, a load MOSFET of the enhancement mode is employed as the load of a driving MOSFET operative in the enhancement mode (hereinafter called "E/E type IC") and there are also known ICs in which a load MOSFET of the depletion mode is employed (hereinafter called "E/D type IC"). Among such ICs, the silicon gate MOSIC employing the depletion load has recently been extensively adopted as a device which is of higher performance for various uses, and has a higher density of integration than the aluminium gate MOSIC. We have found that the area occupied by an Si gate MOS transistor having the self-aligned gate structure is reduced by approximately 20 to 30% as compared with that of an Al gate MOS transistor.

As the result of an investigation of MOSICs commercially available as produced by several manufacturers, however, it has been found that, in a read only memory (hereinafter referred to as "ROM") which occupies a considerable part of a MOSIC chip, the size of a single bit of the ROM is not always substantially smaller in the conventional Si gate ROM structure than in the Al gate structure, as indicated in Table 1:

TABLE 1:

Comparisons of ROM bit sizes

IC manufacturer	Si gate ROM	Al gate ROM	type of IC
A	–	336 μm^2	dynamic type
B	616 μm^2	650 μm^2	static type
C	525 μm^2	–	static type
D	412 μm^2	–	static type
E	441 μm^2	432 μm^2	static type

One prior art Si gate MOS—ROM will now be described with reference to Figures 1, 2*a* and 2*b* of the accompanying drawings, wherein:—

Figure 1 is a circuit diagram of a prior-art Si gate ROM;

Figure 2*a* is a plan view showing a part of the prior art Si gate ROM on an enlarged scale; and

Figure 2*b* is a sectional view of a part of the prior art Si gate MOS—ROM as taken along the line X—X′ in Figure 2*a*.

As illustrated in Figure 1, the prior art Si gate MOS—ROM consists of MOSFETs which are arranged in parallel between the output line and ground. The normal states of the respective memory cells are determined by the thicknesses of gate oxide films. A signal of low level close to a supply voltage is applied to a selected address line, whereas a signal of high level close to zero volts, is applied to unselected address lines. Considering, by way of example, a case where a line IN_2 is selected, the MOSFET underlying this line has the thick gate oxide film and is usually "off", so that the output level is at the low level. As shown in Figures 2*a* and 2*b*, such a prior-art ROM is constructed of P^+-type diffused layers 2, 3 and 4; polycrystalline silicon layers 7 and 8; silicon dioxide films 5 and 6; phosphosilicate glass 9; a through-hole 11; and an aluminium layer 10. The polycrystalline silicon layers are used as an address input line, while the aluminium layer is used as an output line. The through-holes between the Al layer and the P^+-type diffused layers are necessary for commonly connecting the drain electrodes of the MOSFETs which are arranged at each row. As shown, the states of the memory cells at the points of intersection between the input lines and the output lines are determined by the thicknesses of the gate oxide films. More specifically, where a MOSFET, which conducts the normally "on" to "off" operation by the signal voltage applied to the input line, is necessary at a certain point of intersection, the gate oxide film beneath the polycrystalline Si layer at that place is made thin, while where a MOSFET, which conducts the normally "off" to "on" operation, is necessary, the oxide film beneath the polycrystalline Si layer at that place is made thick. Thus, a ROM having a predetermined bit pattern is constructed. The minimum size per unit bit of the Si gate ROM of such construction is about 410 μm^2, and it is substantially equal to that of the Al gate ROM.

As described above, the conventional ROM is characterized by the following construction:

(1) The normal states of the respective memory cells are determined by the thicknesses of the gate oxide films.

(2) Since the self-aligned gate structure is adopted, the polycrystalline Si layer cannot cross over the P^+-type diffused layer. Therefore, the Al wiring layer is necessitated, and the through-hole is required between the P^+-type diffused layer and the Al layer.

Accordingly, the occupying area per bit of the prior art Si gate ROM cannot be made small in spite of the adoption of the self-aligned structure.

According to one aspect of the present invention, there is provide a semiconductor integrated circuit device with insulated gate field effect transistors arranged in a matrix configuration, comprising:

(a) a plurality of gate wiring strips arranged in parallel with an apart from each other along columns of the matrix on an insulating layer lying on a semiconductor substrate of a first conductivity type, said insulating layer having relatively thin gate insulating film portions arranged so as to be spaced under each of said gate wiring strips along rows of the matrix; and

(b) a plurality of semiconductor regions of a second conductivity type opposite to the first conductivity type arranged in parallel with and apart from each other along said rows of the matrix so as to extend between the adjacent gate wiring strips in connection with the portions of the device at which said gate wiring strips cross said gate insulating film portions;

wherein each of the portions at which said gate wiring strips cross said gate insulating film portions acts as an insulated gate field effect transistor in cooperation with said semiconductor regions at both sides thereof, said gate insulating film portions of said insulated gate field effect transistors having substantially equal thicknesses, selected ones of said insulated gate field effect transistors being the depletion type and the others of said insulated gate field effect transistors being the enhancement type.

According to another aspect of the present invention, there is provided a method of manufacturing a semiconductor integrated circuit device including insulated gate field-effect transistors, comprising the steps of:

(a) forming an insulating layer on the surface of a semiconductor substrate of a first conductivity type, said insulating layer having alternating parallel relatively thin and relatively thick strip portions;

(b) selectively implanting ions of impurities of a second conductivity type, opposite said first conductivity type, into predetermined surface portions of said substrate beneath selected areas of the relatively thin strip portions of said insulating layer through said insulating layer

to form channel regions of selected ones of said transistors;

(c) forming parallel gate wiring strips on said insulating layer, said gate wiring strips extending perpendicularly to said relatively thin and thick strip portions of the insulating layer so as to cross said predetermined surface portions and being spaced apart from each other;

(d) doping further impurities of said second conductivity type into the surface of said semiconductor substrate at both sides of each of said gate wiring strips by using said gate wiring strips as a mask to form semiconductor regions of said second conductivity type extending between the adjacent gate wiring strips in connection with the portions of the device at which said gate wiring strips cross said relatively thin strip portions of the insulating layer; whereby ion-implanted said portions at which said gate wiring strips cross said relatively thin strip portions of the insulating layer serve as depletion type insulated gate field effect transistors while the other said portions at which the strips cross serve as enhancement type insulated gate field effect transistors.

Embodiments of the present invention will now be described by way of example, with reference to the remaining figures of the accompanying drawings, wherein:—

Figure 3 is a circuit diagram of one preferred form of MOS—ROM;

Figure 4*a* is an enlarged plan view, and Figures 4*b* and 4*c* are sectional elevation views of a part of the MOS—ROM;

Figure 5 is a circuit diagram showing a particular application of the MOSROM:

Figures 6*a* to 6*f* and Figures 7*a* to 7*d* are enlarged elevation sectional views and plan views respectively of a part of the MOS—ROM for explaining the manufacturing process of the MOS—ROM;

Figures 8*a* and 8*b* are top pattern diagrams of large scale integration chips (hereinafter referred to as "LSI" chips) of a MOS—LSI manufactured in accordance with the present invention, and a MOS—LSI manufactured in accordance with a prior art technique for comparison purposes; and

Figure 9*b* is a diagram showing an example of a circuit in which the MOS—ROM is employed, whilst Figure 9*a* is a graph showing the measured results of speeds of operation of the circuit shown in Figure 9*b*.

Referring first to Figure 3, the ROM is composed of a plurality of enhancement mode and depletion mode MOSFETs, which are connected in series as driving elements. For example, the enhancement mode MOSFETs can be formed under address lines IN_1, IN_3, IN_5 ..... IN_n, whereas the depletion mode MOSFETs can be formed under address lines IN_2, IN_4, IN_6 ..... IN_{n-1}. The depletion mode MOSFETs function additionally as resistance element. A read-out is stably executed by impressing a signal of high level close to zero volts on a selected address line. At this time, a signal of low level is impressed on the unselected address lines.

By way of example, in the case where the address line IN_2 is selected (by applying to it a high level signal i.e. zero volts), the MOSFET underlying this address line IN_2 remains "on", irrespective of the high level signal, as it is a depletion mode MOSFET. Since the MOSFETs associated with other address lines, such as IN_1, IN_3, to IN_n, are enhancement mode MOSFETs, they turn "on" by having a low level signal (—V volts) applied to their gates. Since the MOSFET associated with the address line IN_{n-1} is a depletion mode MOSFET, it also is "on" irrespective of the low level signal is applied to its gate. In this case, accordingly, all the driving elements are substantially "on", so that an output signal of high level close to zero volts is produced at an output terminal OUT.

On the other hand, in the case where the address line IN_3 is selected by applying a high level signal, the MOSFET associated with this line is turned off by the input signal of high level as it operates in the enhancement mode. Therefore, an output signal of low level appears at the output terminal OUT.

As is apparent from the above explanation, in the ROM according to this invention, the output data line to be precharged holds the low level, or is shifted to the high level in dependence on whether an enhancement or depletion mode MOSFET is addressed, respectively.

Figure 5 shows a ROM circuit which is constructed by applying this invention to an actual ROM of a MOSIC on the basis of the circuit illustrated in Figure 3. The ROM circuit comprises a first address decoder MOS matrix 23 and a second MOS—ROM matrix 24 receiving an output of the first MOS matrix as its input. The first matrix 23 has K input lines I_1 to I_k, where k is an even number. A flip-flop circuit 21 for storing signals to be applied to the input lines I_1 to I_k consists of a plurality of stages (for example, k/2 stages) connected in cascade. Outputs from the respective stages are delivered directly or through inverter circuits 22 via the input lines I_1 to K into the first MOS matrix 23, whose outputs are delivered into the second MOS matrix 24 through output lines A_1 to A_m. The second MOS matrix 24 provides outputs OUT 1 to OUT n from lines B_1 to B_l. The matrices 23 and 24 have one MOSFET operative in either the

depletion or enhancement mode in any one of the places in which input lines and output lines intersect. As indicated in the drawing, the depletion type MOSFETs are circled and indicated by reference numeral 25, whereas the enhancement type MOSFETs are uncircled and indicated by the reference numeral 26. Such MOSFETs are connected in series across a source of supply voltage V_{DD}, at every column, the other terminal of the source of supply voltage being connected to earth. Enhancement mode MOSFETs 27 and 28 are connected to the respective matrices 23 and 24 as loads. The gate electrodes of the MOSFETs 27 and 28 are supplied with clock pulse signals, $CLOCK_1$ and $CLOCK_2$ respectively.

Each of the plurality of inverters 22 consists of a driving MOSFET which operates in the enhancement mode, and a load MOSFET which is connected in series therewith and which operates in the depletion mode. As will be stated later, all the MOSFETs in the figure have gate insulating films (for example, SiO_2 films) of substantially equal thicknesses (about 500 to 1,500 angstroms) irrespective of the depletion mode or the enhancement mode. The depletion MOSFETs 25 in the MOS matrices 23 and 24 are formed simultaneously with the depletion MOSFETs in the inverters 22 by an identical process. The input lines of the first and second matrices 23 and 24 are formed of polycrystalline silicon wiring layers, while the connection from the output line of the first matrix to the input line of the second matrix is performed by the use of an aluminium wiring which connects a P^+-type diffused layer and the polycrystalline layer. The operation of the circuit in Figure 5 will be clear from a study of Figure 3. It should be noted that the two trains of clock pulses, $CLOCK_1$ and $CLOCK_2$, which are applied to the gate electrodes of the load MOSFETs 27 and 28 respectively, differ in phase, and that the amplitudes of these pulses (for example, −12 to −16 volts) are greater than the amplitude of the supply voltage V_{DD} (for example, −6 volts).

Referring now to Figures 4*a*, 4*b* and 4*c*, the structure of the MOS—ROM according to this invention will be described. Figure 4*a* is a plan view with a part of the MOS—ROM enlarged, whilst Figures 4*b* and 4*c* show sections along the lines X—X′ and Y—Y′ in Figure 4*a*, respectively. As shown, the MOS—ROM comprises an N-type single crystal Si substrate 31; P^+-type diffused layers 32 to 34 and 47 to 49, which are formed by being self-aligned by Si gate electrodes; gate insulating films 35, 36 and 43 consisting of silicon dioxide, which have essentially equal thicknesses (about 1,000 Å); input lines 37 and 38 of polycrystalline Si; an insulating film 39 of phosphosilicate glass; P-type channel layers 41 and 42 which are formed by implanting P-type impurity ions into selected areas of the surface of the substrate in order to form the depletion MOSFETs; and field insulating films 44 to 46 consisting of silicon dioxide, which are comparatively thick (about 1 to 2 μ). As apparent from the figures, one memory cell is formed in each of the places of intersection between the polycrystalline Si input lines 37 and 38, acting as the address input lines, and the P^+-type diffused layers as the self-connected data output lines. The normal states of the respective memory cells are determined by the presence or absence of the P-type channel formed by the ion implantation. All the memory cells have thin gate oxide films and operate as either enhancement or depletion MOSFETs.

The MOS matrix has a self-aligned gate structure and needs no through-holes. It will be appreciated that the area occupied by the single bit is substantially smaller in the MOS matrix of this invention than in the prior-art. Figures 8*a* and 8*b*, respectively, show by comparison the semiconductor chip sizes and the areas occupied by respective circuits in the cases where the MOSICs for achieving the same circuit function are formed by the technique of the present invention, and by the Si gate MOS manufacturing technique of the prior art. In Figs. 8*a* and 8*b* there can be seen areas occupied by an 8×10^3 bit ROM circuit, a shift register SR; and gate, flip-flop (F/F) and internal connecting circuits. By the adoption of the MOS matrix according to this invention, in comparison with the case of adopting the mere self-aligned type Si gate MOS—ROM, the ROM part, which occupies a comparatively large area in the LSI, can be reduced by approximately 50%. As the result, it becomes possible to reduce the whole chip size by approximately 20%.

The speed of operation of the ROM according to the present invention will now be explained with reference to Figures 9*a* and 9*b*. Since a ratioless circuit, as shown in Figure 9*b*, is employed, the output level of the ROM has two states, and as previously set forth, the precharged data line holds the low level or is shifted to the high level. In this case, the speed of operation of the ROM is mainly dependent upon the discharge time t_d in which the precharged data line is shifted to the high level. Figure 9*a* illustrates the measurements of the relationship between the discharge time t_d of the MOS—ROM shown in Figure 9*b* and the amplitude of the clock pulse V_{cp} supplied to the gate of the load MOSFET of the enhancement mode, the MOS—ROM possessing 48 address lines,

and having 48 enhancement or depletion MOSFETs connected in series. One of the curves in Fig. 9*a* illustrates the case in which the depletion type transistors of the ROM in Fig. 9*b* have a threshold voltage V th D of 2.3 volts; while the other is for V th D = 1.85 volts. The output capacitance of the ROM is approximately 1.5 pF. As seen from the graph, the discharge time t_d is smaller than 1.5 μs. When used as an integrated circuit for an electronic desk top calculator, there is no problem because an operation in the order of 100 KHz is thus possible.

The method of manufacturing the MOS—ROM according to this invention, as shown in Figures 4*a* to 4*c* and Figure 5, will now be described in greater detail with reference to Figures 6*a* to 6*f* and to Figures 7*a* to 7*d*. First, an SiO_2 film 40 being about 1.4 μ thick is formed in the surface of an N-type *Si* single crystal substrate 31, whose principal surface is the (1 1 1)-face, and which has a specific resistance in the range of from 5 to 8 ohm-cm. Thereafter, those parts of the SiO_2 film 40 on the principal surface of the substrate at which the MOSFETs are to be formed are removed in the shape of narrow slots. The exposed substrate surface is oxidized to form a thin SiO_2 film 30 (gate oxide film) of about 1,200 Å there (Figures 6*a* and 7*a*). Subsequently, boron ions are implanted into the substrate surface through the thin SiO_2 film 30 at a concentration of about 1.4×10^{11} atoms/cm^2, in order to control the overall carrier concentration of the surface in which MOSFETs are to be formed next. Further, a layer of photo-resistive material 50 is deposited on to that part of the thin oxide film 30 on the substrate surface at which depletion MOSFETs are not to be formed (Figure 6*b*). Using the photo-resistive layer and the thick oxide film 40 as a mask, boron ions are again implanted into the substrate surface through the exposed thin SiO_2 film at a concentration of 6.5×10^{11} atoms/cm^2. Thus, the P-type region 41 which constitutes the channel of the depletion type MOSFET is formed (Figures 6*b* and 7*b*). Subsequently the photo-resistive layer 50 is removed. Polycrystalline silicon is deposited on the entire oxide films to the extent of about 5,000 Å. Those parts of the polycrystalline Si layer which are other than parts for constructing the address lines (37, 38) are removed (Figure 6*c*). Subsequently, using the parts which form the address lines 37 and 38 of the polycrystalline Si layer left behind, the thin SiO_2 film 30 is removed to expose the substrate surface (Figures 6*d* and 7*c*). Subsequently, by employing the polycrystalline *Si* parts which form the address lines 37 and 38 and the thick SiO_2 film 40 as a mask, boron is diffused into the exposed substrate surface by a conventional vapour diffusion process. Thus, the P^+-type diffused regions 32, 33, 34, 47, 48 and 49, having a thickness of about 0.8 μ are formed (Figures 6*e* and 7*d*). Thereafter, a phosphosilicate glass film 39, having a thickness of about 0.9 to 1 μ is deposited from vapour, to complete the MOS—ROM as shown in Figure 6*f*. In this way, there is produced a MOS matrix composed of a combination of enhancement mode and depletion mode MOSFETs having gate oxide films of substantially equal thicknesses. As described above, in the MOS matrix the respective input lines of the polycrystalline Si and the respective P^+-type diffused layers intersect substantially orthogonally and all the insulating films under the polycrystalline Si layers in any place of the intersection are made of equal thickness of about 1,200 Å, so that the transistor operation is positively carried out. Which transistors are made the depletion type is determined by the implantation of the boron ions as illustrated in Figure 6*b*. Such a step of fabricating the depletion MOSFETs is not necessarily added to the manufacturing process. In the case of forming the circuit as shown in Figure 5 or Figure 9*b* within the surface of a single semiconductor substrate, the MOSFETs are fabricated by the same process as that of the other depletion MOSFETs, for example, the depletion load MOSFETs of the inverters.

To sum up, a ROM according to this invention can have the following features:

(1) The ROM is constituted by enhancement type and depletion type MOSFETs as the driving elements.

(2) The size of the ROM may be substantially reduced by about 50% as compared with that of the ROM of the prior art *Si* gate structure.

(3) The ROM can be fabricated by the process which is compatible with the Si gate MOS—LSI employing depletion loads as at present used extensively.

(4) The cascade ratioless circuit is applicable to the ROM, and LSIs with excellent characteristics can be realized by paying sufficient attention to the estimation of the operating speed.

The application of the present invention as stated above can also be applied to other complicated logical circuits, such as a programmable logic array and a four-phase ratioless dynamic circuit.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit device with insulated gate field effect transistors arranged in a matrix configuration, comprising:

(a) a plurality of gate wiring strips arranged in parallel with and apart from each other along columns of the matrix on

and having 48 enhancement or depletion MOSFETs connected in series. One of the curves in Fig. 9*a* illustrates the case in which the depletion type transistors of the ROM in Fig. 9*b* have a threshold voltage V th D of 2.3 volts; while the other is for V th D = 1.85 volts. The output capacitance of the ROM is approximately 1.5 pF. As seen from the graph, the discharge time t_d is smaller than 1.5 μs. When used as an integrated circuit for an electronic desk top calculator, there is no problem because an operation in the order of 100 KHz is thus possible.

The method of manufacturing the MOS—ROM according to this invention, as shown in Figures 4*a* to 4*c* and Figure 5, will now be described in greater detail with reference to Figures 6*a* to 6*f* and to Figures 7*a* to 7*d*. First, an SiO_2 film 40 being about 1.4 μ thick is formed in the surface of an N-type Si single crystal substrate 31, whose principal surface is the (1 1 1)-face, and which has a specific resistance in the range of from 5 to 8 ohm-cm. Thereafter, those parts of the SiO_2 film 40 on the principal surface of the substrate at which the MOSFETs are to be formed are removed in the shape of narrow slots. The exposed substrate surface is oxidized to form a thin SiO_2 film 30 (gate oxide film) of about 1,200 Å there (Figures 6*a* and 7*a*). Subsequently, boron ions are implanted into the substrate surface through the thin SiO_2 film 30 at a concentration of about 1.4×10^{11} atoms/cm^2, in order to control the overall carrier concentration of the surface in which MOSFETs are to be formed next. Further, a layer of photo-resistive material 50 is deposited on to that part of the thin oxide film 30 on the substrate surface at which depletion MOSFETs are not to be formed (Figure 6*b*). Using the photo-resistive layer and the thick oxide film 40 as a mask, boron ions are again implanted into the substrate surface through the exposed thin SiO_2 film at a concentration of 6.5×10^{11} atoms/cm^2. Thus, the P-type region 41 which constitutes the channel of the depletion type MOSFET is formed (Figures 6*b* and 7*b*). Subsequently the photo-resistive layer 50 is removed. Polycrystalline silicon is deposited on the entire oxide films to the extent of about 5,000 Å. Those parts of the polycrystalline Si layer which are other than parts for constructing the address lines (37, 38) are removed (Figure 6*c*). Subsequently, using the parts which form the address lines 37 and 38 of the polycrystalline Si layer left behind, the thin SiO_2 film 30 is removed to expose the substrate surface (Figures 6*d* and 7*c*). Subsequently, by employing the polycrystalline Si parts which form the address lines 37 and 38 and the thick SiO_2 film 40 as a mask, boron is diffused into the exposed substrate surface by a conventional vapour diffusion process. Thus, the P^+-type diffused regions 32, 33, 34, 47, 48 and 49, having a thickness of about 0.8 μ are formed (Figures 6*e* and 7*d*). Thereafter, a phosphosilicate glass film 39, having a thickness of about 0.9 to 1 μ is deposited from vapour, to complete the MOS—ROM as shown in Figure 6*f*. In this way, there is produced a MOS matrix composed of a combination of enhancement mode and depletion mode MOSFETs having gate oxide films of substantially equal thicknesses. As described above, in the MOS matrix the respective input lines of the polycrystalline Si and the respective P^+-type diffused layers intersect substantially orthogonally and all the insulating films under the polycrystalline Si layers in any place of the intersection are made of equal thickness of about 1,200 Å, so that the transistor operation is positively carried out. Which transistors are made the depletion type is determined by the implantation of the boron ions as illustrated in Figure 6*b*. Such a step of fabricating the depletion MOSFETs is not necessarily added to the manufacturing process. In the case of forming the circuit as shown in Figure 5 or Figure 9*b* within the surface of a single semiconductor substrate, the MOSFETs are fabricated by the same process as that of the other depletion MOSFETs, for example, the depletion load MOSFETs of the inverters.

To sum up, a ROM according to this invention can have the following features:

(1) The ROM is constituted by enhancement type and depletion type MOSFETs as the driving elements.

(2) The size of the ROM may be substantially reduced by about 50% as compared with that of the ROM of the prior art Si gate structure.

(3) The ROM can be fabricated by the process which is compatible with the Si gate MOS—LSI employing depletion loads as at present used extensively.

(4) The cascade ratioless circuit is applicable to the ROM, and LSIs with excellent characteristics can be realized by paying sufficient attention to the estimation of the operating speed.

The application of the present invention as stated above can also be applied to other complicated logical circuits, such as a programmable logic array and a four-phase ratioless dynamic circuit.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit device with insulated gate field effect transistors arranged in a matrix configuration, comprising:

(a) a plurality of gate wiring strips arranged in parallel with and apart from each other along columns of the matrix on

an insulating layer lying on a semiconductor substrate of a first conductivity type, said insulating layer having relatively thin gate insulating film portions arranged so as to be spaced under each of said gate wiring strips along rows of the matrix; and

(b) a plurality of semiconductor regions of a second conductivity type opposite to the first conductivity type arranged in parallel with and apart from each other along said rows of the matrix so as to extend between the adjacent gate wiring strips in connection with the portions of the device at which said gate wiring strips cross said gate insulating film portions;

wherein each of the portions at which said gate wiring strips cross said gate insulating film portions acts as an insulated gate field effect transistor in cooperation with said semiconductor regions at both sides thereof, said gate insulating film portions of said insulated gate field effect transistors having substantially equal thicknesses, selected ones of said insulated gate field effect transistors being the depletion type and the others of said insulated gate field effect transistors being the enhancement type.

2. A semiconductor integrated circuit device according to claim 1, in which said gate wiring strips are made of polycrystalline silicon.

3. A semiconductor integrated circuit device according to claim 1 or claim 2, in which said transistors form a read only memory.

4. A semiconductor integrated circuit device according to any one of the claims 1 to 3, further comprising a plurality of inverter circuits each including a driving insulated gate field effect transistor operating in the enhancement mode and a load insulated gate field effect transistor operating in the depletion mode and being connected in series with said driving transistor.

5. A semiconductor integrated circuit device constructed and arranged to operate substantially as herein described, with reference to and as illustrated in Figures 3 to 7, 8*a* and 9 of the accompanying drawings.

6. A method of manufacturing a semiconductor integrated circuit device including insulated gate field-effect transistors, comprising the steps of:

(a) forming an insulating layer on the surface of a semiconductor substrate of a first conductivity type, said insulating layer having alternating parallel relatively thin and relatively thick strip portions;

(b) selectively implanting ions of impurities of a second conductivity type, opposite said first conductivity type, into predetermined surface portions of said substrate beneath selected areas of the relatively thin strip portions of said insulating layer through said insulating layer to form channel regions of selected ones of said transistors;

(c) forming parallel gate wiring strips on said insulating layer, said gate wiring strips extending perpendicularly to said relatively thin and thick strip portions of the insulating layer so as to cross said predetermined surface portions and being spaced apart from each other;

(d) doping further impurities of said second conductivity type into the surface of said semiconductor substrate at both sides of each of said gate wiring strips by using said gate wiring strips as a mask to form semiconductor regions of said second conductivity type extending between the adjacent gate wiring strips in connection with portions of the device at which said gate wiring strips cross said relatively thin strip portions of the insulating layer; whereby ion-implanted said portions at which said gate wiring strips cross said relatively thin strip portions of the insulating layer serve as depletion type insulated gate field effect transistors while the other said portions at which the strips cross serve as enhancement type insulated gate field effect transistors.

7. A method of manufacturing a semiconductor integrated circuit device according to claim 6, in which the insulated gate field effect transistors form a read-only memory.

8. A method of manufacturing a semiconductor integrated circuit device, substantially as herein described, with reference to Figures 6 and 7 of the accompanying drawings.

9. A semiconductor integrated circuit device according to any one of the claims 1 to 5, when manufactured by a method according to claim 6, claim 7 or claim 8.

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