Claims

1. A method of forming an integrated circuit, comprising:

(i) forming at least a pair of optoelectronic devices from at least a first wafer material arranged on a semiconductor substrate, the first wafer material selected from a group III-V semiconductor material;

(ii) etching the first wafer material to form a first recess to be filled with a second material;

(iii) processing the second material to form a waveguide for coupling the pair of optoelectronic devices to define an optical interconnect thereby forming a photonic wafer; and

(iv) bonding at least one partially processed CMOS device layer having at least one transistor on the photonic wafer with the optical interconnect of the photonic wafer arranged below the at least one partially processed CMOS device layer to form the integrated circuit.

2. The method of claim 1, wherein the group III-V semiconductor material includes GaN, InGaP, GaAs, AlGaAs or InGaAs.

3. The method of claim 1 or claim 2, wherein the second material includes silicon nitride.

4. The method of any one of the preceding claims, wherein bonding the at least one partially processed CMOS device layer on the photonic wafer includes processing the at least one partially processed CMOS device layer to provide a second recess permitting access to the optical interconnect and filling the second recess with a first electrically insulating material; and processing the first electrically insulating material to electrically connect the at least one transistor and the pair of optoelectronic devices to form the integrated circuit.

5. The method of claim 4, wherein the first electrically insulating material includes silicon dioxide.

6. The method of any one of the preceding claims, wherein the pair of optoelectronic devices are selecting from the group consisting of photodetectors and light emitting devices.

7. The method of claim 6, wherein the light emitting devices include Light Emitting Diodes (LEDs) or Organic-LEDs.

8. The method of any one of the preceding claims, further comprising performing CMOS processing on a further semiconductor substrate to obtain the at least one partially processed CMOS device layer having the at least one transistor; and removing the at least one partially processed CMOS device layer from the further semiconductor substrate.

9. The method of claim 8, wherein the further semiconductor substrate includes a silicon-on-insulator substrate.

10. The method of any one of the preceding claims, further comprising:

depositing a second electrically insulating material to cover the first wafer material subsequent to forming the pair of optoelectronic devices; and

planarizing the second electrically insulating material using Chemical Mechanical Polishing.

11. The method of any one of the preceding claims, further comprising:

planarizing the first recess filled with the second material using Chemical Mechanical Polishing, subsequent to the first recess being filled with the second material.

12. The method of any one of the preceding claims, wherein processing the second material to form the waveguide includes using lithography and/or etching.

13. The method of any one of the preceding claims, further comprising:

depositing a third electrically insulating material to cover the first wafer material and the second material subsequent to forming the waveguide; and

planarizing the third electrically insulating material using Chemical Mechanical Polishing.

14. The method of claim 4, wherein processing the at least one partially processed CMOS device layer to provide the second recess includes using etching and/or mechanical grinding.

15. The method of claim 4, further comprising:

planarizing the at least one partially processed CMOS device layer and the second recess filled with the first electrically insulating material using Chemical Mechanical Polishing.

16. The method of claim 4, wherein processing the first electrically insulating material to electrically connect the at least one transistor and the pair of optoelectronic devices includes forming a plurality of vias in the first electrically insulating material and filling the vias with an electrically conducting material.

17. The method of any one of the preceding claims, wherein the first wafer material includes a plurality of layers of wafer materials, each layer formed of a different material.

18. An integrated circuit comprising:

at least one transistor arranged in a partially processed CMOS device layer; and

a photonic wafer being bonded to the partially processed CMOS device layer, the photonic wafer comprising at least a pair of optoelectronic devices adapted to be coupled by a waveguide to define an optical interconnect on a semiconductor substrate, the optical interconnect being arranged below the partially processed CMOS device layer and is formed prior to the photonic wafer being bonded to the CMOS device layer,

wherein the pair of optoelectronic devices are configured to be electrically connected to the at least one transistor, and the pair of optoelectronic devices are formed from at least a first wafer material selected from a group III-V semiconductor material, and

wherein the waveguide is formed from a second material deposited in a first recess formed in the first wafer material.

19. The integrated circuit of claim 18, wherein the group III-V semiconductor material includes GaN, InGaP, GaAs, AlGaAs or InGaAs.

20. The integrated circuit of claim 18 or claim 19, wherein the integrated circuit is formed as a single processor or a portion of a processor.

21. The method of any one of claims 18 to 20, wherein the second material includes silicon nitride.