the processor 544 to the slave clock 550 to adjust the clock frequency and phase to match the RF clock signal in the RF signal.

[0076] Figure 12 illustrates a clock generation circuit in an impedance matching system coupled to an RF generator in alternate embodiments of the present disclosure. Referring to Figure 12, an impedance matching system 604 is coupled to an RF generator 602 in an RF system to receive an RF signal 35 and to provide an impedance matched RF signals 664a, 664b to a load 680. The impedance matching system 604 includes an input impedance sensor 642, an impedance match network 660 and an output impedance sensor 662 providing the impedance matched RF signal 664. In the present embodiment, the impedance matching system 604 includes two output impedance sensor 1 and 2 662a, 662b to provide two output RF signals 664a, 664b, respectively.

[0077] In the RF system of Figure 12, the master clock, or the reference clock, of the RF generator 602 is shared with the impedance matching system ~~640~~604. Furthermore, the sample index generated in the RF generator 602 is also shared with the impedance matching system ~~640~~604. For example, the master clock 90 of the RF generator 602 may be shared with the impedance matching system 604, such as by coupling the master clock 90 to a phase-locked loop 646. The sample index generated by the index generator processor 610 are provided to the match system processor 670. By using the same clock and the same sample index, the impedance matching system 604 can process the sensor data within the matching system with greater efficiency.

[0078] More specifically, the phase-locked loop 646 drives an oscillator 650 in response to the master clock 90 being shared by the RF generator 602. The oscillator 650 provides an output clock signal to a clock generator 644 which, in the present embodiment, generates the sampling signals for the input impedance sensor 642 and the two output impedance sensors 662a, 662b. With the same clock signal and the same sample index, the input impedance sensors 642 and the output impedance sensors 664a, 664b can run at the same timing as the RF generator 602. In practice, there will be a certain amount of clock delay but the delay can be compensated.

[0079] In general, the clock synchronization scheme of Figure 12 is implemented by sharing the clock signal and index data between two independent systems, and having the sample

CLAIMS

1. A radio frequency generator, comprising:

a radio frequency (RF) circuit comprising an RF source providing an RF signal of a first frequency derived from a first clock and a signal modulator generating a pulsed radio frequency (RF) signal having an On period where the RF signal is provided at an output terminal and an Off period where no RF signal is provided; and

an automatic level control circuit configured to sample the pulsed RF signal at the output terminal and to generate a control signal to modulate the RF signal at the radio frequency circuit, the automatic level control circuit comprising:

first and second analog-to-digital converters configured to sample respective forward RF signal and reflected RF signal at the output terminal at a sampling frequency and to generate digital samples of the respective forward and reflected RF signals, the sampling frequency being derived from a sampling clock synchronized to the first clock and being less than the first frequency of the RF signal;

a gated accumulation circuit configured to receive respective digital samples of the forward and reflected RF signals and selecting digital samples based on a sample index identifying the digital samples;

a digital signal processor configured to process the selected digital samples to generate a measured signal level value;

an error processor configured to compare the measured signal level value to a reference signal level to generate an error signal indicative of a difference thereof; and

a modulator controller configured to generate the control signal in response to the error signal and a pulse modulation signal, the pulse modulation signal indicating the On period and Off period of the pulsed RF signal, the control signal being coupled to the modulator of the radio frequency circuit to modulate the RF signal to generate the pulsed RF signal and to control a signal level of the pulsed RF signal during the On period.

2. The radio frequency generator of claim 1, wherein the sample index is related to the sampling frequency and identifies the digital samples as a first number of data points sampled within a given conversion.

3. The radio frequency generator of claim 2, where the gated accumulation circuit selects the digital samples of the forward RF signal and the reflected RF signal during the On period of the pulsed RF signal based on the sample index.

4. The radio frequency generator of claim 2, where the sample index identifies the digital samples as four data points sampled within a given conversion.

5. The radio frequency generator of claim 1, further comprising:

a digital-to-analog convert configured to convert the control signal to an analog signal and to couple the analog signal to control the signal modulator of the radio frequency circuit.

6. The radio frequency generator of claim 1, wherein the digital signal processor comprises:

a digital filter configured to process the selected digital samples and to generate a first parameter value associated with the forward RF signal and a second parameter value associated with the reflected RF signal, each of the first and second parameter values being indicative of a level value and a phase value of the respective forward or reflected RF signal measured by the selected digital samples; and

an impedance and level processor configured to process the first parameter value and the second parameter value to generate the measured signal level value.

7. The radio frequency generator of claim 1, further comprising:

a simulated attenuation processor configured to generate an estimated signal level value and to provide the estimated signal level value to the error processor during the Off period where no digital sample of the RF signal is selected by the gated accumulation circuit, the estimated signal level value being provided to the error processor as the measured signal level,

wherein the simulated attenuation processor generates the estimated signal level value based on the error signal and parameters of the radio frequency circuit.

8. The radio frequency generator of claim 1, wherein the pulsed RF signal comprises a multi-level pulsed RF signal having a first signal level during a first On period and a second signal level during a second On period, the first signal level being different from the second level.

9. The radio frequency generator of claim 8, wherein the sample index comprises a first sample index identifying the digital samples as the first number of data points and a second sample index identifying the signal level of the pulsed RF signal, the second sample index having a first logical value indicating the first signal level and a second logical value indicating the second signal level.

10. The radio frequency generator of claim 9, wherein the automatic level control circuit further comprises:

a first signal processing path for processing digital samples having the first signal level identified by the second sample index;

a second signal processing path for processing digital samples having the second signal level identified by the second sample index, wherein each of the first and second signal processing path comprises the gated accumulation circuit, the digital signal processor and the error processor, the first signal processing path generating a first error signal indicative of a difference between the first signal level and a first reference signal level and the second signal processing path generating a second error signal indicative of a difference between the second signal level and a second reference signal level; and

a data selector configured to select one of the first and second error signals and provide the selected error signal to the modulator controller, wherein the modulator controller generates the control signal in response to the selected error signal to control the signal level of the pulsed RF signal during an On period of the pulsed RF signal having a signal level associated with the selected error signal.

11. The radio frequency generator of claim 10, wherein each of the first and second signal processing path further comprises:

a simulated attenuation processor configured to generate an estimated signal level value and to provide the estimated signal level value to the error processor in each signal processing path during the Off period where no digital sample of the RF signal is selected by the gated accumulation circuit, the estimated signal level value being provided to the error processor as the measured signal level, wherein the simulated attenuation processor generates the estimated signal level value based on the respective error signal and parameters of the radio frequency circuit.

12. The radio frequency generator of claim 1, further comprising:

an index generator configured to generate the sample index in response to the pulse modulation signal and the sampling frequency.

13. The radio frequency generator of claim 1, further comprising:

first and second directional couplers coupled to the output terminal to sample the respective forward RF signal and reflected RF signal and to provide the sampled signals to the respective first and second analog-to-digital converters.

14. A method of controlling a signal level of a radio frequency (RF) signal, comprising:

generating the RF signal of a first frequency derived from a first clock;

generating a pulsed RF signal having an On period where the RF signal is provided and an Off period where no RF signal is provided;

sampling, at a sampling frequency, a forward RF signal and a reflected RF signal relating to the pulsed RF signal to generate digital samples of the forward RF signal and the reflected RF signal, the sampling frequency being derived from a sampling clock synchronized to the first clock and being less than the first frequency of the RF signal;

selecting digital samples of the forward and reflected RF signals based on a sample index identifying the digital samples;

processing the selected digital samples to generate a measured signal level value;

determining an error signal indicative of a difference between the measured signal level value and a reference signal level;

generating a control signal in response to the error signal and a pulse modulation signal, the pulse modulation signal indicating the On period and Off period of the pulsed RF signal; and

applying the control signal to modulate the RF signal to generate the pulsed RF signal and to control a signal level of the pulsed RF signal during the On period.

15. The method of claim 14, further comprising wherein the sample index is related to the sampling frequency and identifies the digital samples as a first number of data points sampled within a given conversion.

16. The method of claim 14, wherein selecting digital samples of the forward and reflected RF signals based on a sample index identifying the digital samples comprises:

selecting digital samples of the forward and reflected RF signals during the On period of the pulsed RF signal based on the sample index.

17. The method of claim 14, further comprising:

generating an estimated signal level value and providing the estimated signal level value as the measured signal level value for determining the error signal, the estimated signal level value being based on the error signal and parameters associated with generating the RF signal.

18. The method of claim 14, wherein the pulsed RF signal comprises a multi-level pulsed RF signal having a first signal level during a first On period and a second signal level during a second On period, the first signal level being different from the second level; and wherein the sample index comprises a first sample index identifying the digital samples as the first number of data points and a second sample index identifying the signal level of the pulsed RF signal, the second sample index having a first logical value indicating the first signal level and a second logical value indicating the second signal level.

19. The method of claim 18, further comprising:

processing digital samples having the first signal level identified by the second sample index;

generating a first error signal indicative of a difference between the first signal level and a first reference signal level;

processing digital samples having the second signal level identified by the second sample index;

generating a second error signal indicative of a difference between the second signal level and a second reference signal level;

selecting one of the first and second error signals as the error signal to generate the control signal; and

generating the control signal in response to the selected error signal to control the signal level of the pulsed RF signal during an On period of the pulsed RF signal having a signal level associated with the selected error signal.

20. The method of claim 14, further comprising:

generating the sample index in response to the pulse modulation signal and the sampling frequency.

~~21. A clock generation circuit to generate a local clock synchronized to a radio frequency (RF) signal of a first frequency derived from a first clock, the clock generation circuit comprising:~~

~~an impedance measurement circuit configured to measure a load impedance value associated with a load to which the RF signal is applied;~~

~~a processor receiving the RF signal and the local clock and receiving a signal indicative of the load impedance value, the processor generating a phase synchronization signal in response to the load impedance value and further generating a frequency and phase adjust signal;~~

~~an oscillator generating a slave clock in response to the frequency and phase adjust signal;~~

a frequency generator receiving the slave clock and generating a second clock in response to the slave clock and the phase synchronization signal; and

a phase frequency detector measuring a phase difference between the RF signal and the second clock and generating the local clock in response to the phase difference,

wherein the processor is configured to determine a time period when the load impedance value indicates a resistive load and generates the phase synchronization signal to synchronize the local clock to the first clock of the RF signal.

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22. The clock generation circuit of claim 21, wherein the processor is configured to disable synchronization of the local clock during a time period when the signal indicative of the load impedance indicates a capacitive or inductive load.

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23. The clock generation circuit of claim 21, wherein the frequency generator comprises a phase-locked loop.