

**ABSTRACT****METHOD AND APPARATUS FOR ENHANCED TIMING LOOP
FOR A PRML DATA CHANNEL**

Methods and apparatus for an enhanced timing loop are provided for a partial-response maximum-likelihood (PRML) data channel (100) in a direct access storage device (DASD). An acquisition timing circuit (500) for generating an acquisition timing signal includes a plurality of compare functions (508,510,512) for receiving and comparing consecutive input signal samples on an interleave with a threshold value. Tracking timing circuitry (600) for generating a timing error signal during a read operation includes a channel data detector (108). The tracking timing circuit includes a low latency detector receiving disk signal input samples. A selector function (610) is coupled to an output of the low latency detector and is coupled to the multiple-state path memory (606) for selecting a state. The selector function (610) provides a low latency output corresponding to the selected state. The low latency output is used for generating the timing error signal during a read operation.

(Fig. 1)