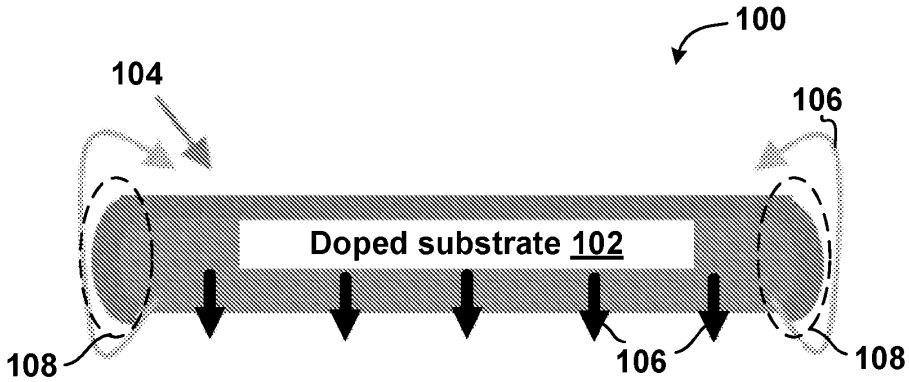

100
104
106
Doped substrate 102
108
106
108

FIG. 1A

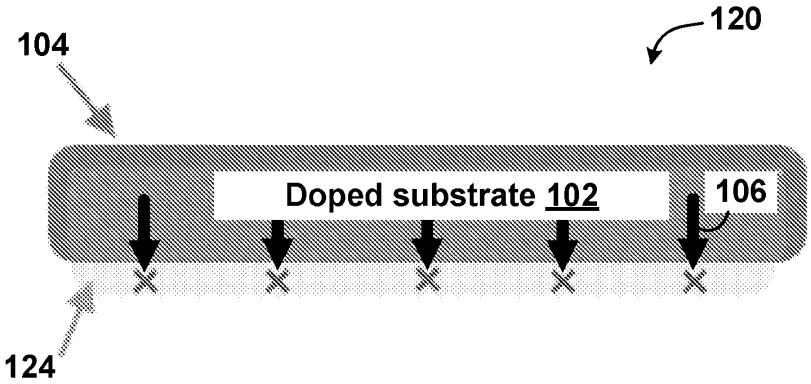

120
104
Doped substrate 102
106
124

FIG. 1B

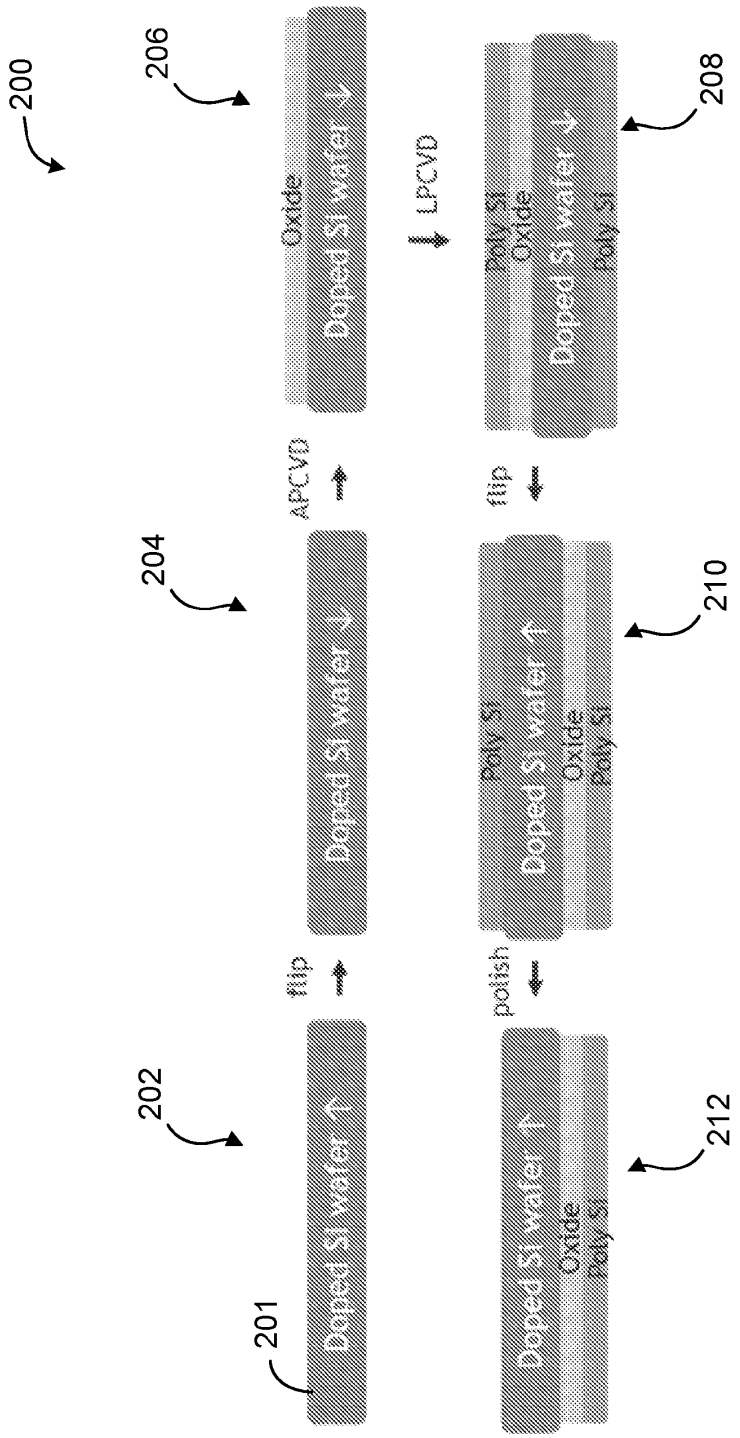

200
206
208
Oxide
Doped Si wafer V
LPCVD
Poly Si
Oxide
Doped Si wafer V
Poly Si
APCVD
flip
204
210
Doped Si wafer V
Poly Si
Doped Si wafer P
Oxide
Poly Si
flip
polish
202
212
201
Doped Si wafer P
Doped Si wafer P
Oxide
Poly Si

FIG. 2

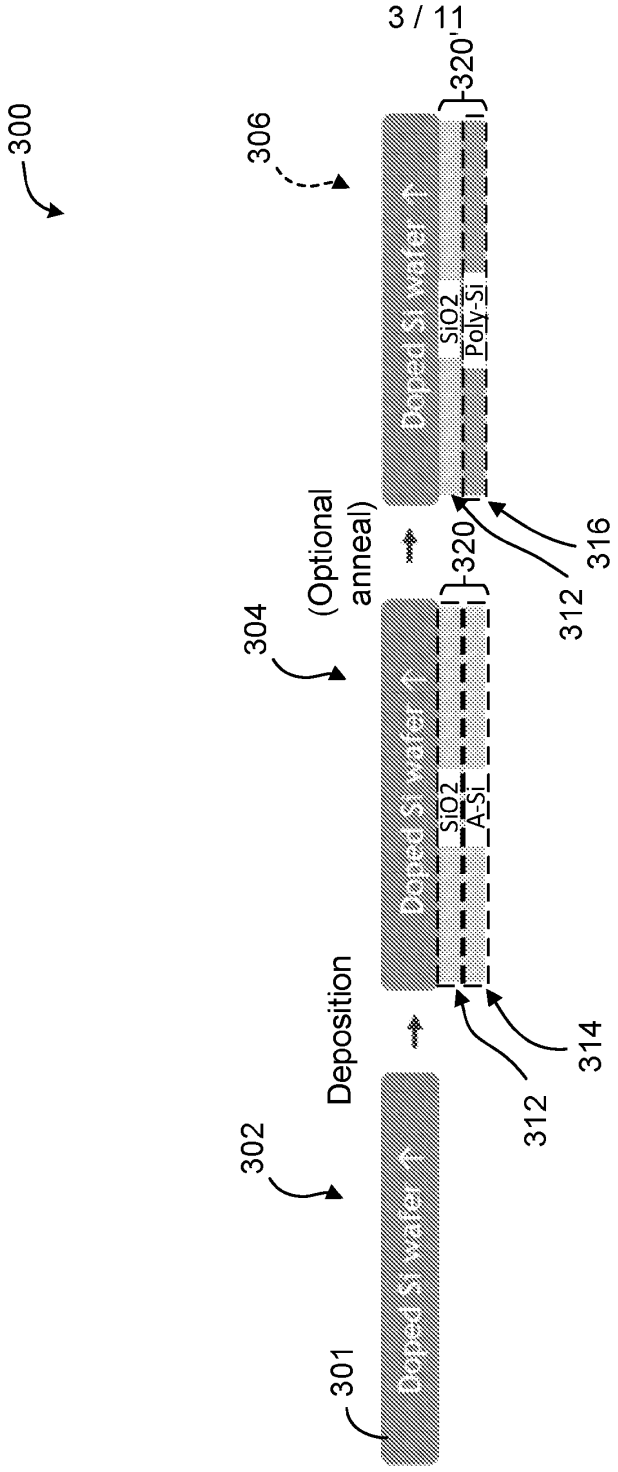

300
306
320'
Doped Si Wafer /n
SiO2
Poly-Si
(Optional anneal)
304
320
316
312
Doped Si Wafer /n
SiO2
A-Si
Deposition
314
312
302
Doped Si Wafer /n
301

FIG. 3

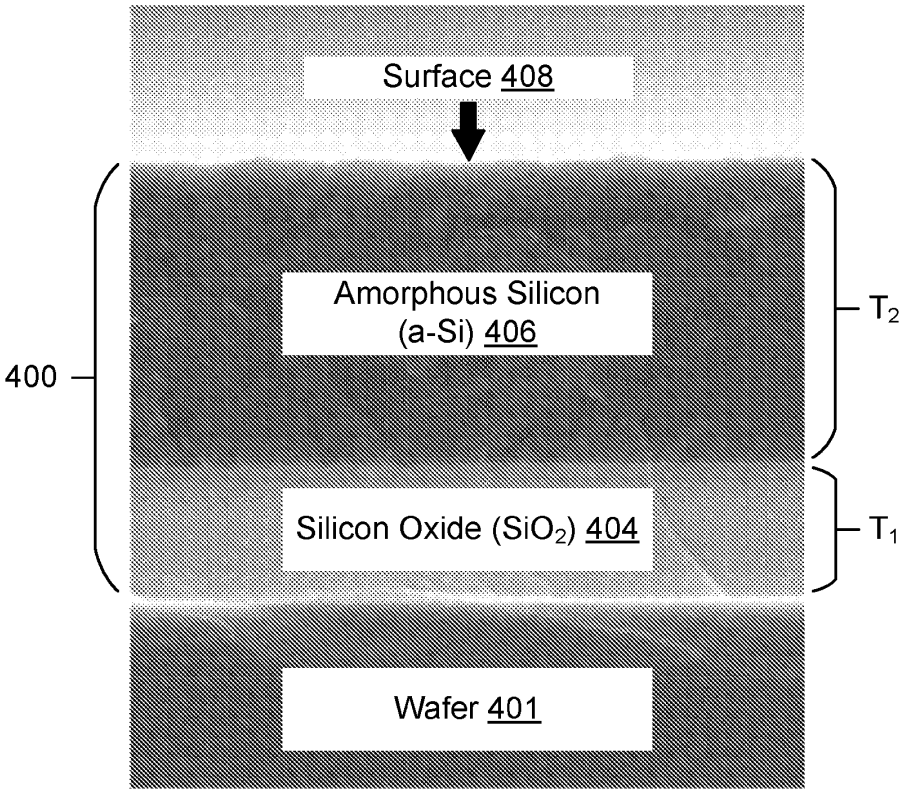

Surface 408
Amorphous Silicon
(a-Si) 406
Silicon Oxide (SiO_2) 404
Wafer 401
400
T_2
T_1

FIG. 4

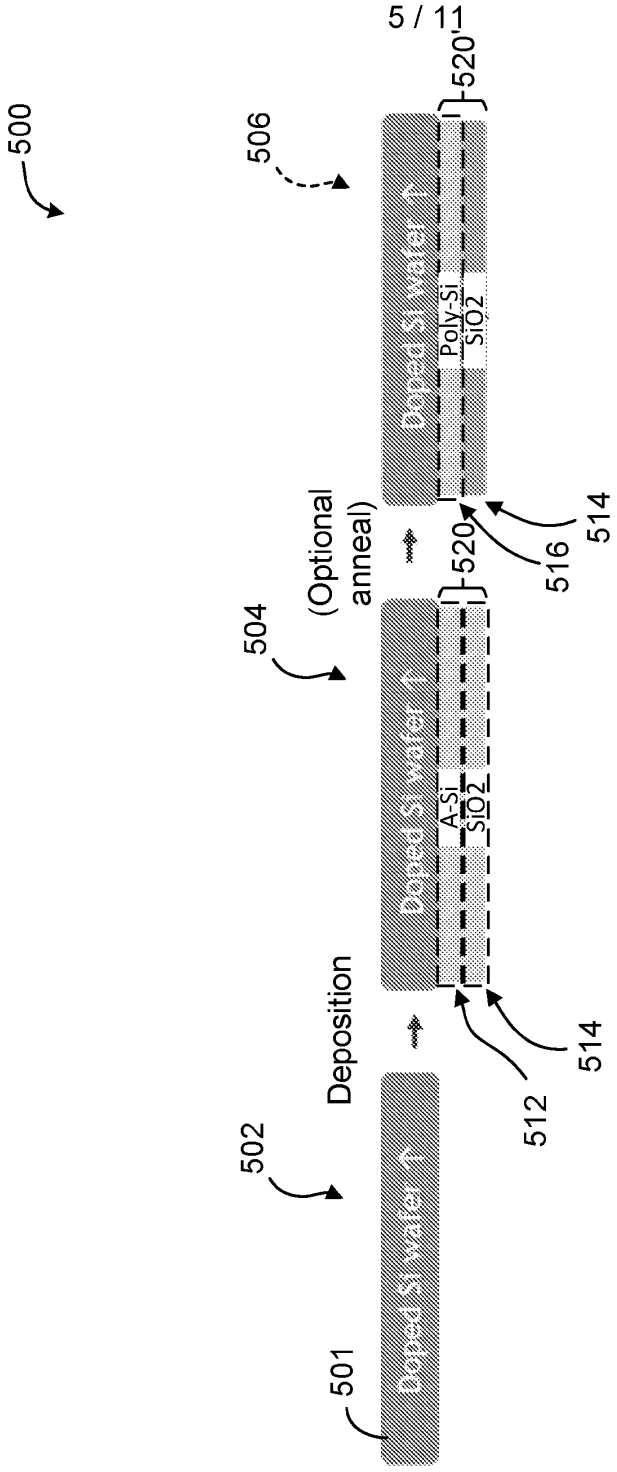

500
506
520'
Doped Si Wafer /P
Poly-Si
SiO2
(Optional anneal)
504
520
516
514
Doped Si Wafer /P
A-Si
SiO2
Deposition
502
512
514
501
Doped Si Wafer /P

FIG. 5

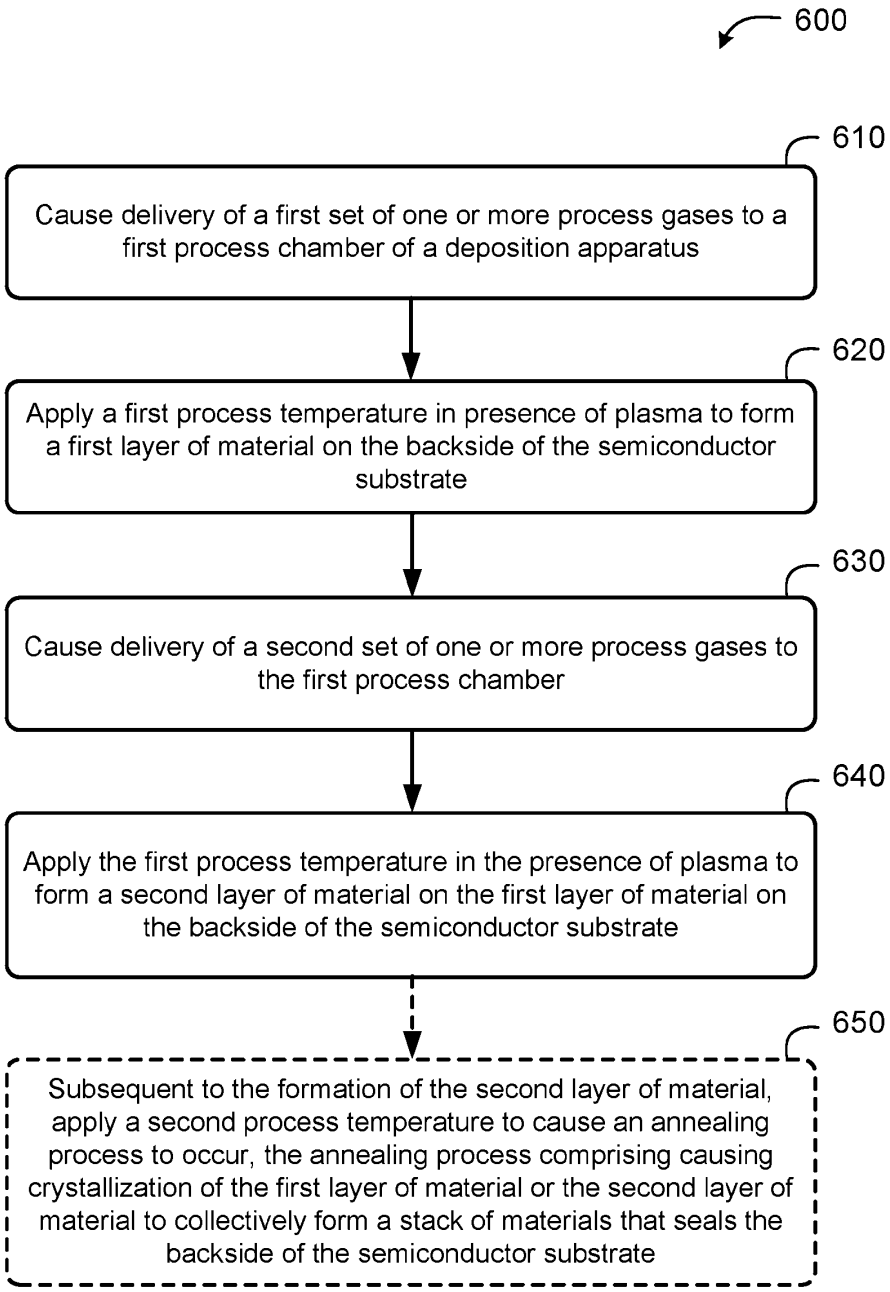

600
610
Cause delivery of a first set of one or more process gases to a first process chamber of a deposition apparatus
620
Apply a first process temperature in presence of plasma to form a first layer of material on the backside of the semiconductor substrate
630
Cause delivery of a second set of one or more process gases to the first process chamber
640
Apply the first process temperature in the presence of plasma to form a second layer of material on the first layer of material on the backside of the semiconductor substrate
650
Subsequent to the formation of the second layer of material, apply a second process temperature to cause an annealing process to occur, the annealing process comprising causing crystallization of the first layer of material or the second layer of material to collectively form a stack of materials that seals the backside of the semiconductor substrate

FIG. 6

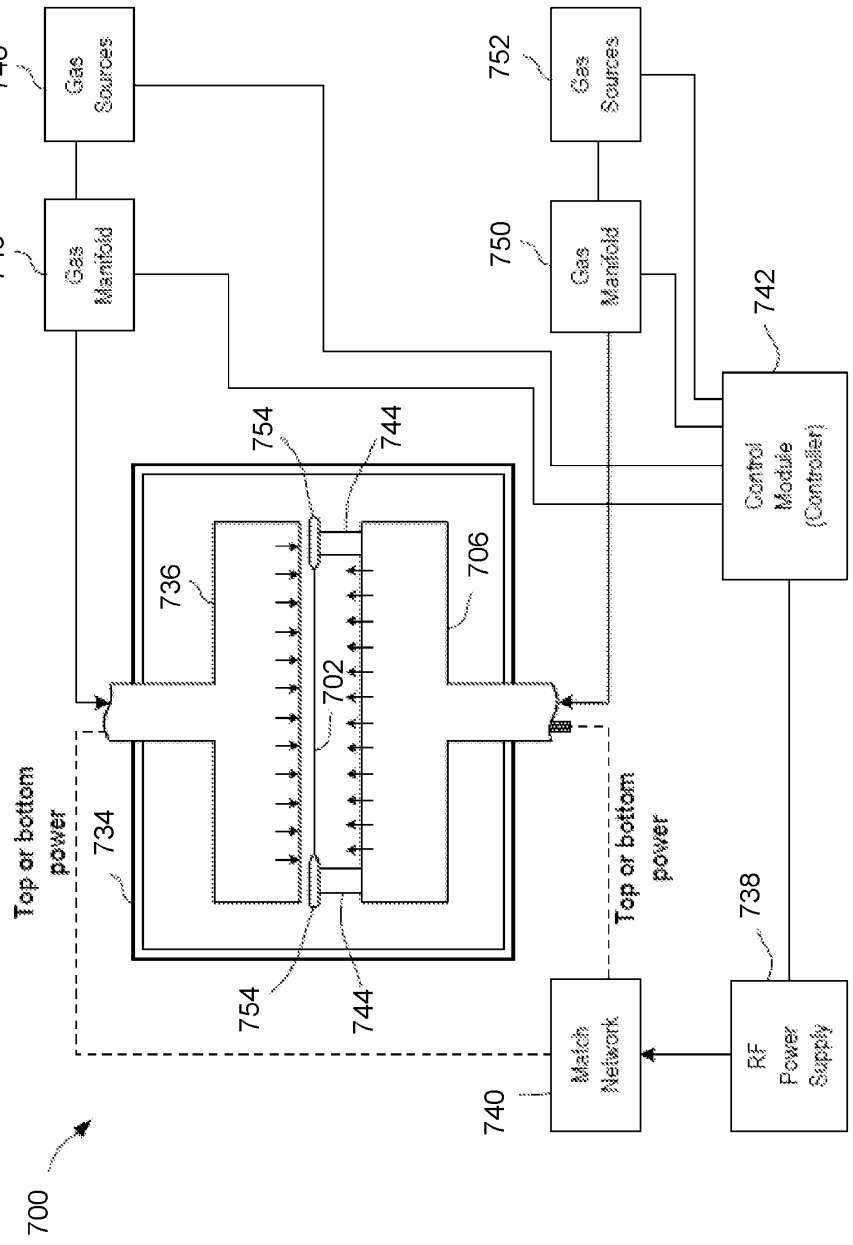

748
Gas Sources
746
Gas Manifold
752
Gas Sources
750
Gas Manifold
742
Control Module (Controller)
754
744
736
706
702
734
Top or bottom power
Top or bottom power
738
754
744
Match Network
740
RF Power Supply
700

FIG. 7

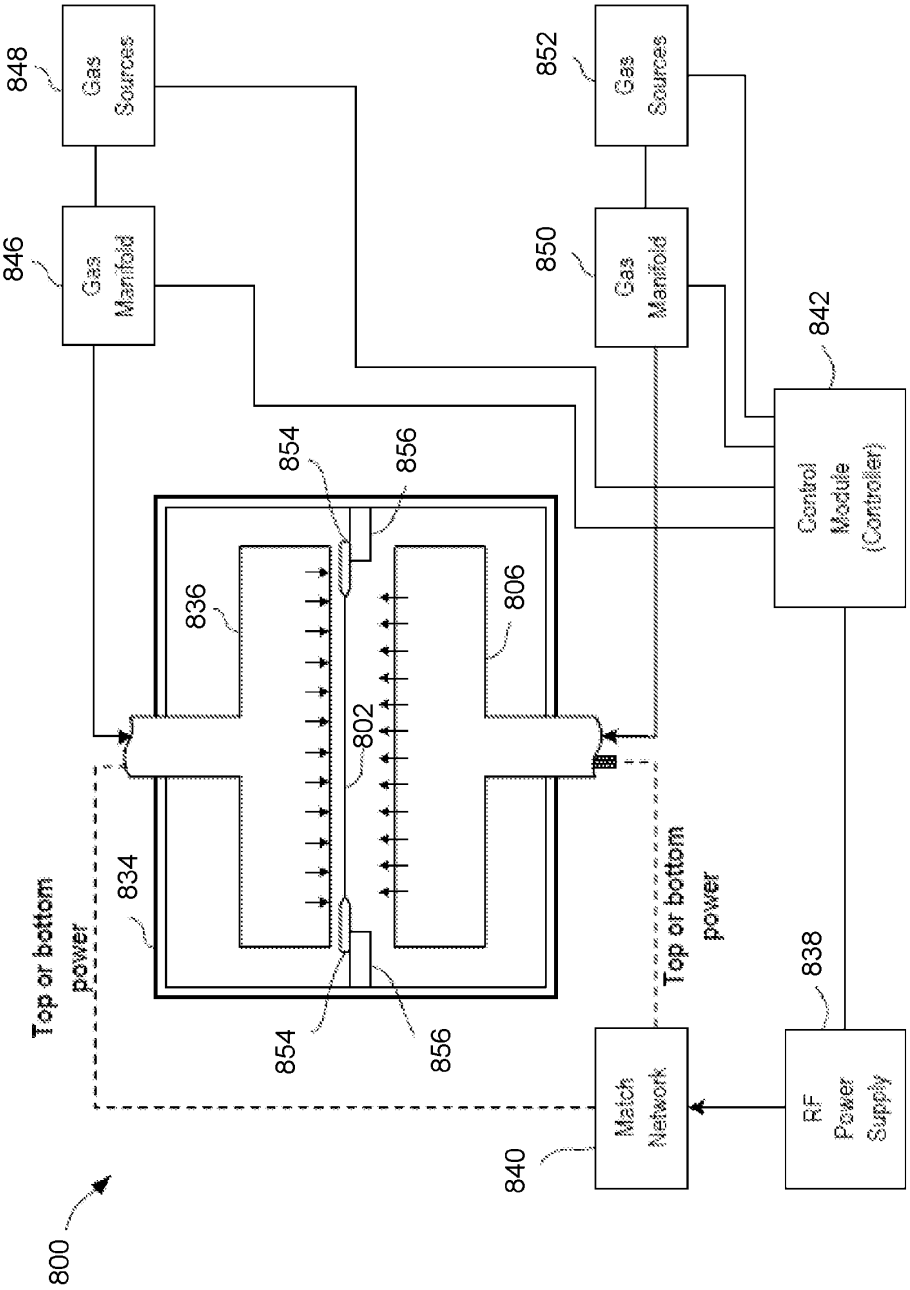

848
Gas Sources
846
Gas Manifold
852
Gas Sources
850
Gas Manifold
842
Control Module (Controller)
854
856
836
806
802
834
Top or bottom power
Top or bottom power
838
RF Power Supply
840
Match Network
800

FIG. 8

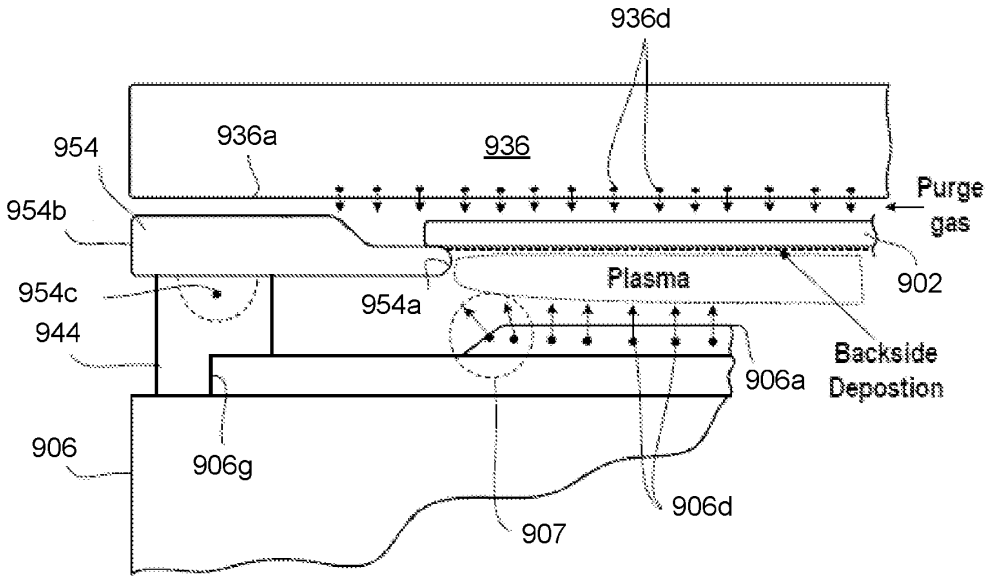

936d
936a
936
954
954b
Purge gas
954c
954a
Plasma
902
944
Backside Depostion
906a
906
906g
906d
907

FIG. 9A

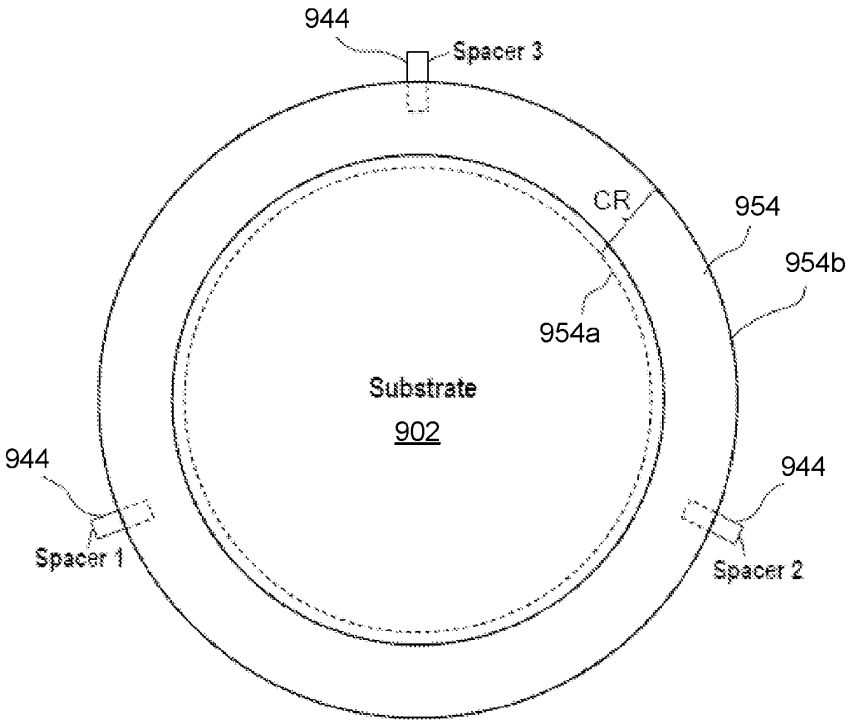

944
Spacer 3
CR
954
954b
954a
Substrate
902
944
Spacer 1
944
Spacer 2

FIG. 9B

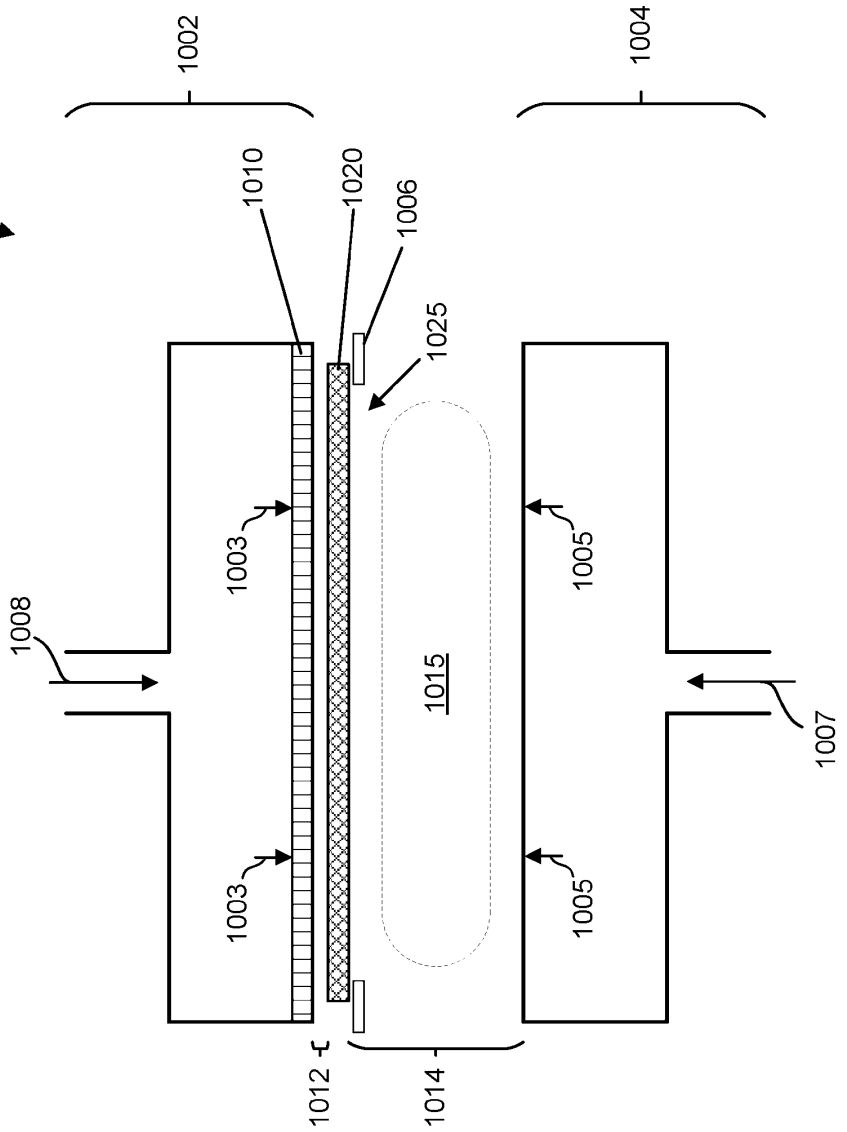

1000
1002
1004
1010
1020
1006
1025
1003
1003
1005
1005
1008
1015
1007
1012
1014

FIG. 10

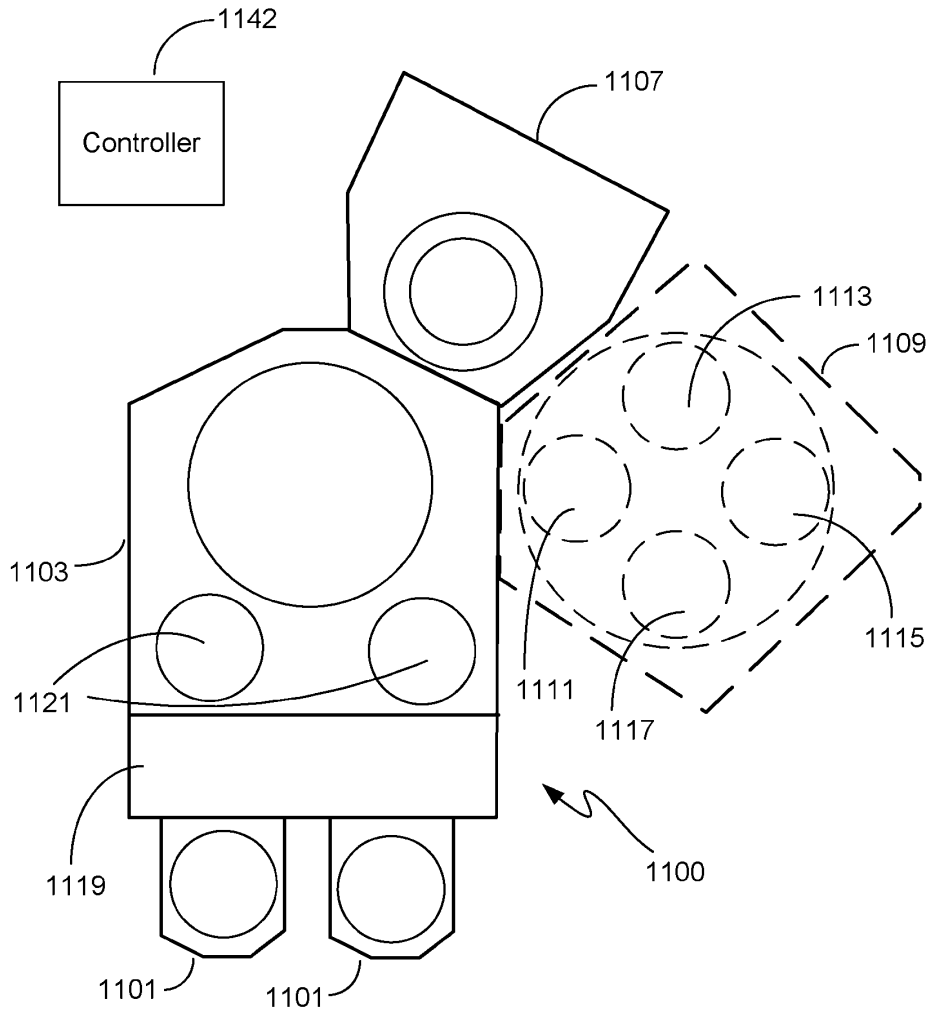

1142
Controller
1107
1113
1109
1103
1121
1111
1117
1115
1119
1100
1101
1101

FIG. 11