ABSTRACT

STABLE STRESS DIELECTRIC LAYER

An integrated circuit is provided having a substrate and a transistor in an active region of the substrate. The substrate also has an isolation region having a dielectric material. In one embodiment, a pre-metal dielectric (PMD) layer is disposed over the substrate and the transistor. At least one of the isolation region or the PMD layer includes O_3-TEOS having a first stress. A cap layer is disposed over the O_3-TEOS in the isolation region or the PMD layer. The cap layer prevents degradation of the first stress of the O_3-TEOS.

Fig. 1