ABSTRACT

A memory device may include: a control circuit suitable for performing a program loop including a program operation including a program voltage application operation on a selected word line and a bit line setup operation on a plurality of bit lines and a verification operation of applying (N-1) first verification voltages to the selected word line according to a predetermined order to check N types of first program states for each of a plurality of memory cells included in the selected word line; and control logic suitable for controlling the control circuit to repeatedly perform the program loop until programming for the selected word line is completed, and controlling the control circuit to apply any one of N types of column voltages to each of the plurality of bit lines in the bit line setup operation included in a second program loop.

FIG. 4