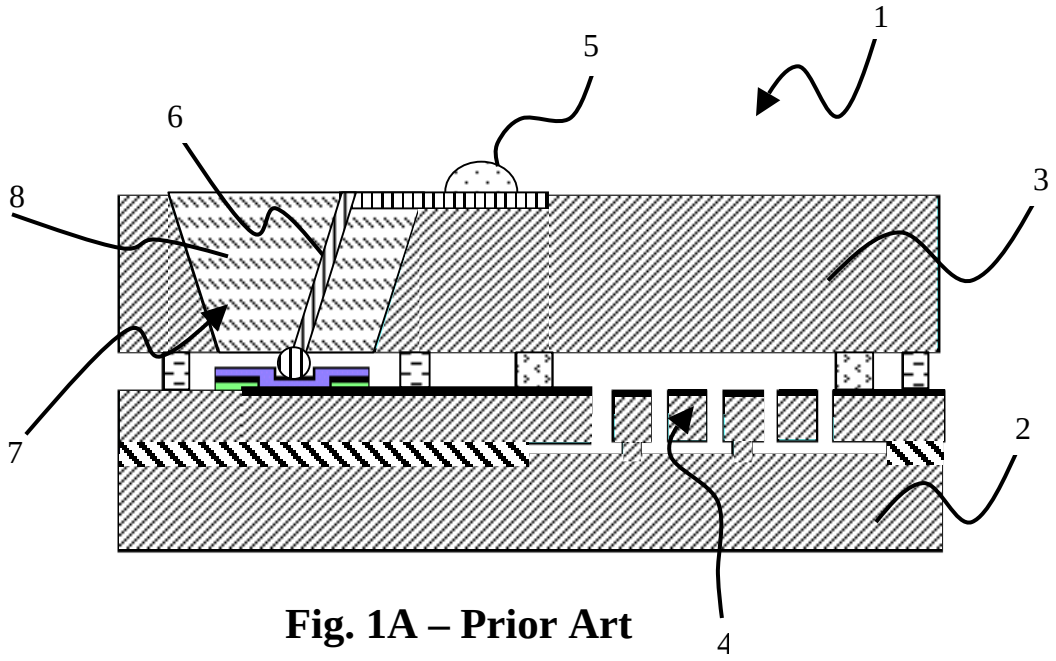


Fig. 1A – Prior Art

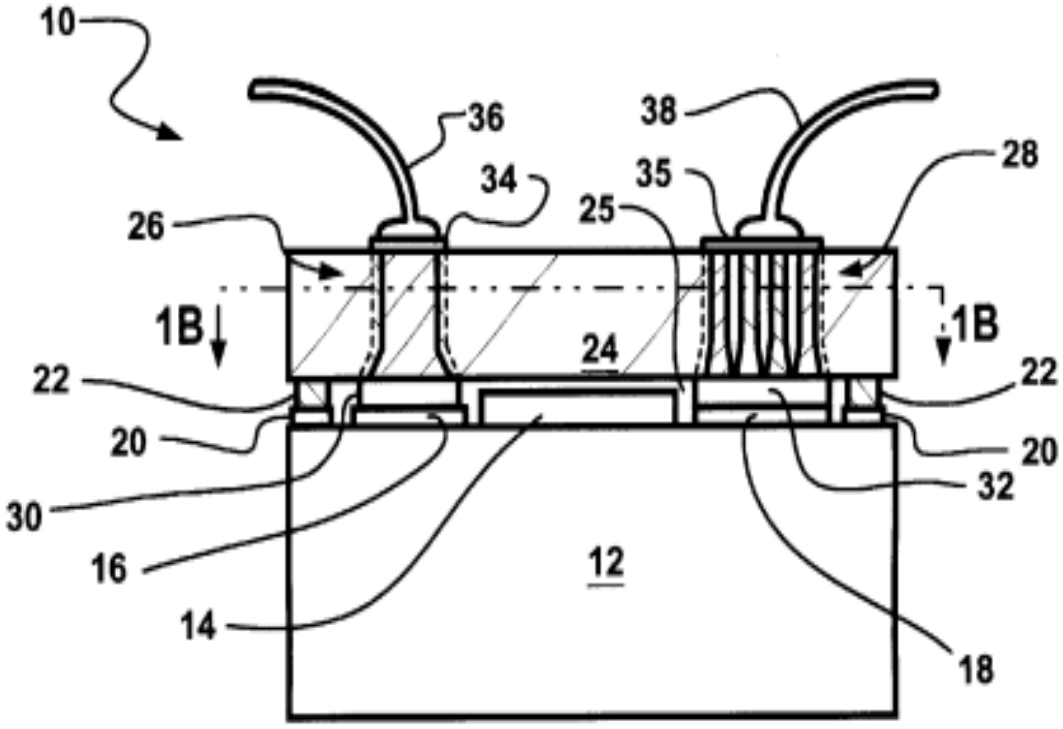


Fig. 1B – Prior Art

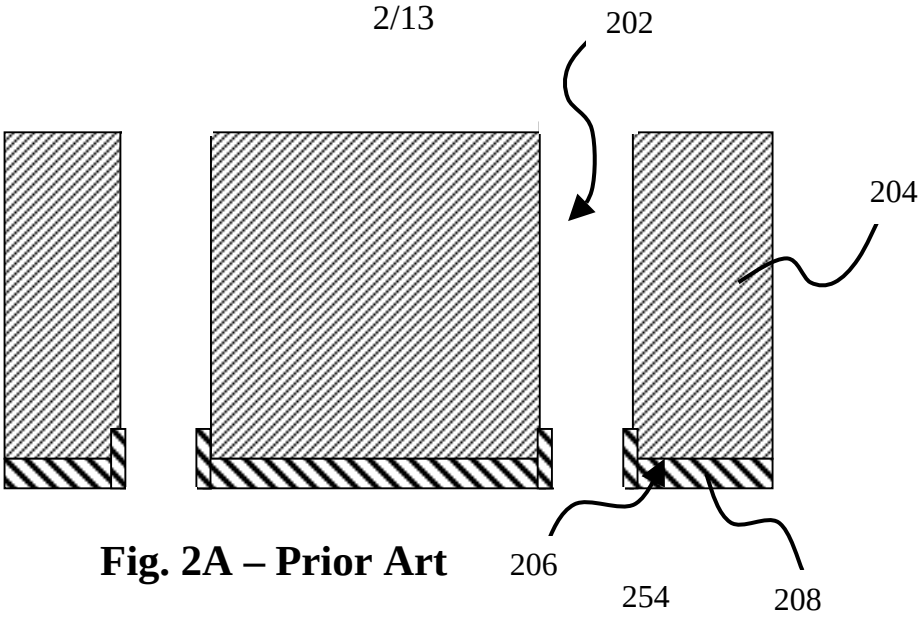


Fig. 2A – Prior Art

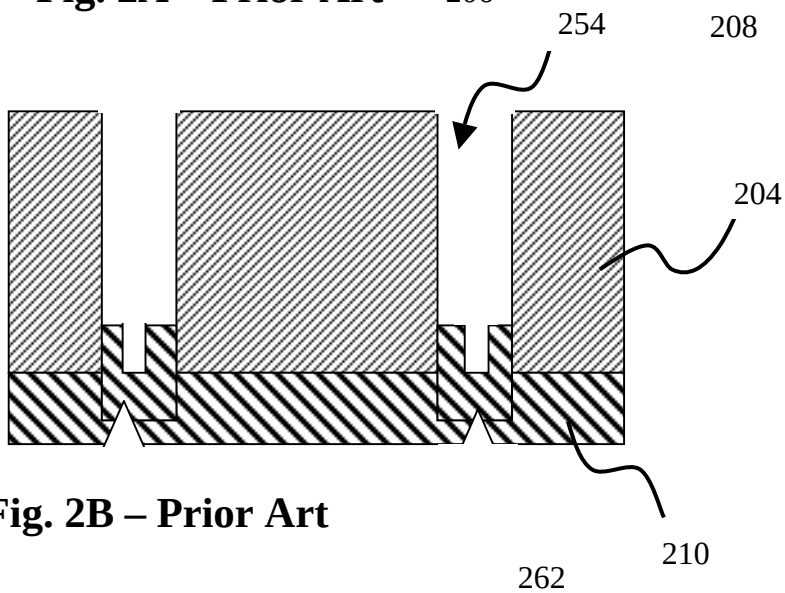


Fig. 2B – Prior Art

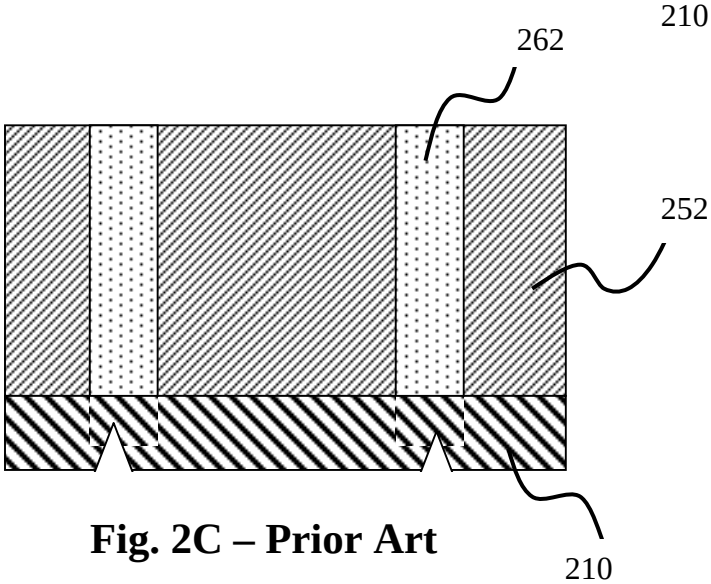


Fig. 2C – Prior Art

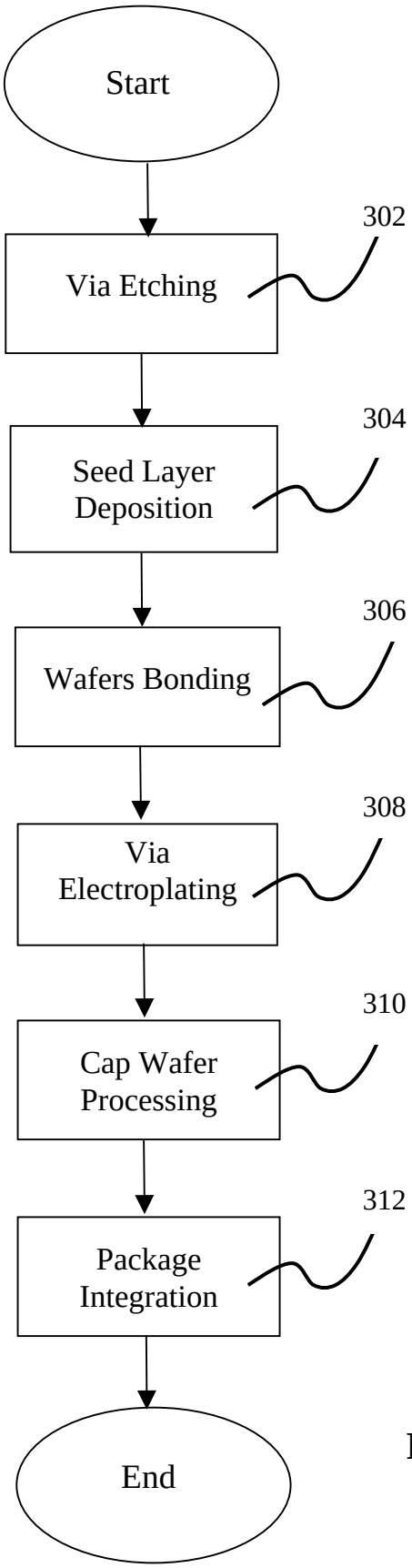

Start
302
Via Etching
304
Seed Layer Deposition
306
Wafers Bonding
308
Via Electroplating
310
Cap Wafer Processing
312
Package Integration
End

Fig. 3A

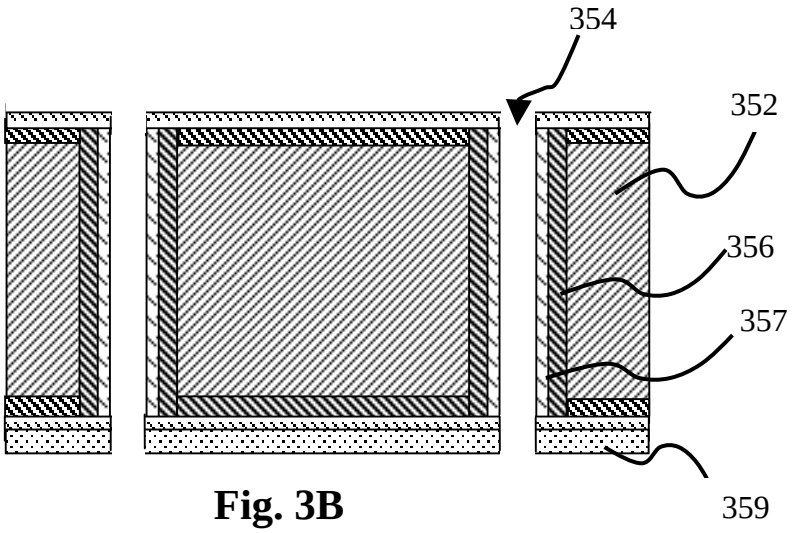


Fig. 3B

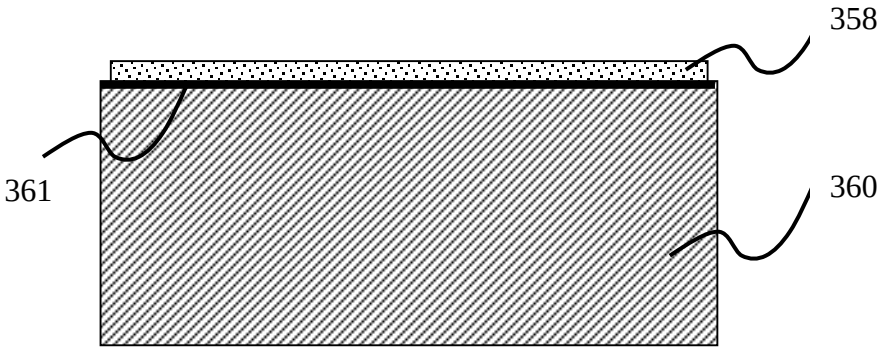


Fig. 3C

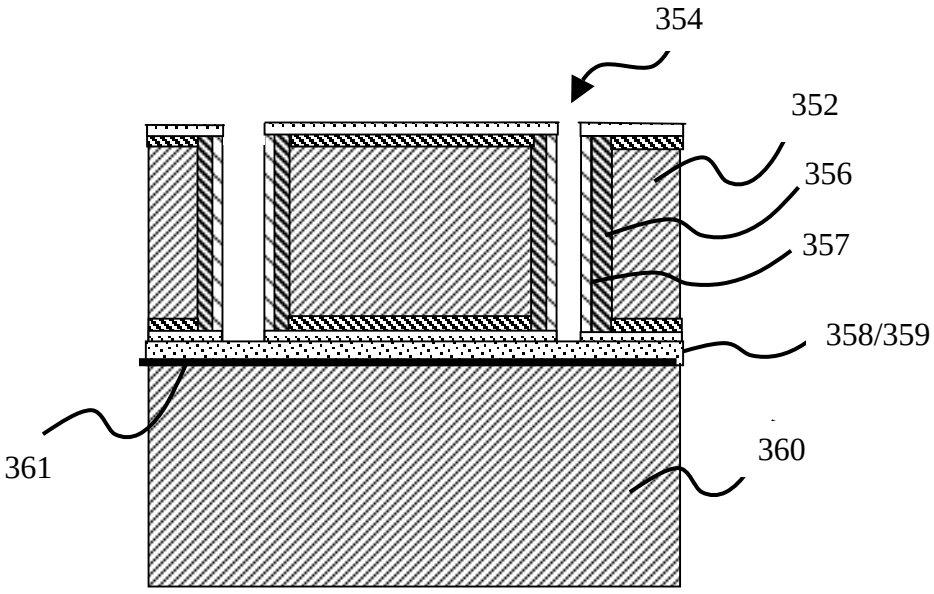


Fig. 3D

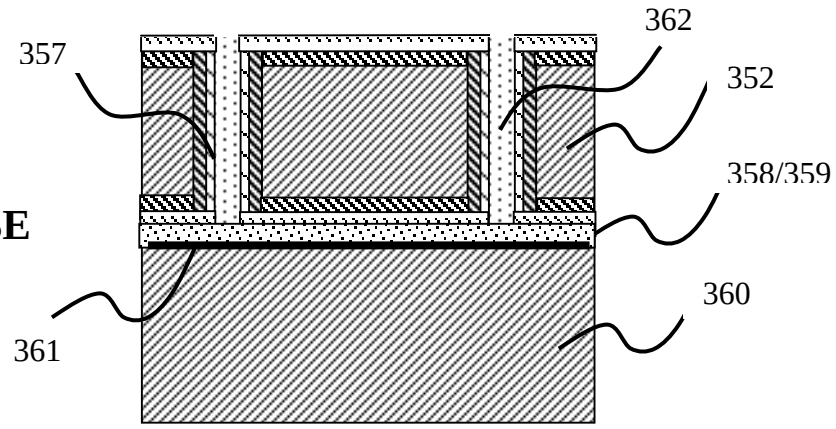


Fig. 3E

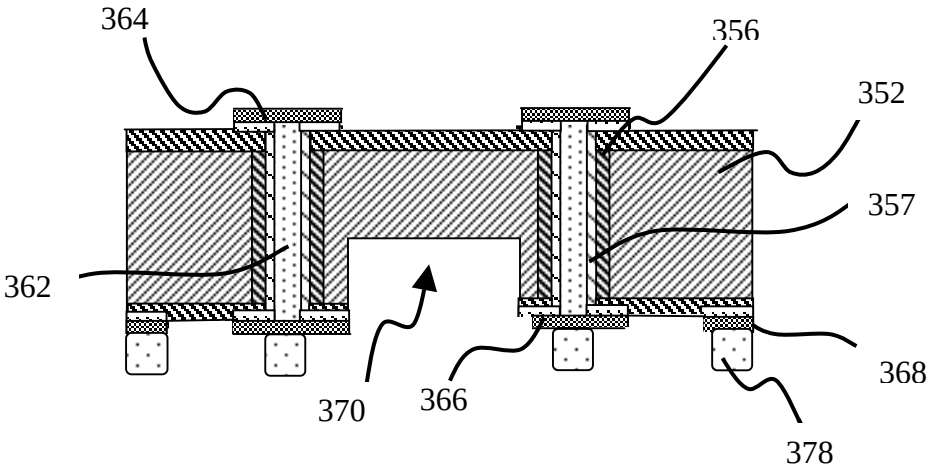


Fig. 3F

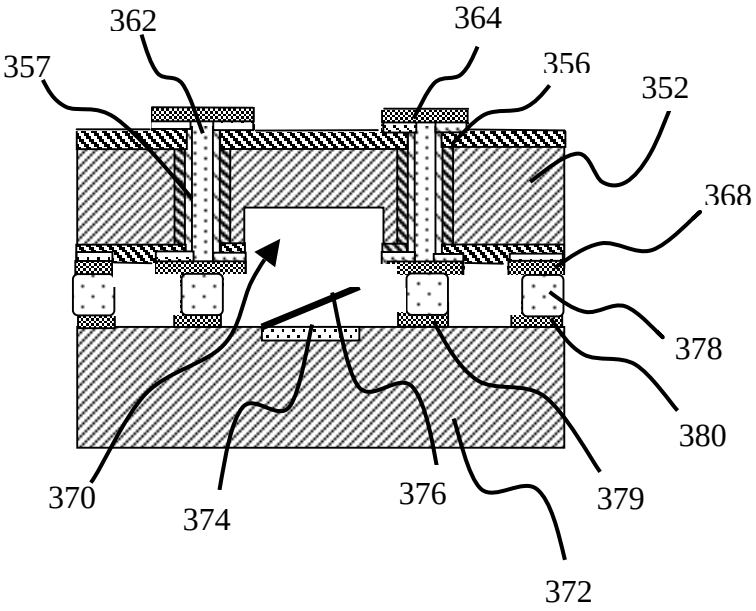


Fig. 3G

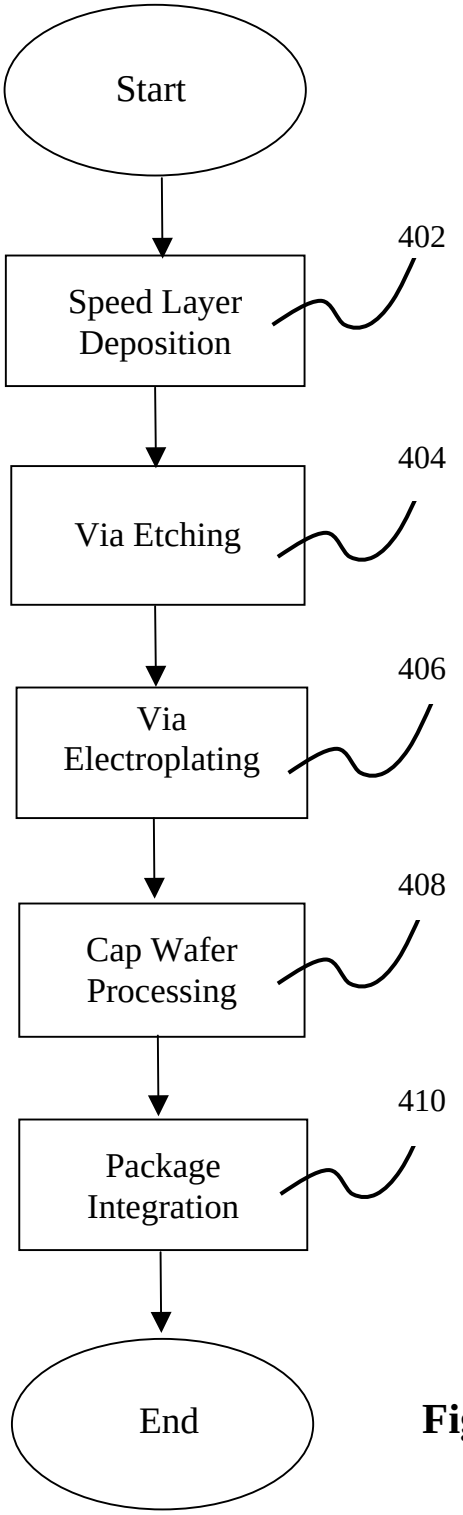

Start
402
Speed Layer Deposition
404
Via Etching
406
Via Electroplating
408
Cap Wafer Processing
410
Package Integration
End

Fig. 4A

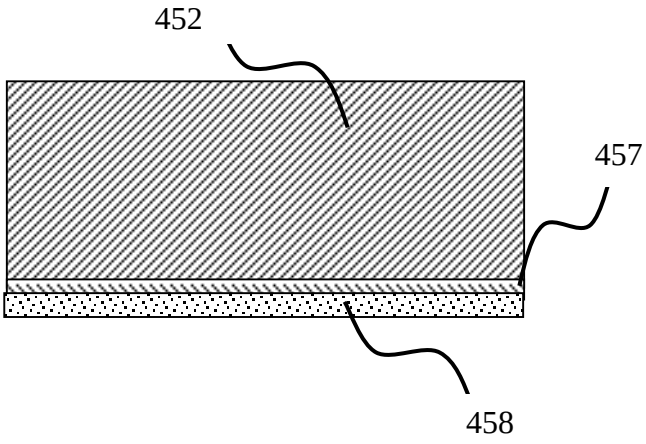


Fig. 4B

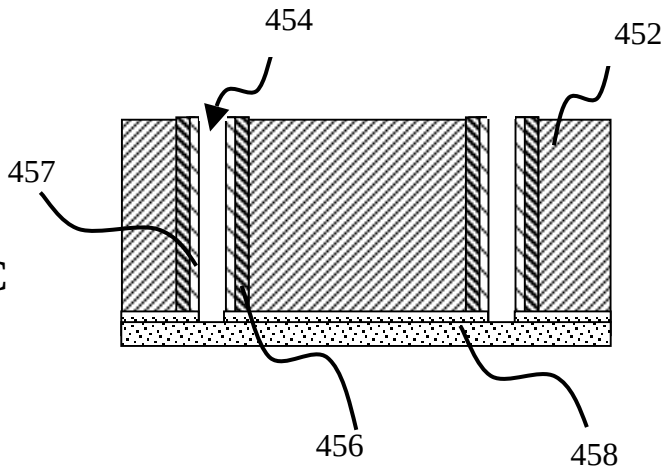


Fig. 4C

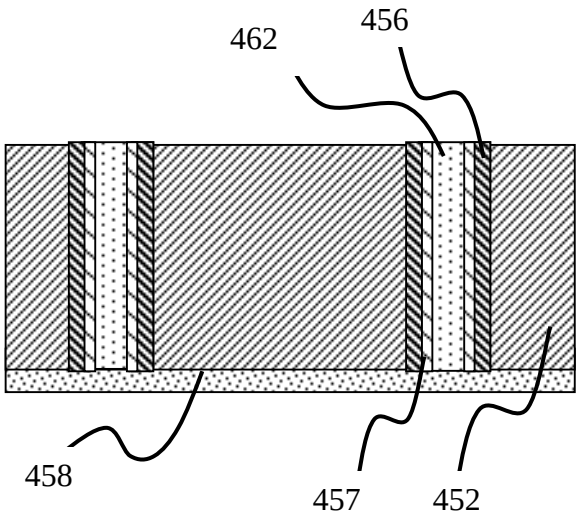


Fig. 4D

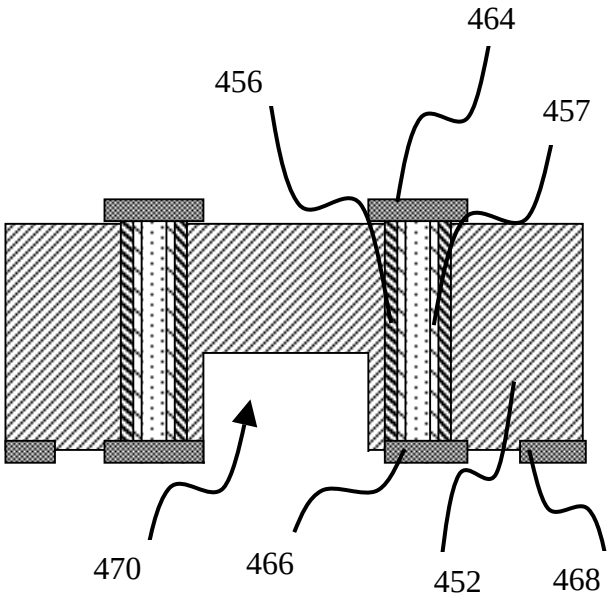

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Fig. 4E

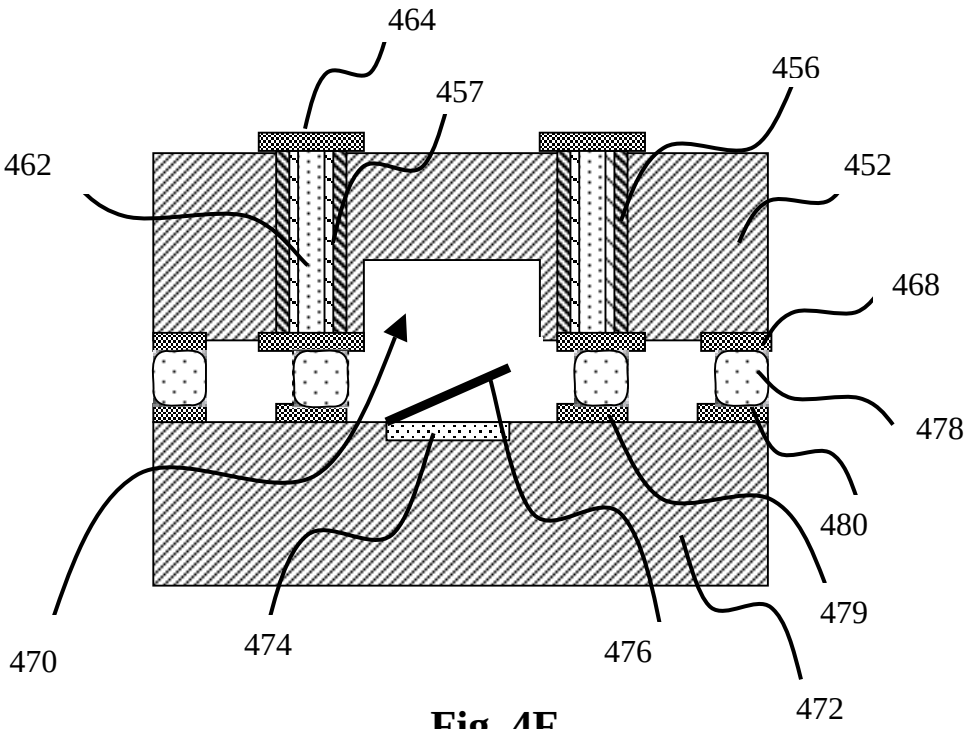

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Fig. 4F

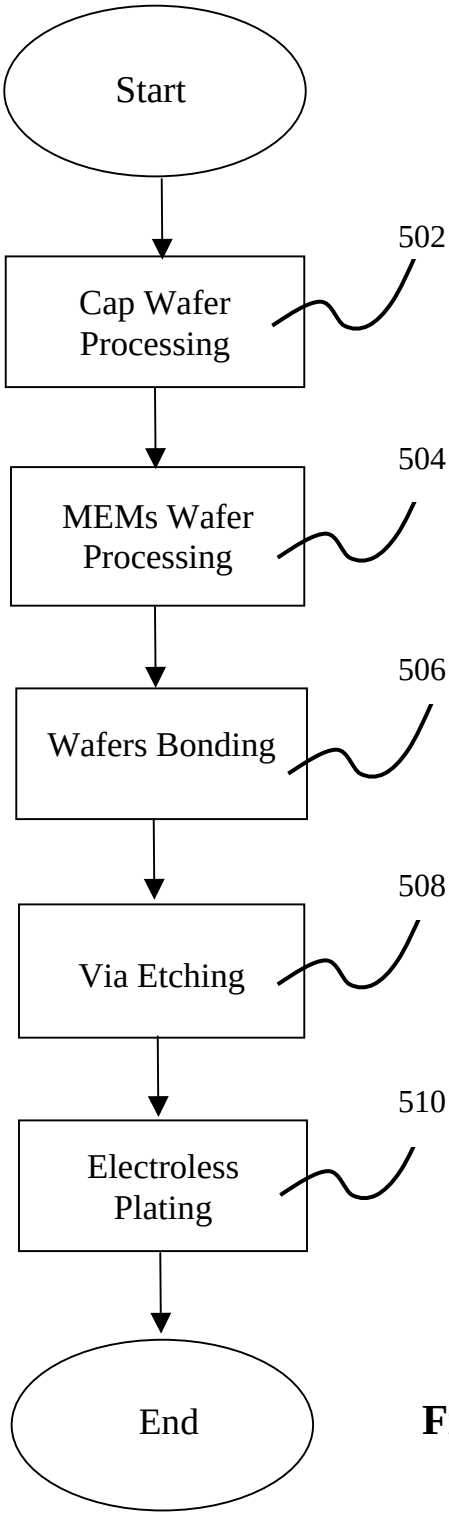

Start
502
Cap Wafer Processing
504
MEMs Wafer Processing
506
Wafers Bonding
508
Via Etching
510
Electroless Plating
End

Fig. 5A

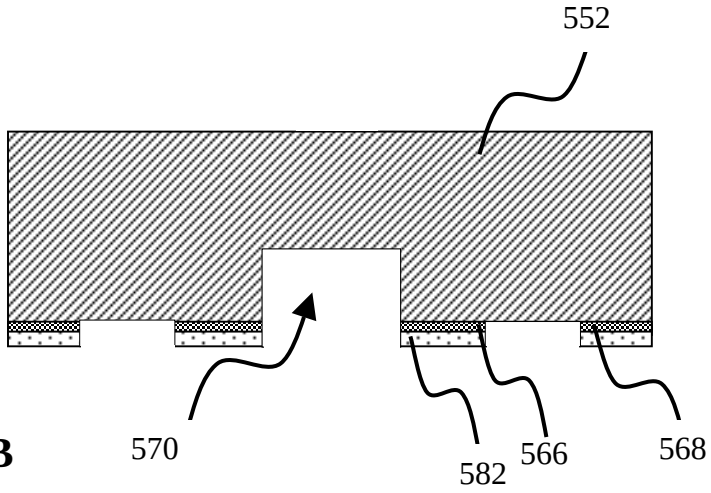


Fig. 5B

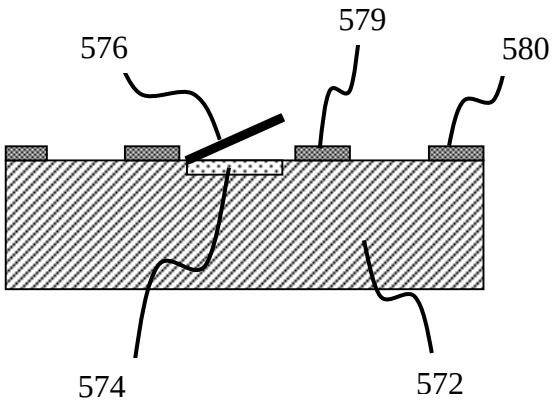


Fig. 5C

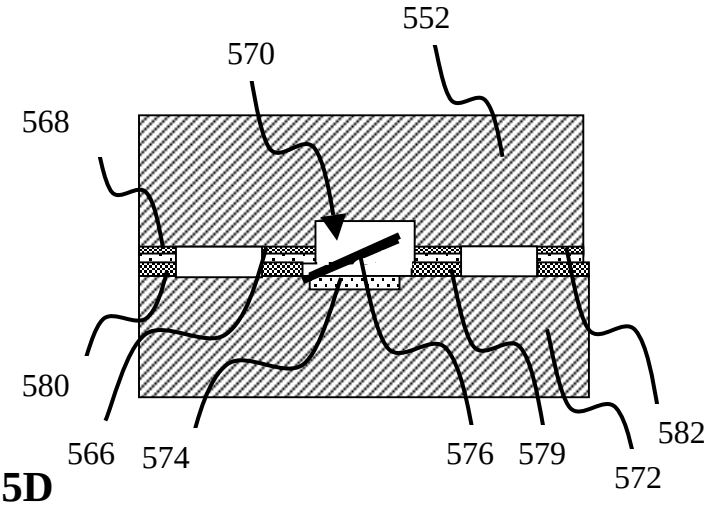


Fig. 5D

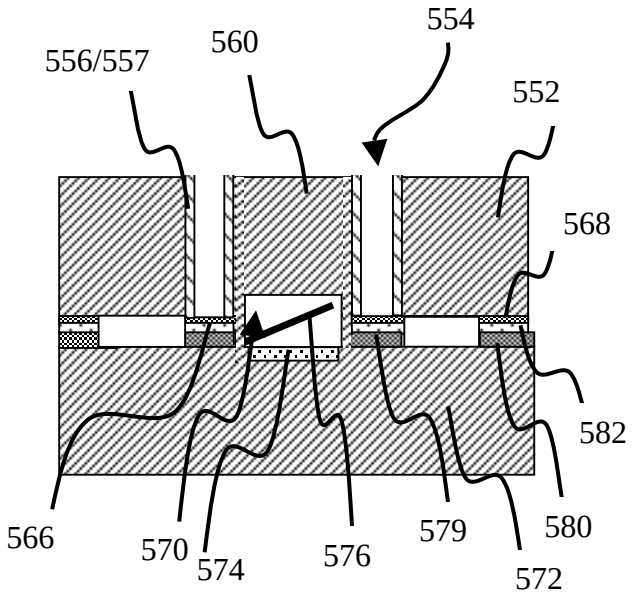

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Fig. 5E

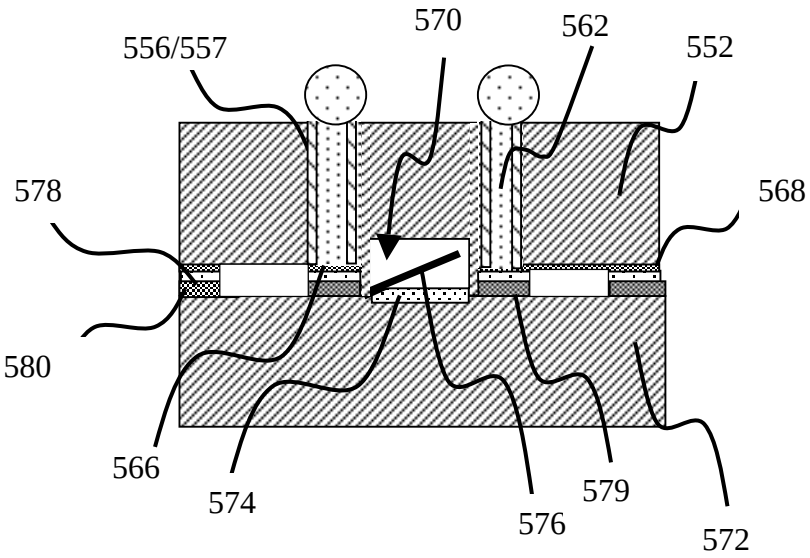

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Fig. 5F

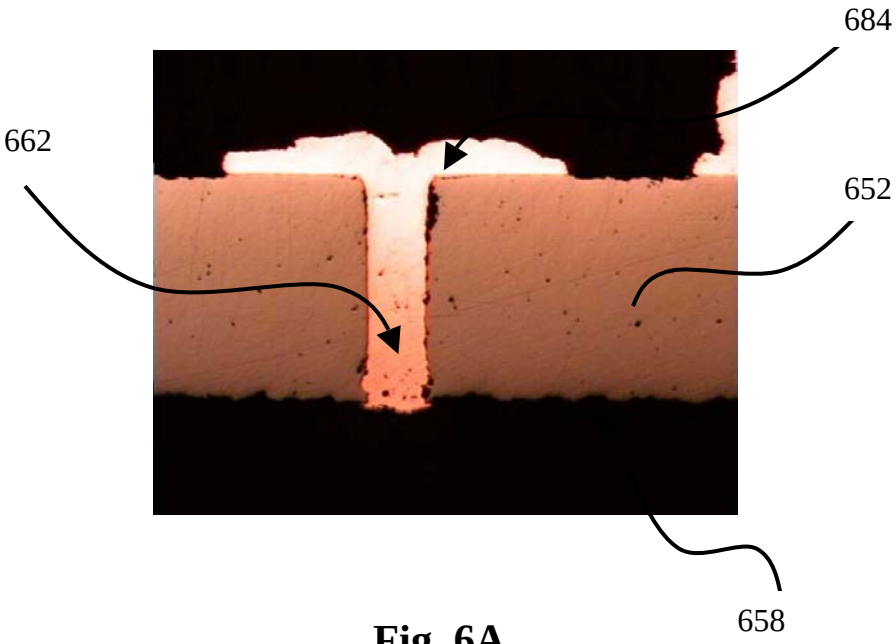


Fig. 6A

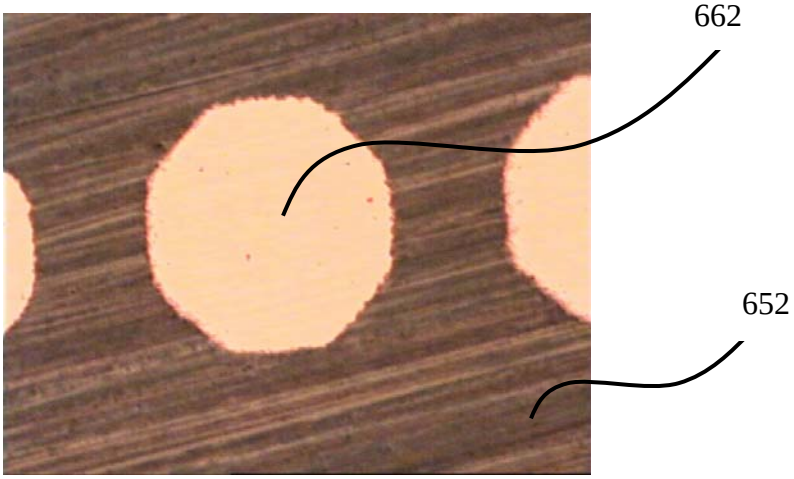


Fig. 6B

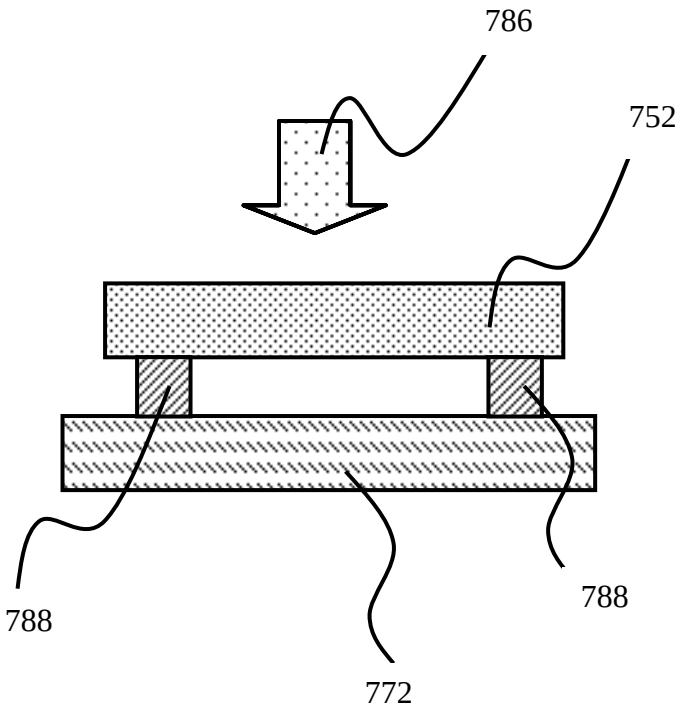


Fig. 7