

FIG. 1

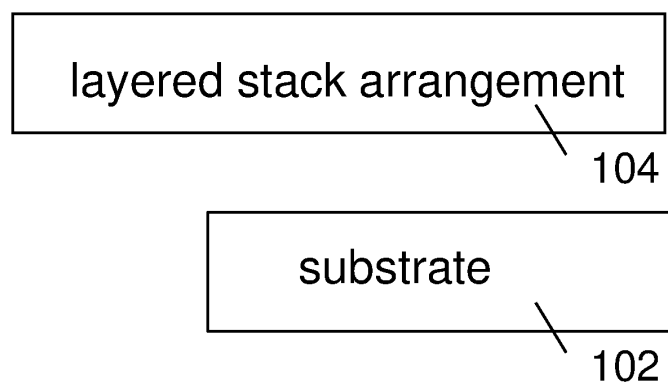


FIG. 2

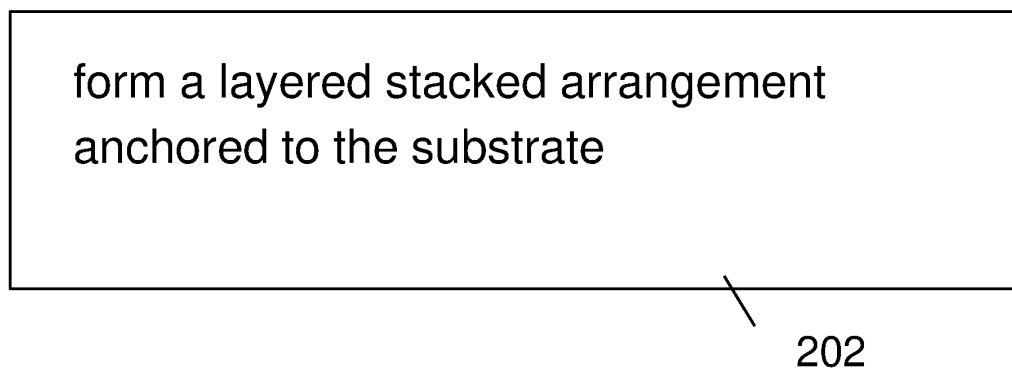


FIG. 3

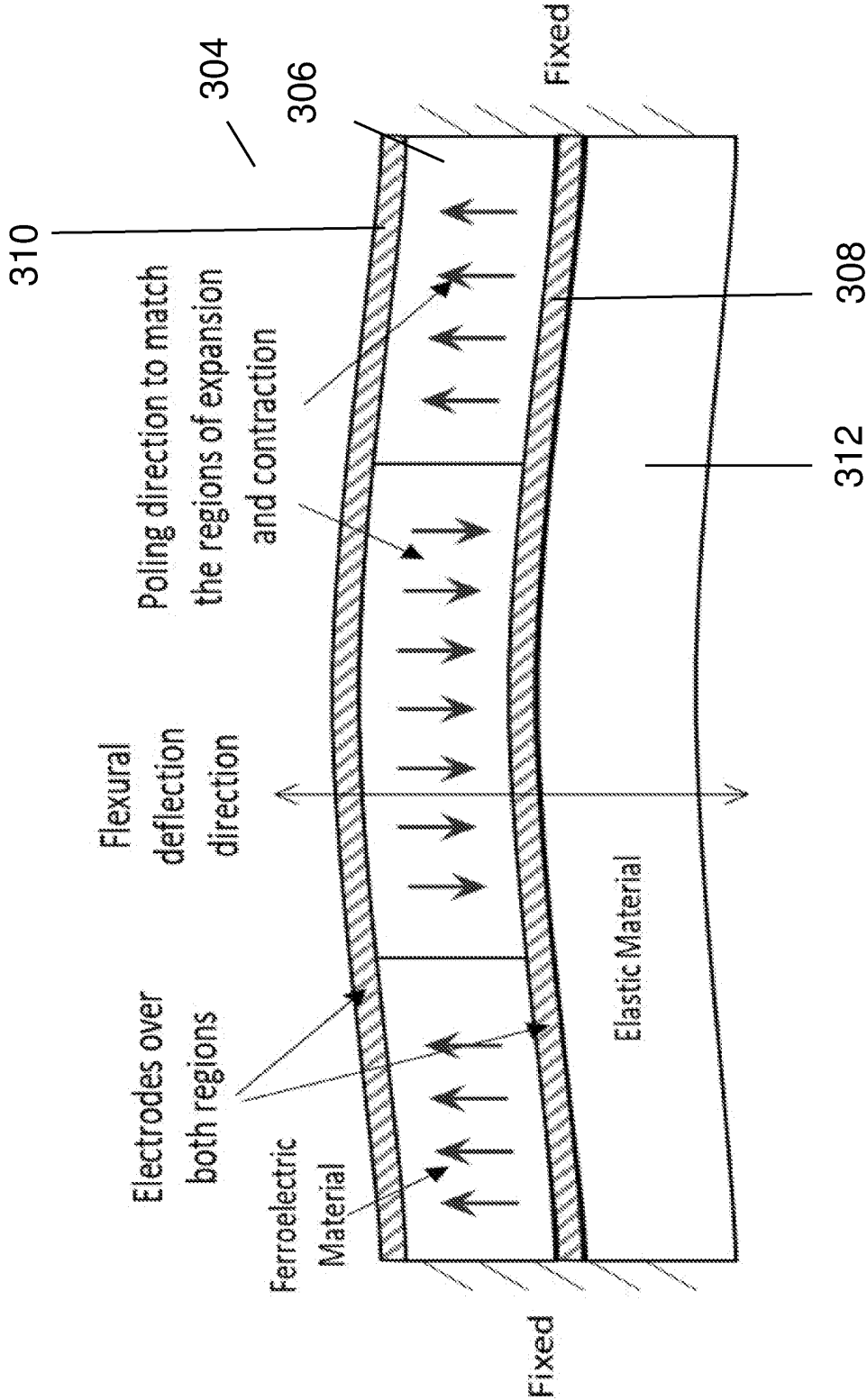


FIG. 4A

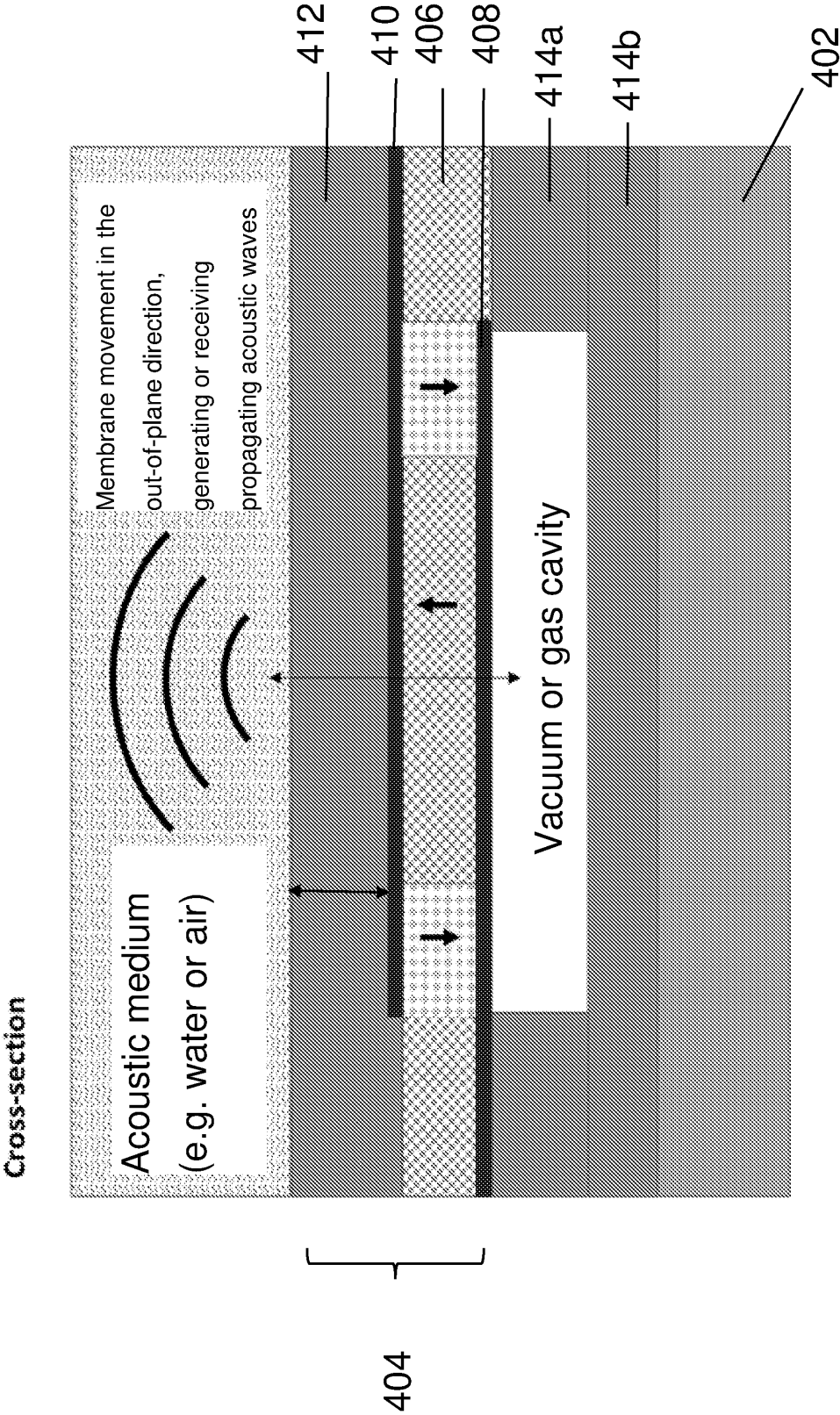


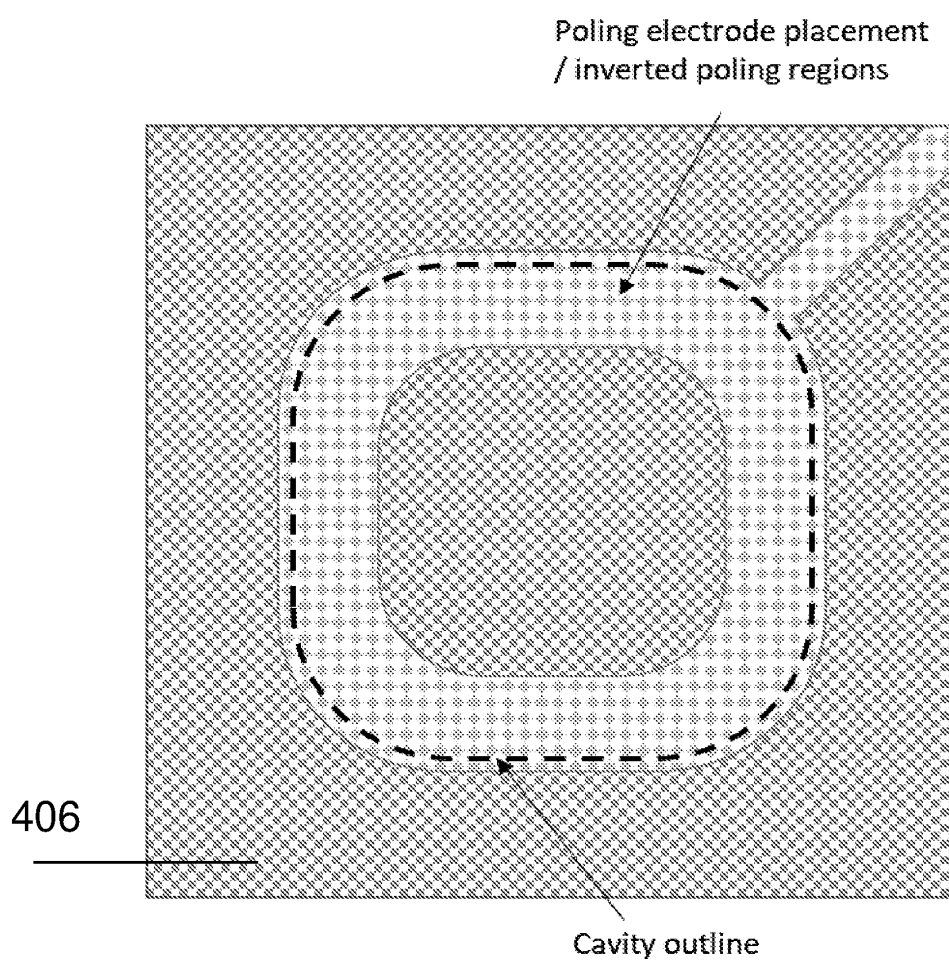
FIG. 4B**Top View**

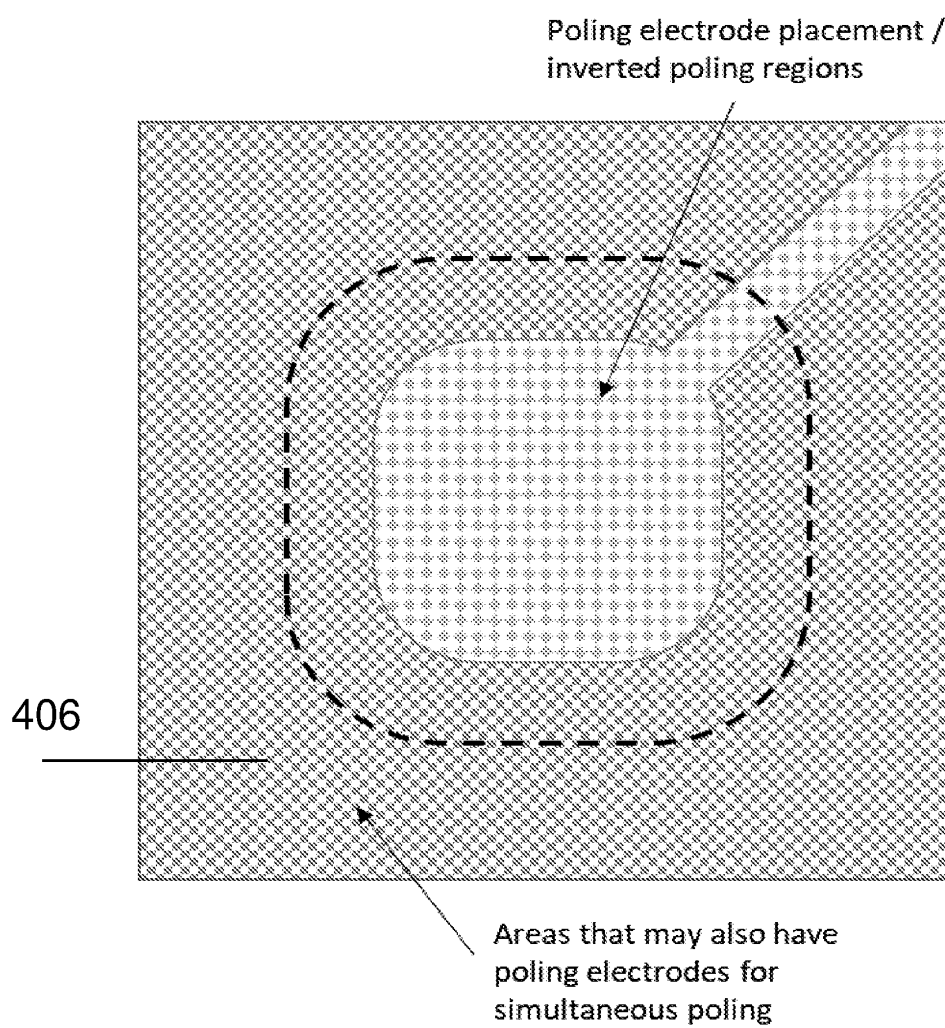
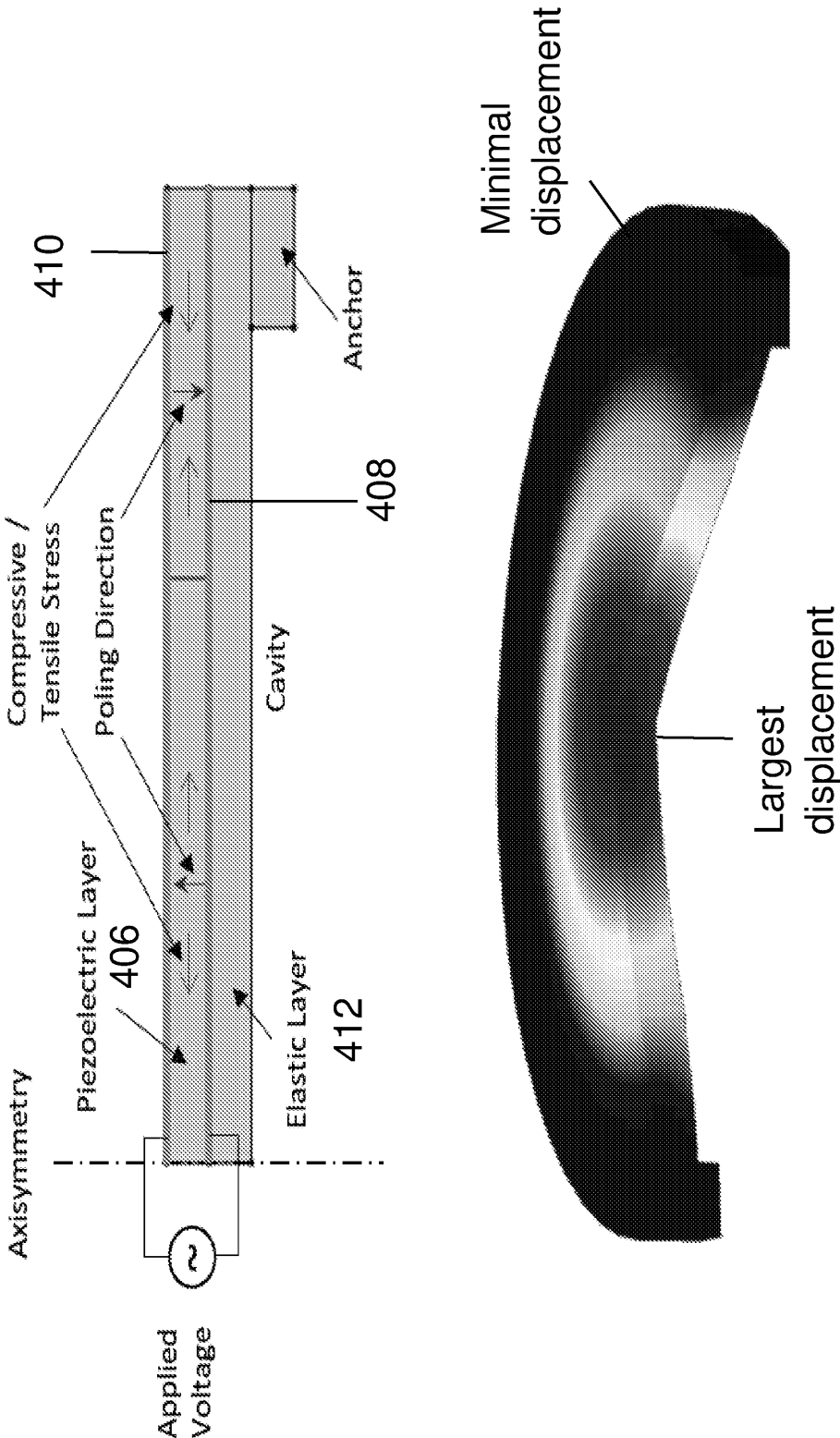
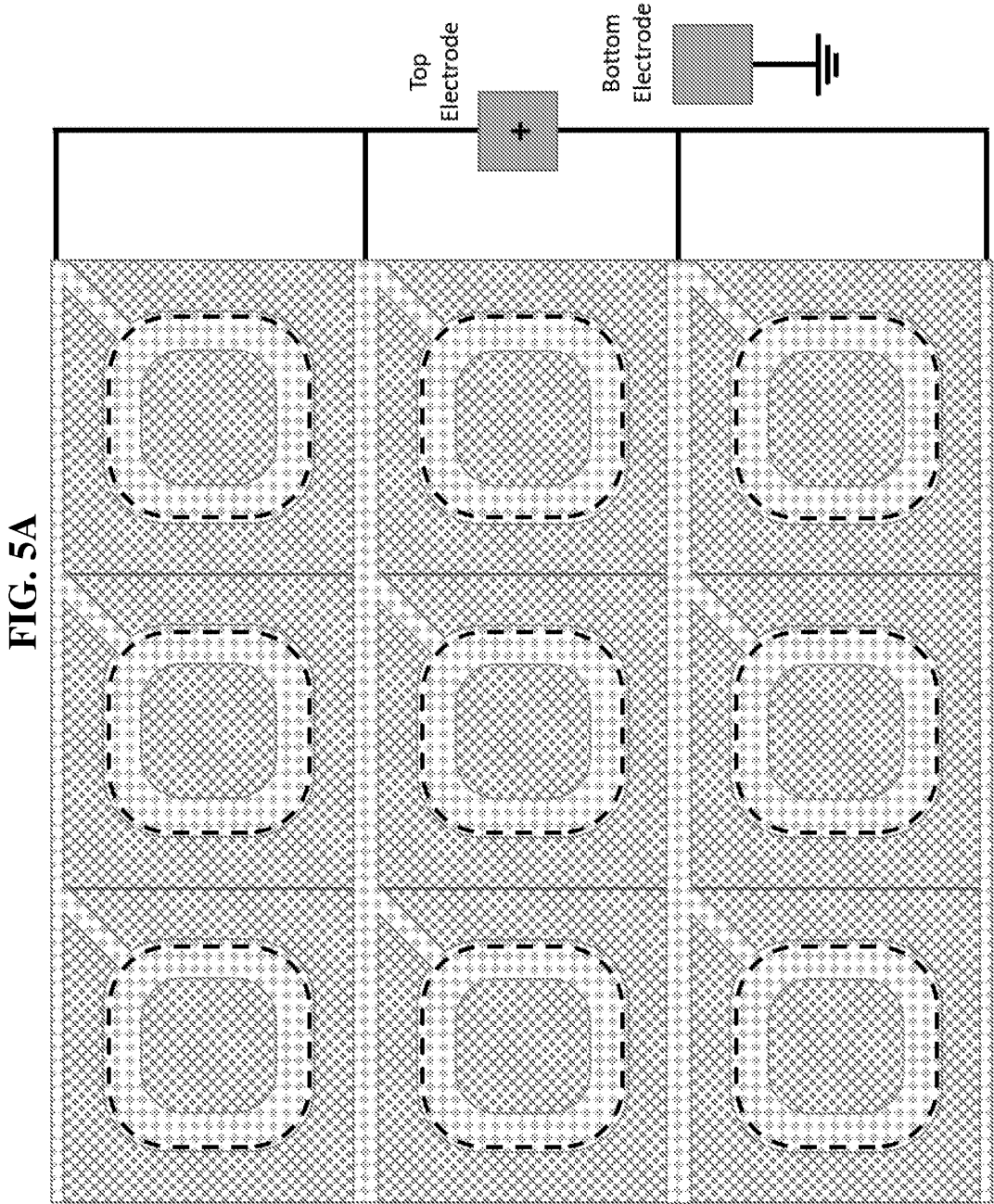
FIG. 4C**Top View**

FIG. 4D





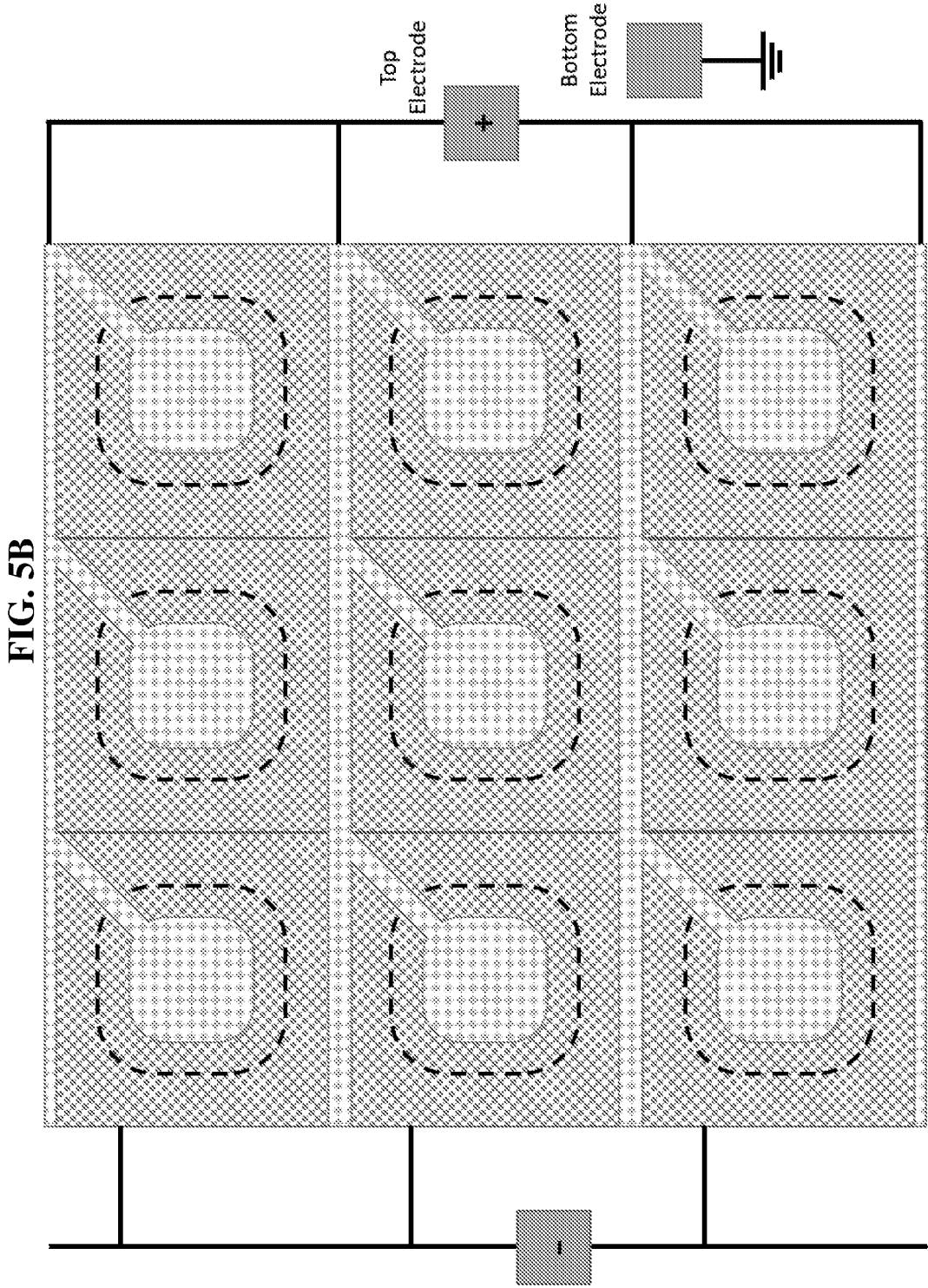


FIG. 6

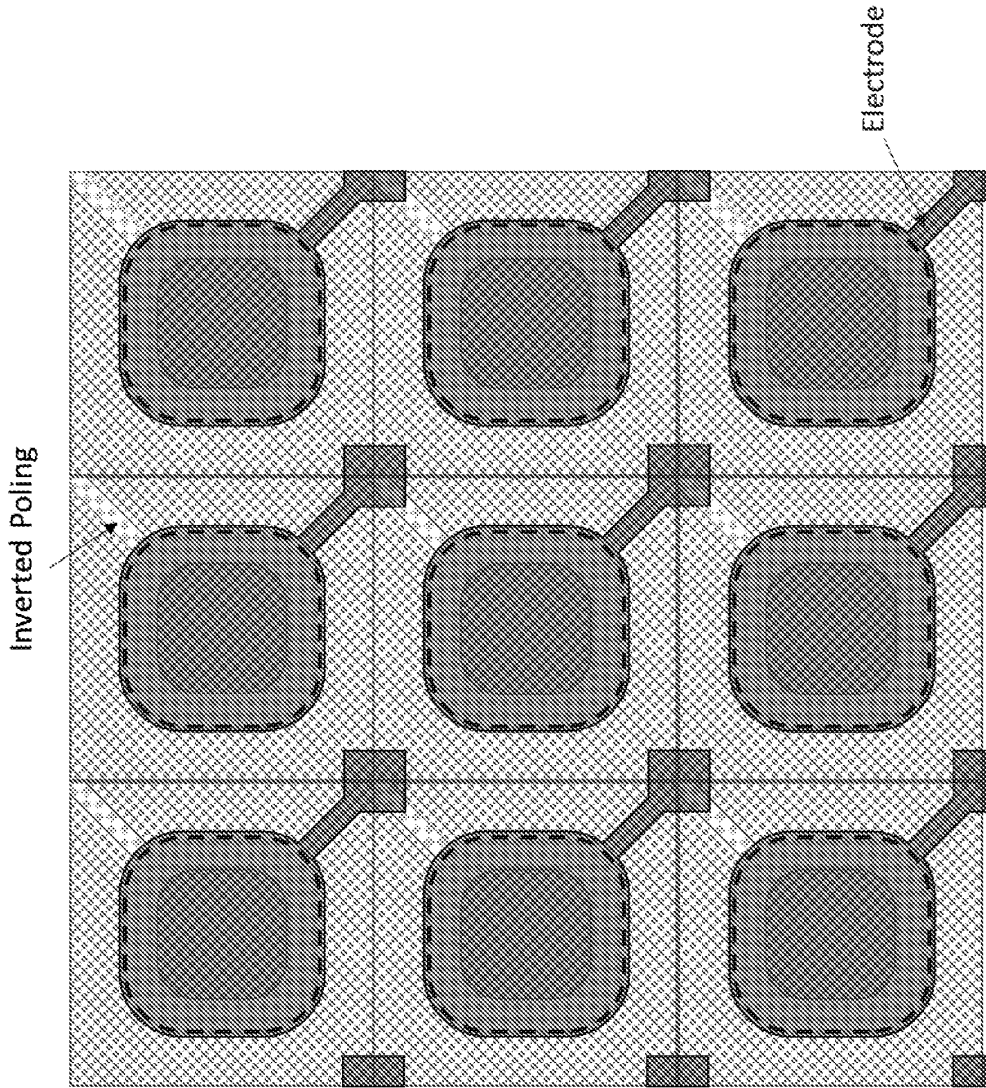


FIG. 7

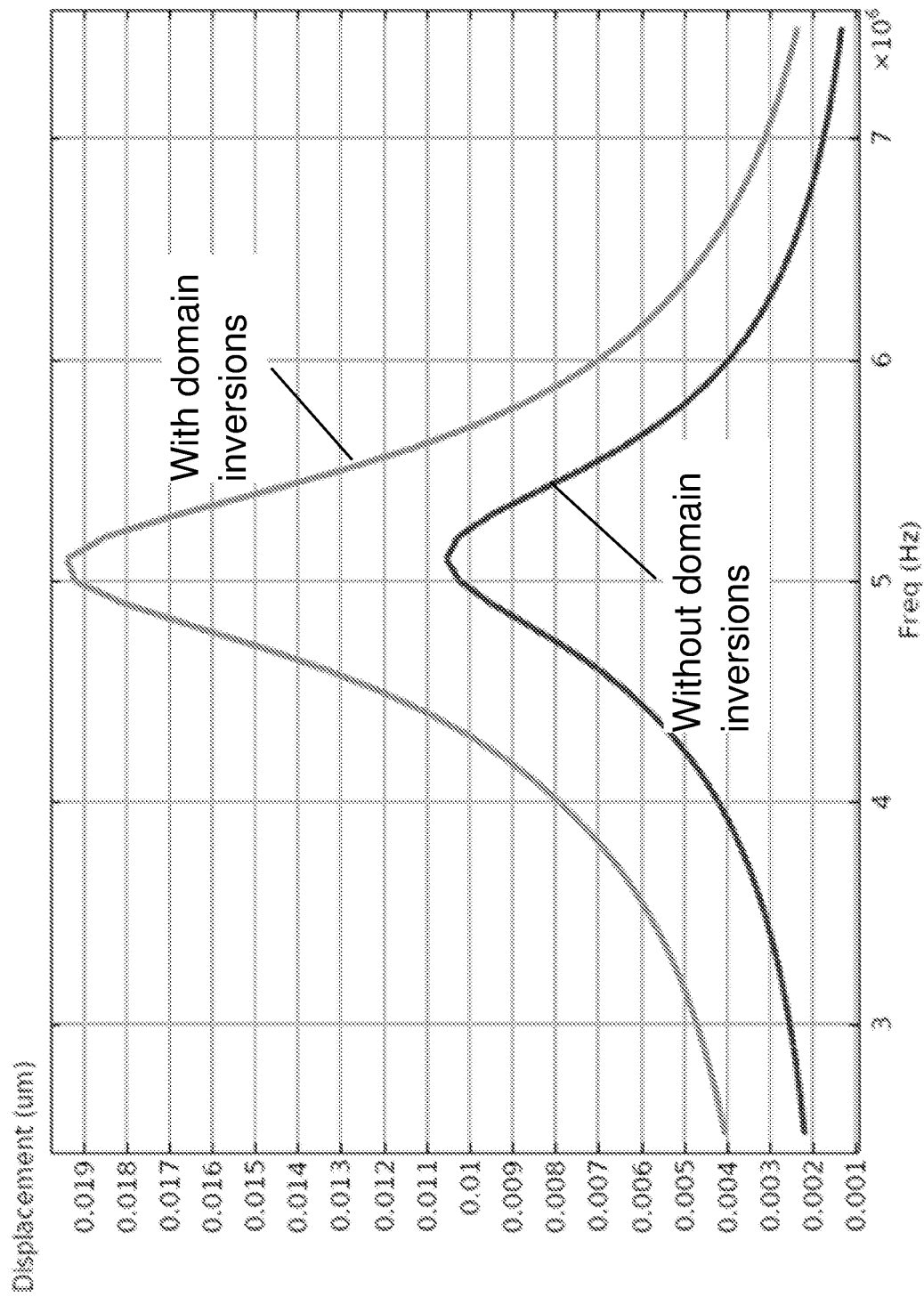
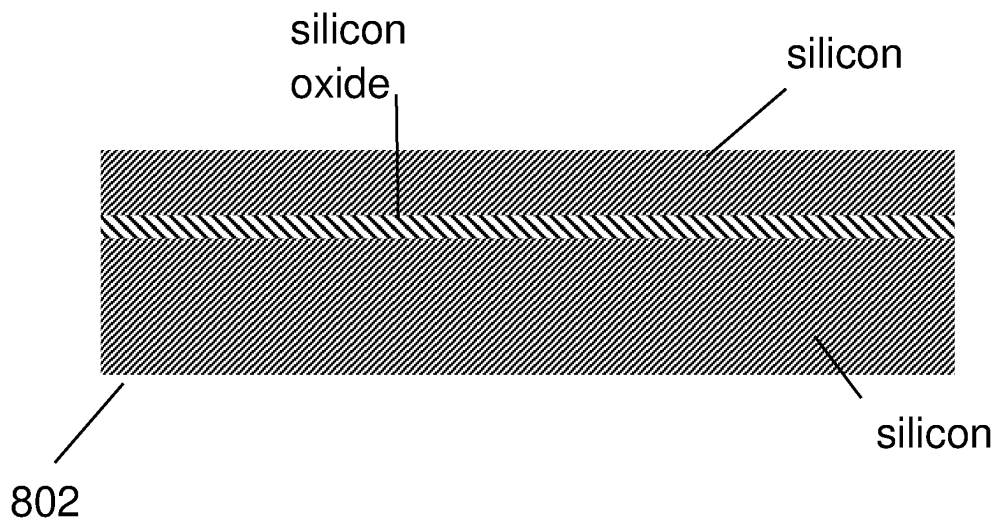


FIG. 8A

Start with a substrate, such as a silicon-on-insulator (SOI)

**FIG. 8B**

Deposit a bottom electrode

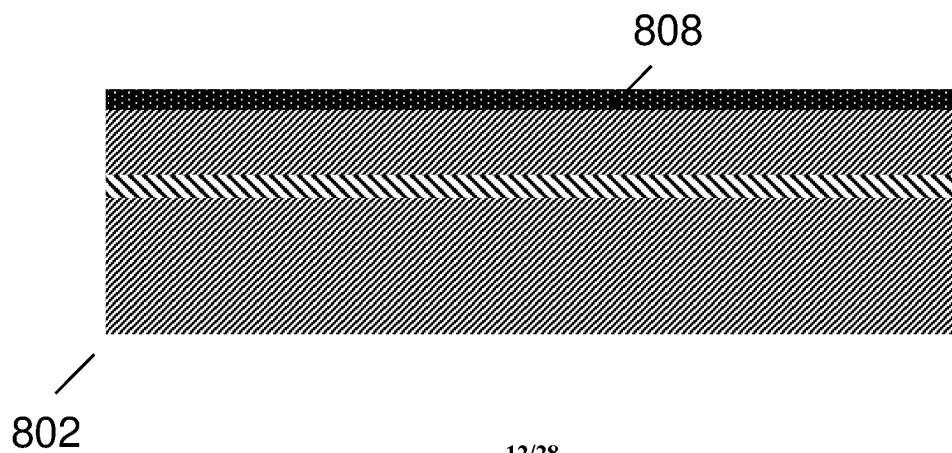
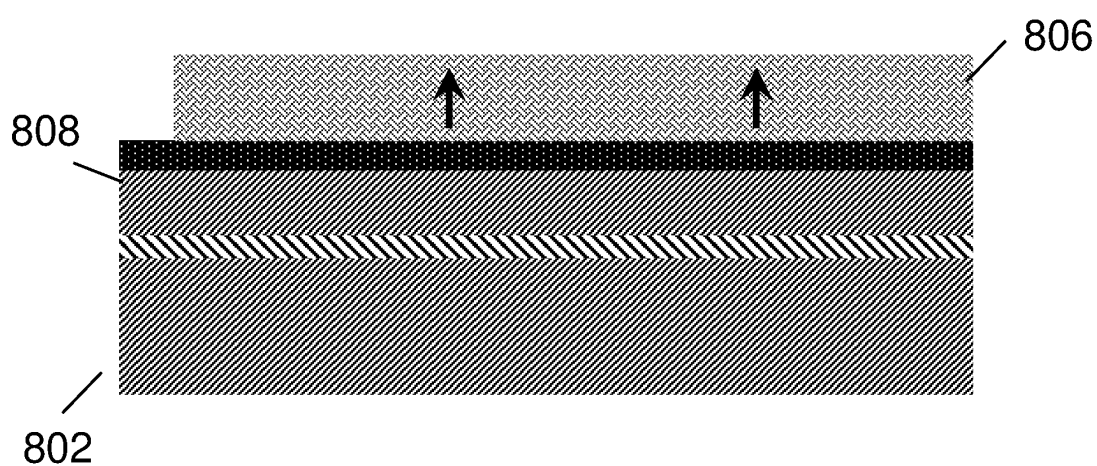


FIG. 8C

Deposit a piezoelectric layer

**FIG. 8D**

Deposit a temporary electrode and pattern.
Pole multiple connected regions at the same time

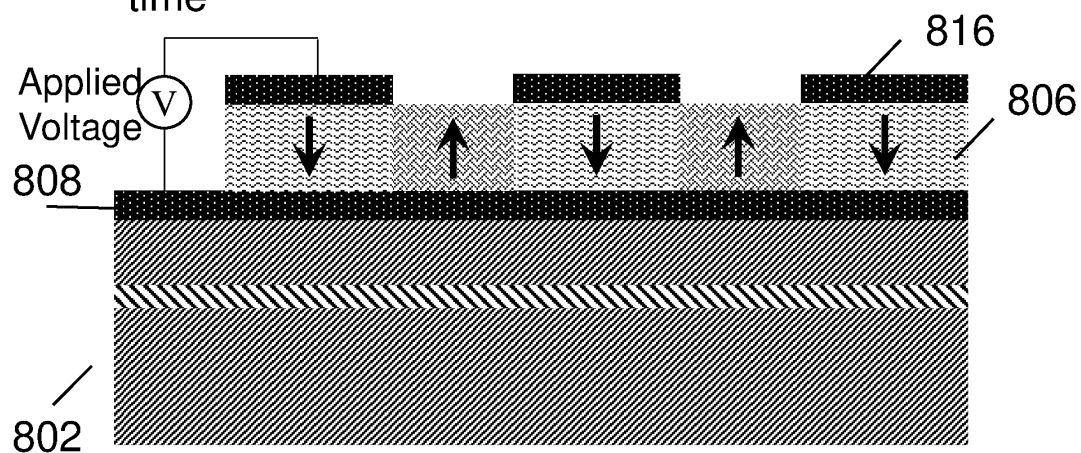


FIG. 8E

Remove the temporary electrode

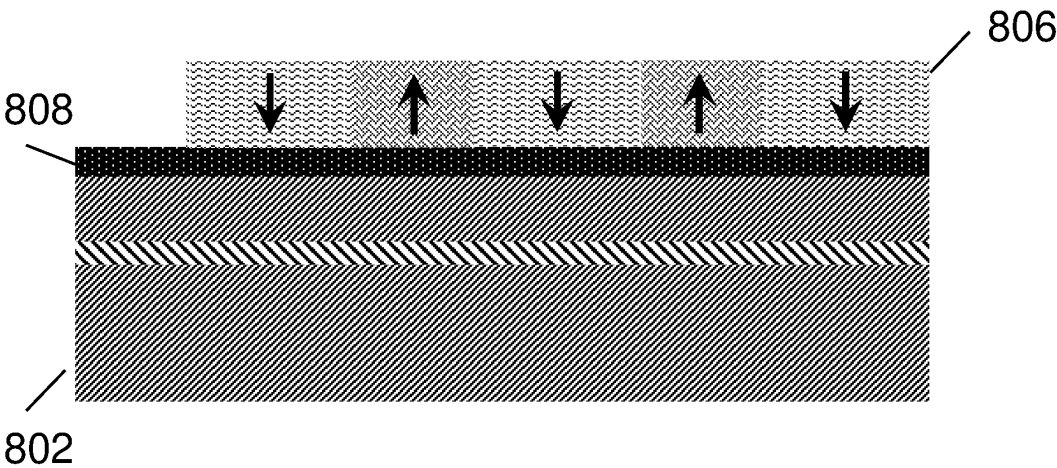


FIG. 8F

Deposit a final top electrode of a different geometry from the temporary electrode

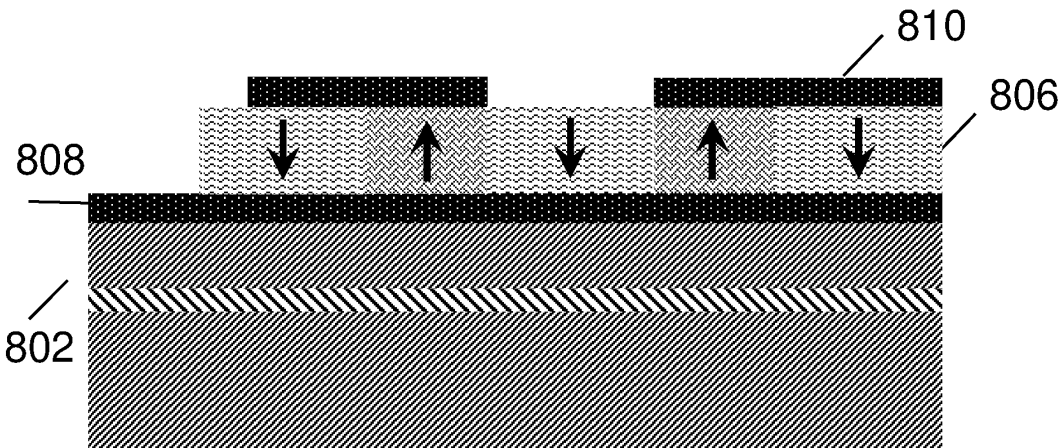
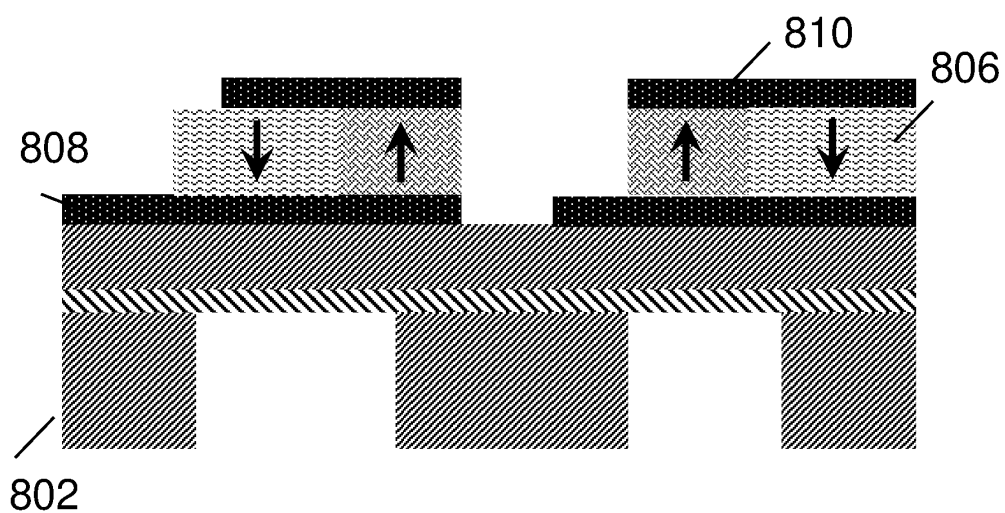


FIG. 8G

Additional process: e.g. Device release

**FIG. 8H**

Singulate the devices

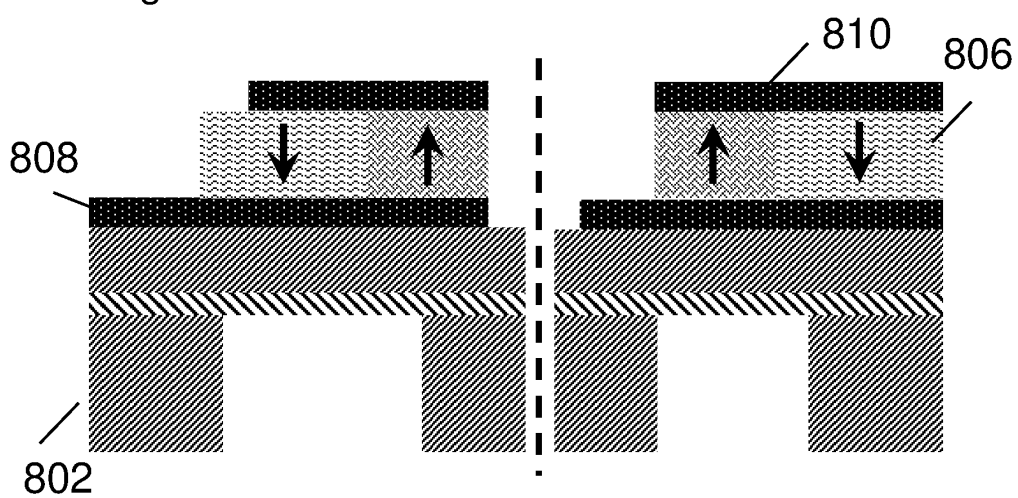


FIG. 9A

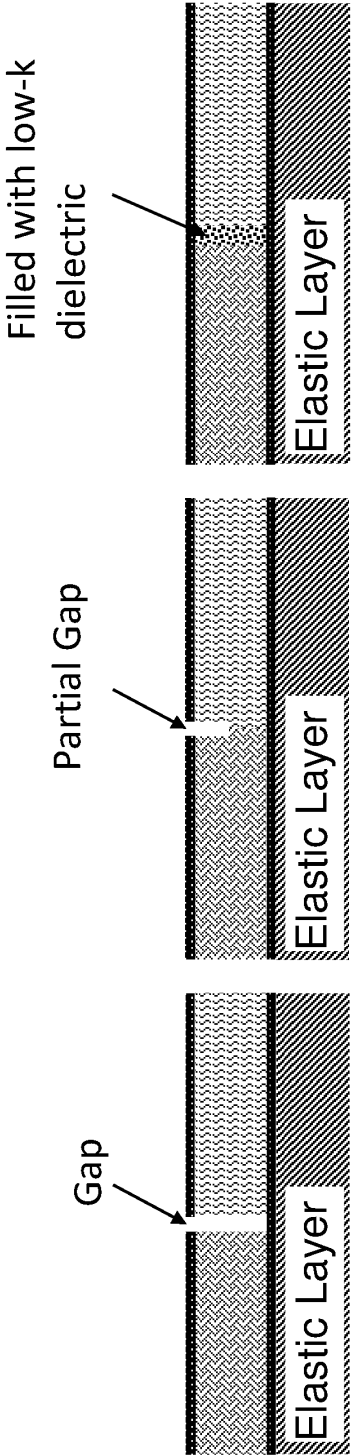


FIG. 9B

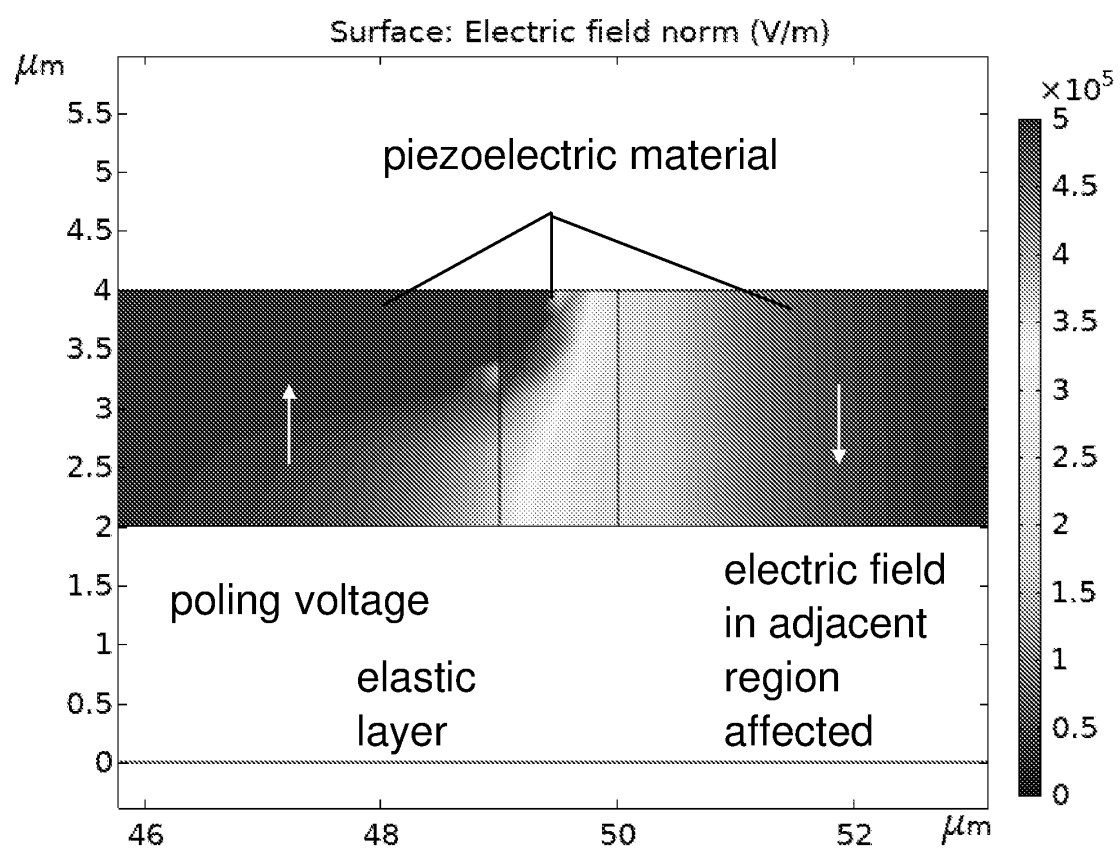


FIG. 9C

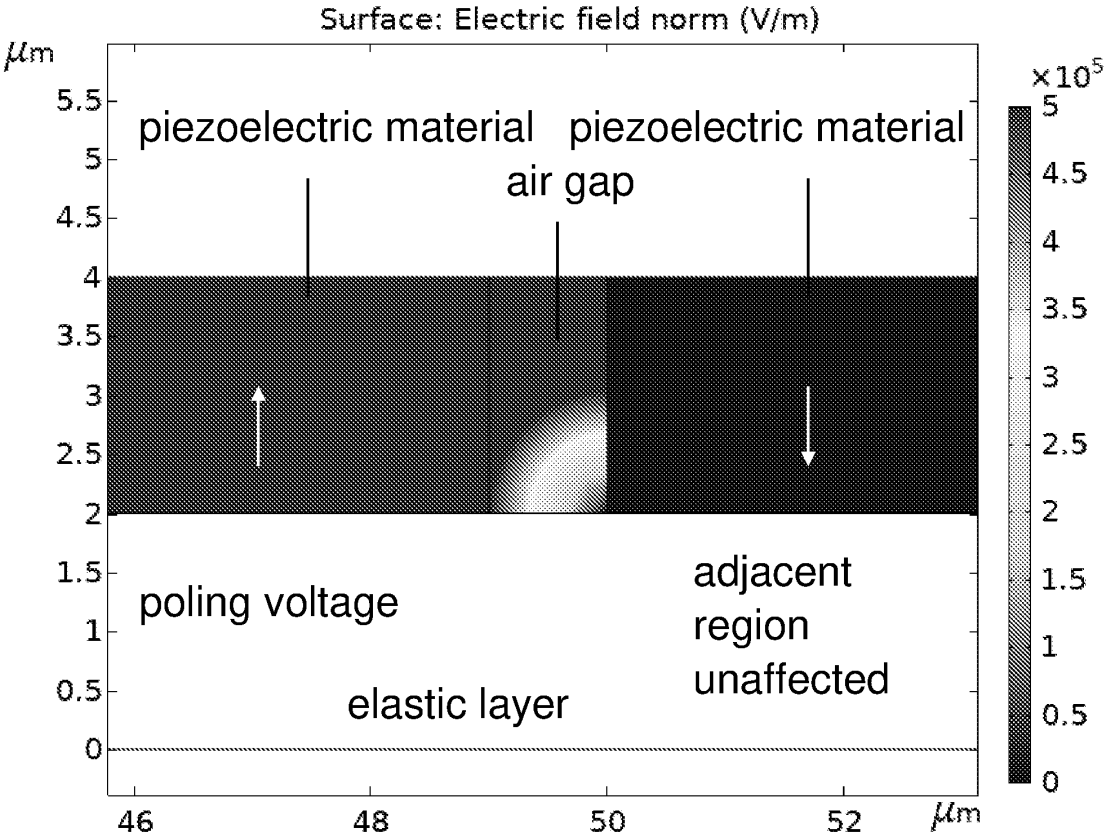


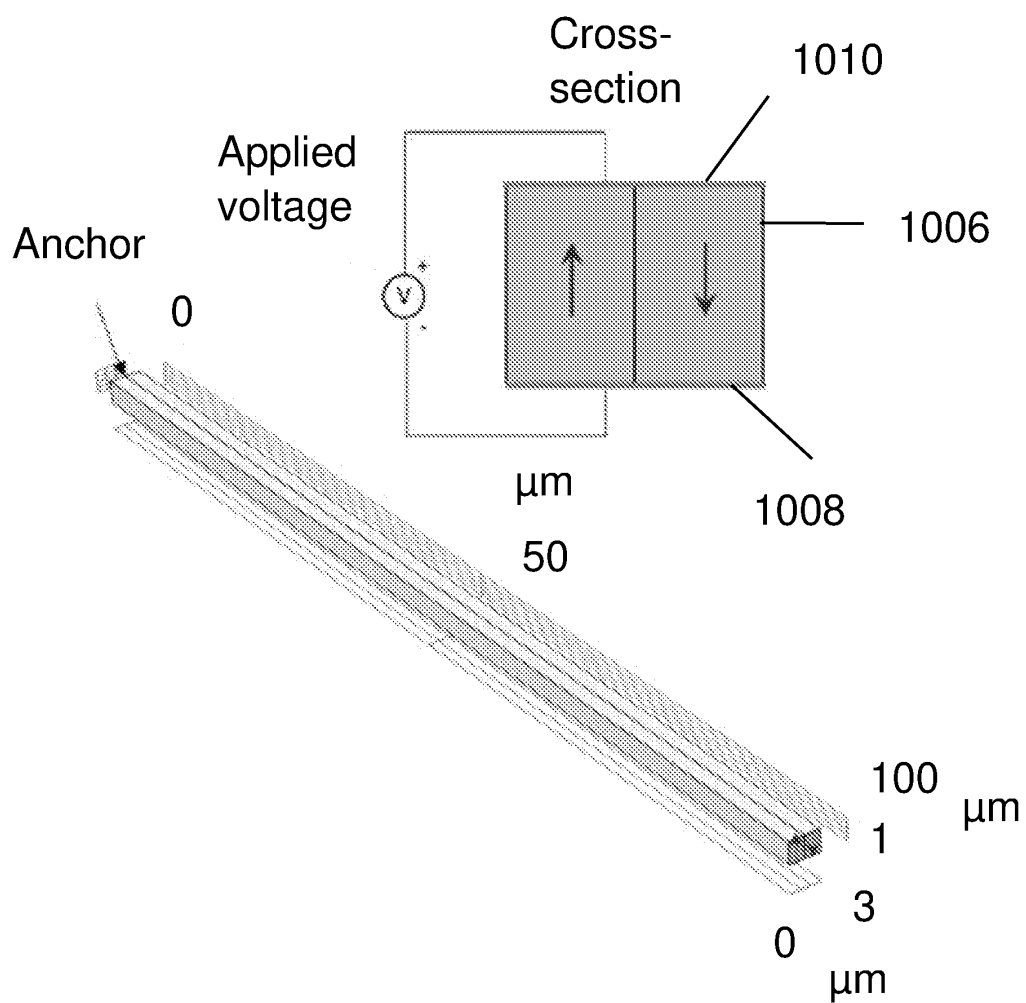
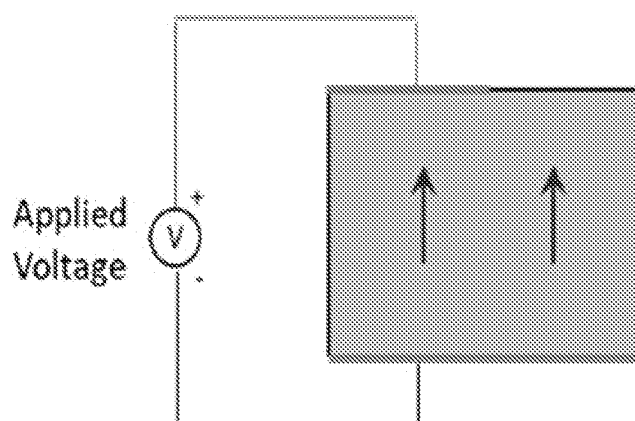
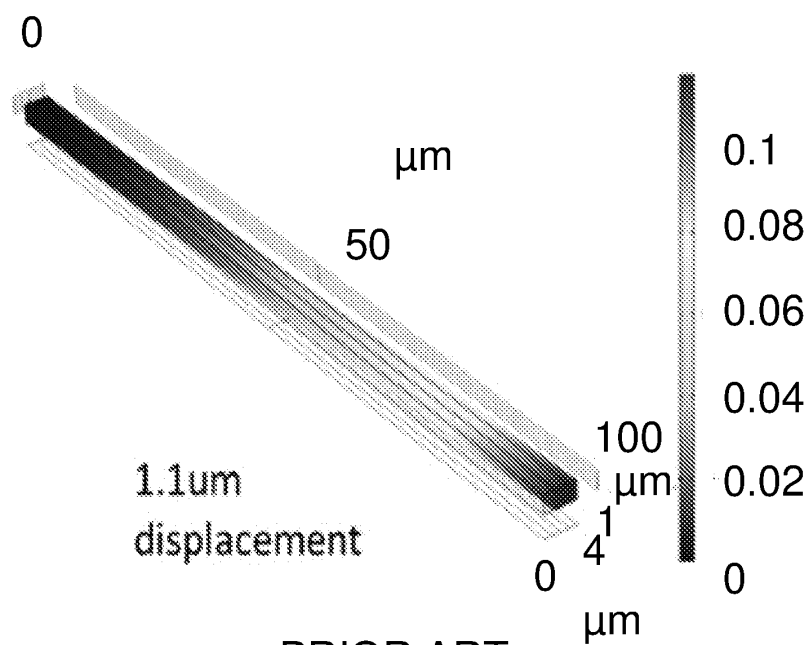
FIG. 10A

FIG. 10B

Unimorph structure: easy to fabricate but low performance



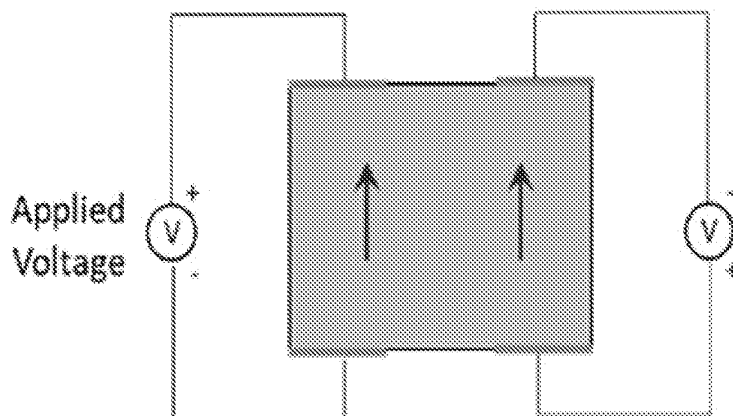
Surface: Total displacement (μm)



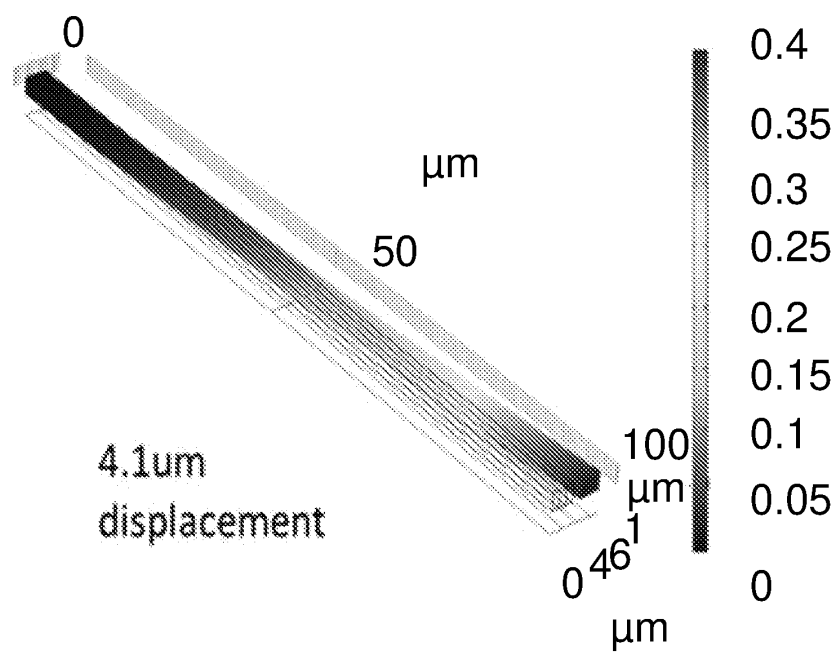
- PRIOR ART -

FIG. 10C

Bimorph structure: high performance
but hard to fabricate and electrically
address



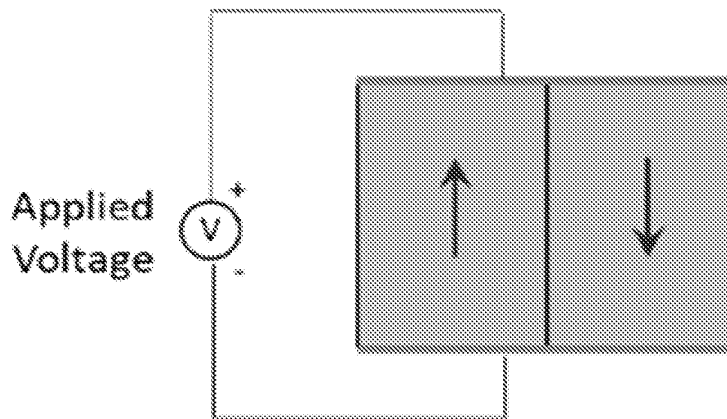
Surface: Total displacement (μm)



- PRIOR ART -

FIG. 10D

Proposed structure: easy to fabricate
and high performance



Surface: Total displacement (μm)

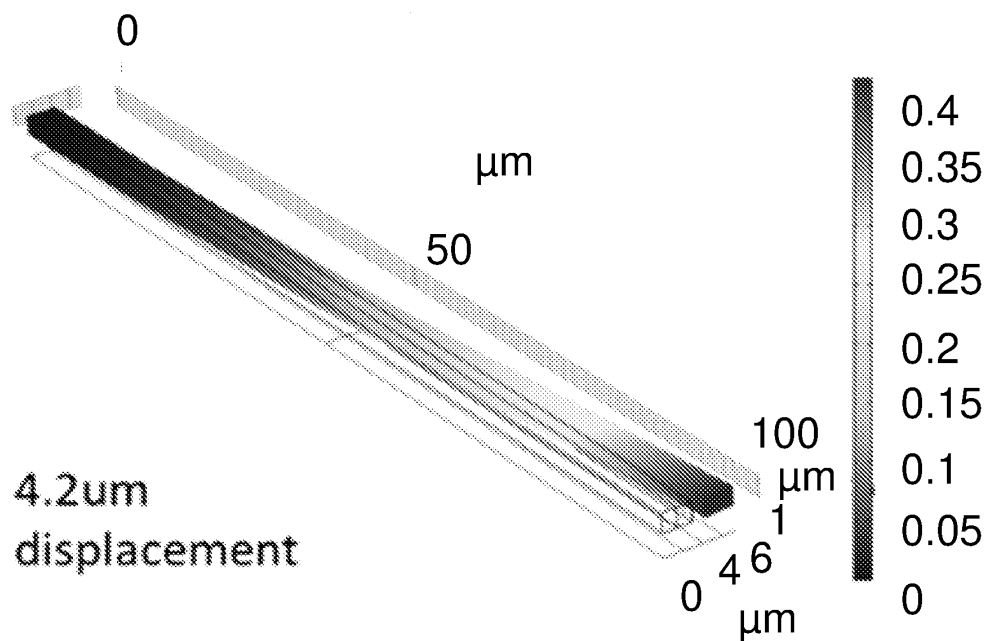


FIG. 11

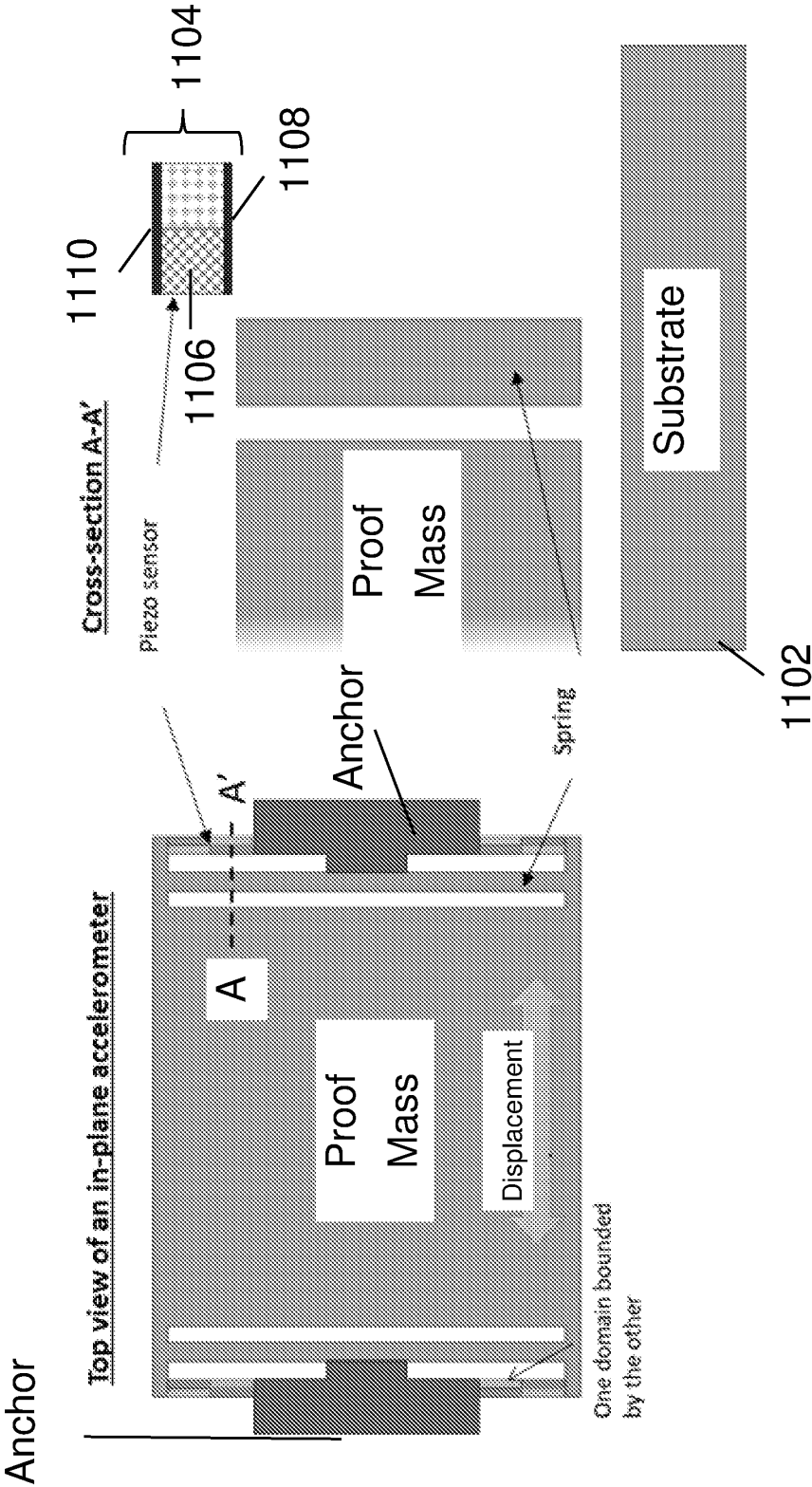


FIG. 12

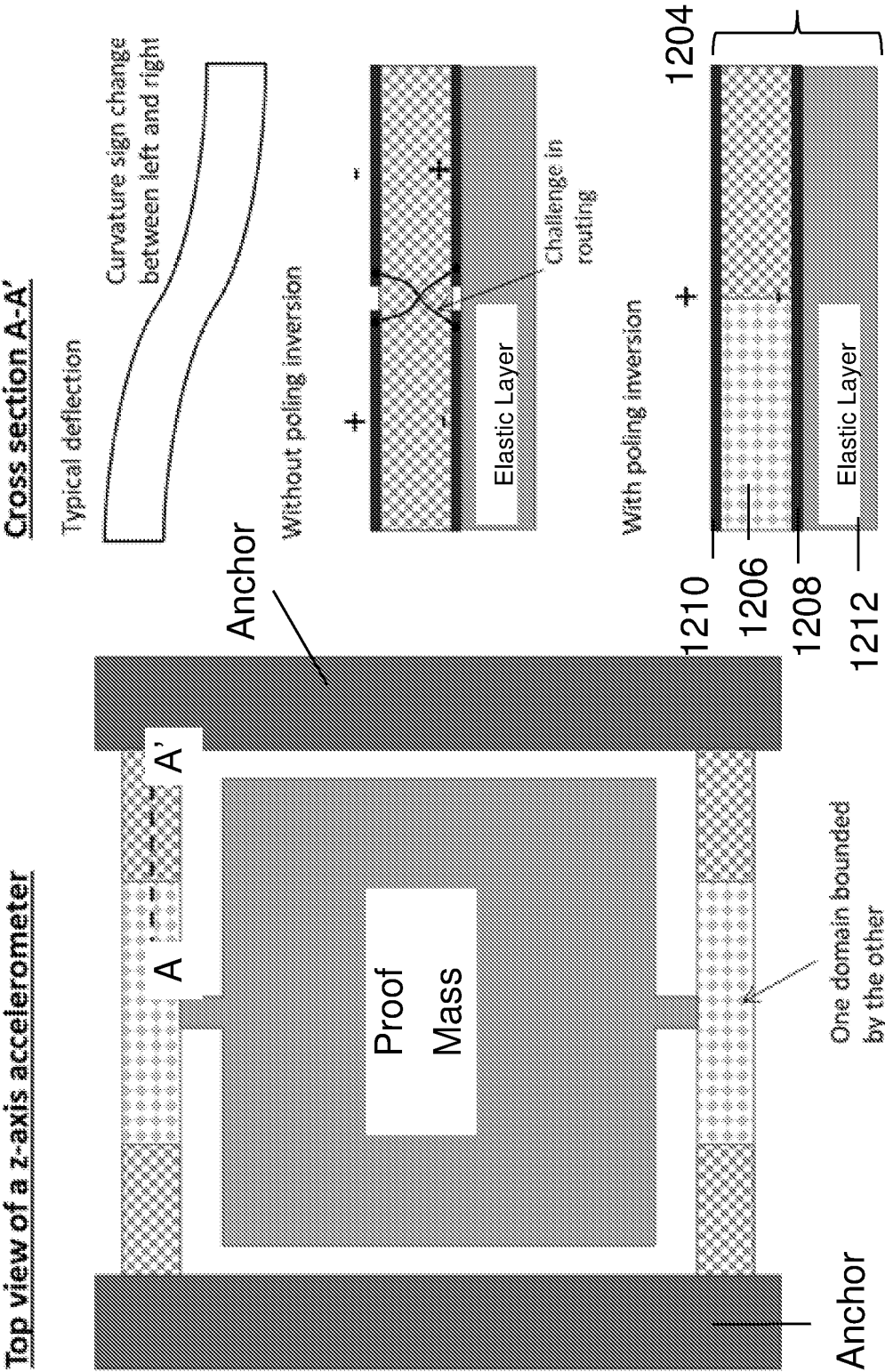


FIG. 13

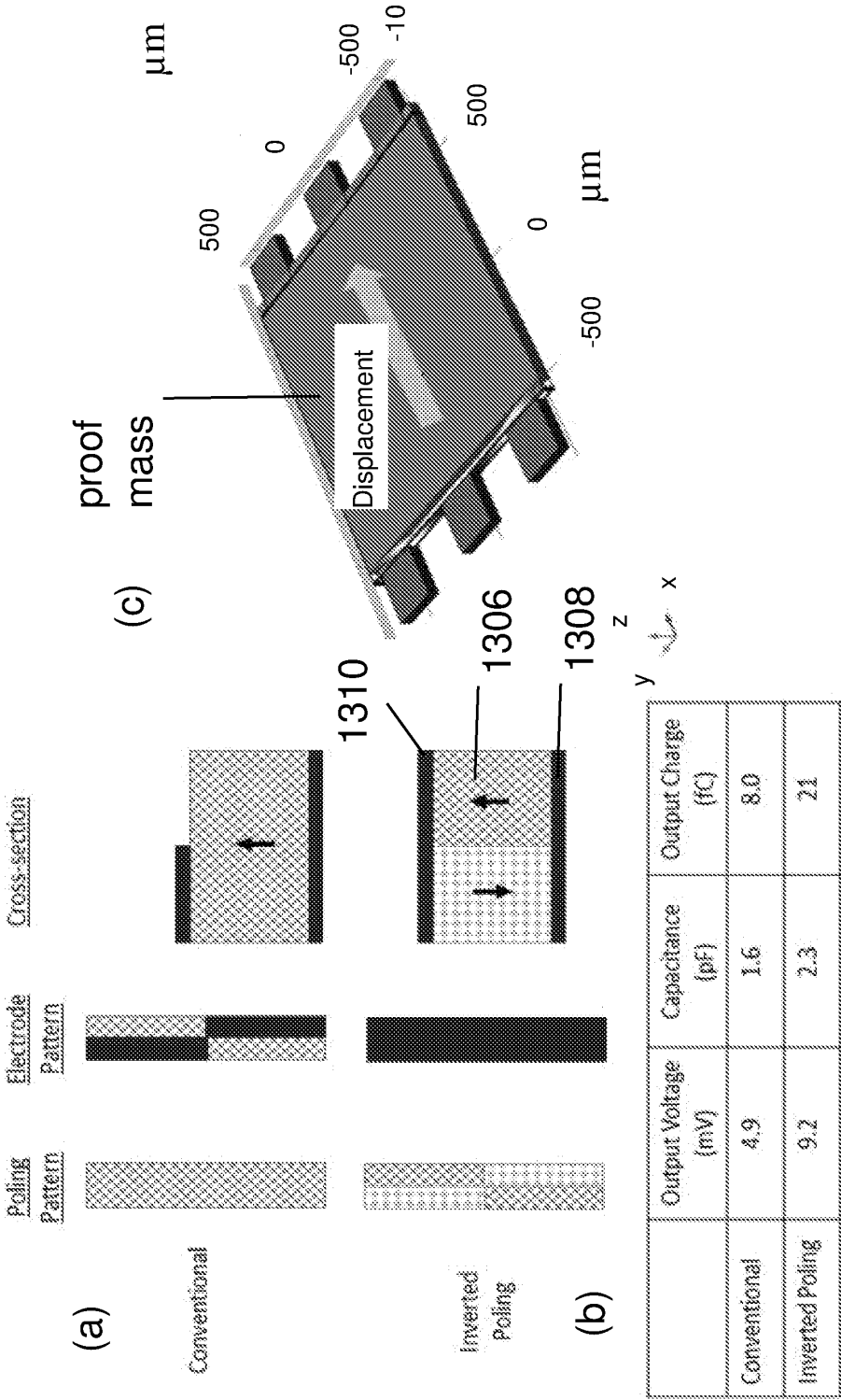


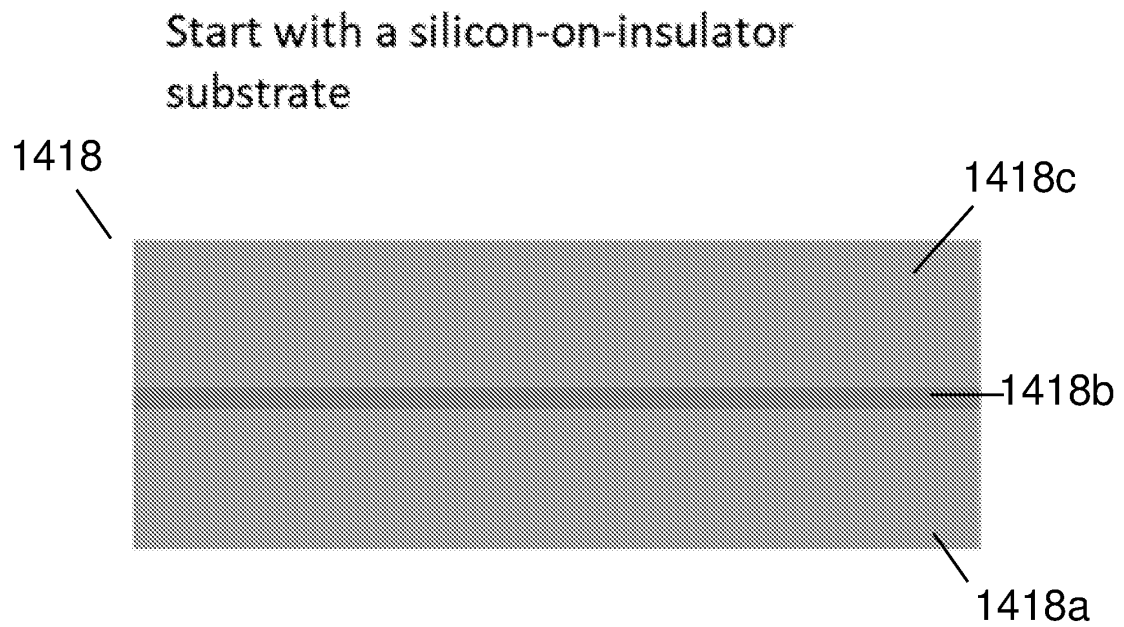
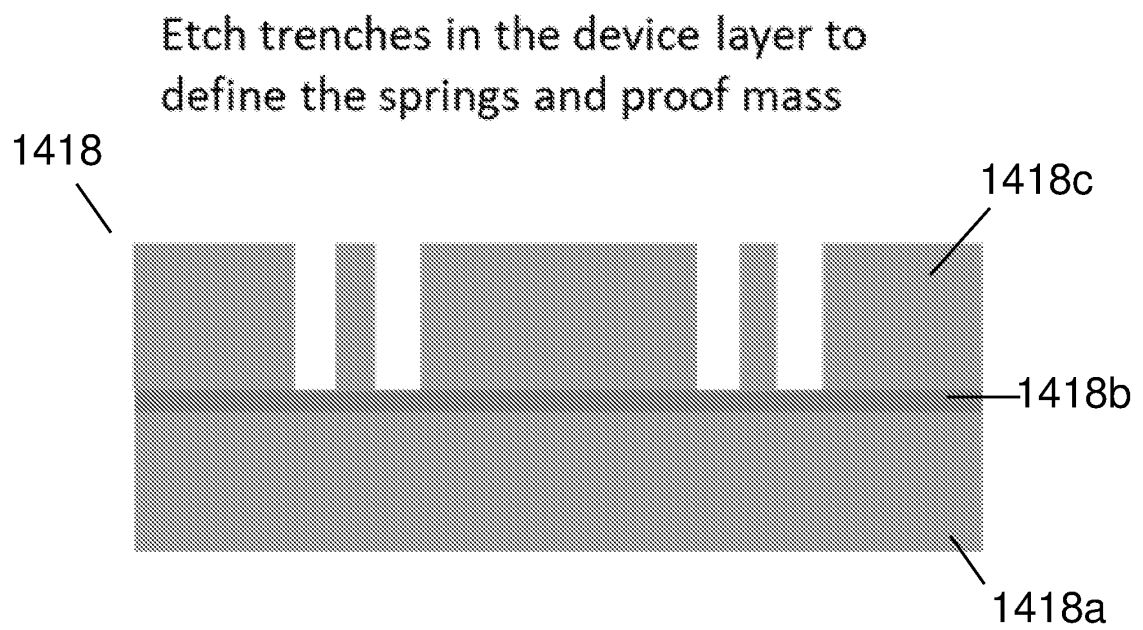
FIG. 14A**FIG. 14B**

FIG. 14C

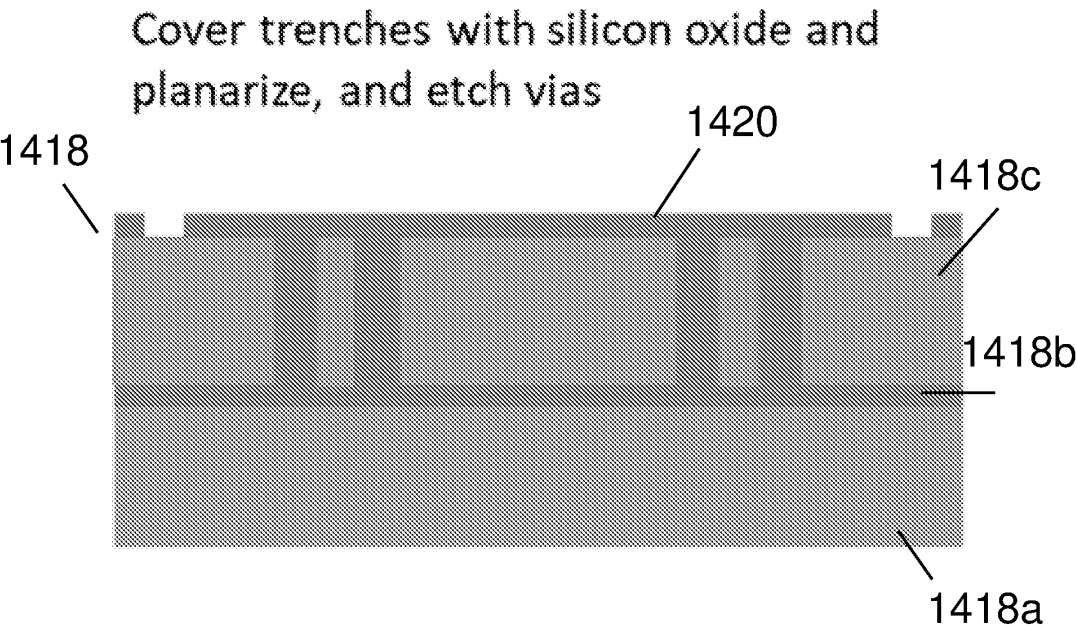


FIG. 14D

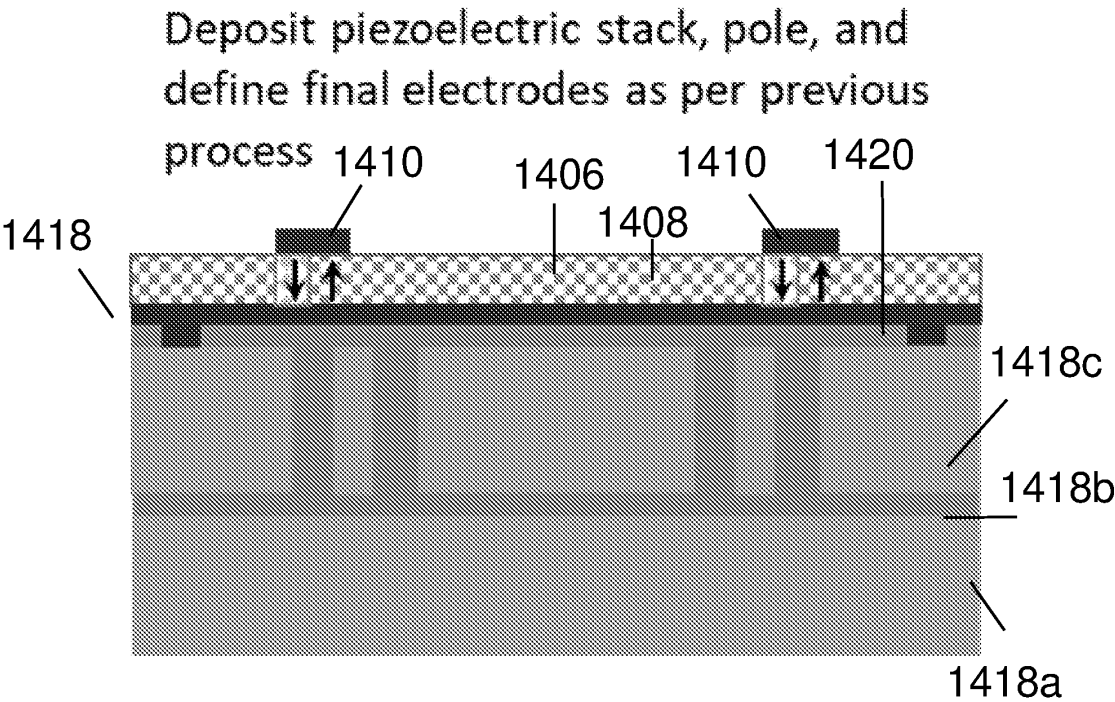


FIG. 14E

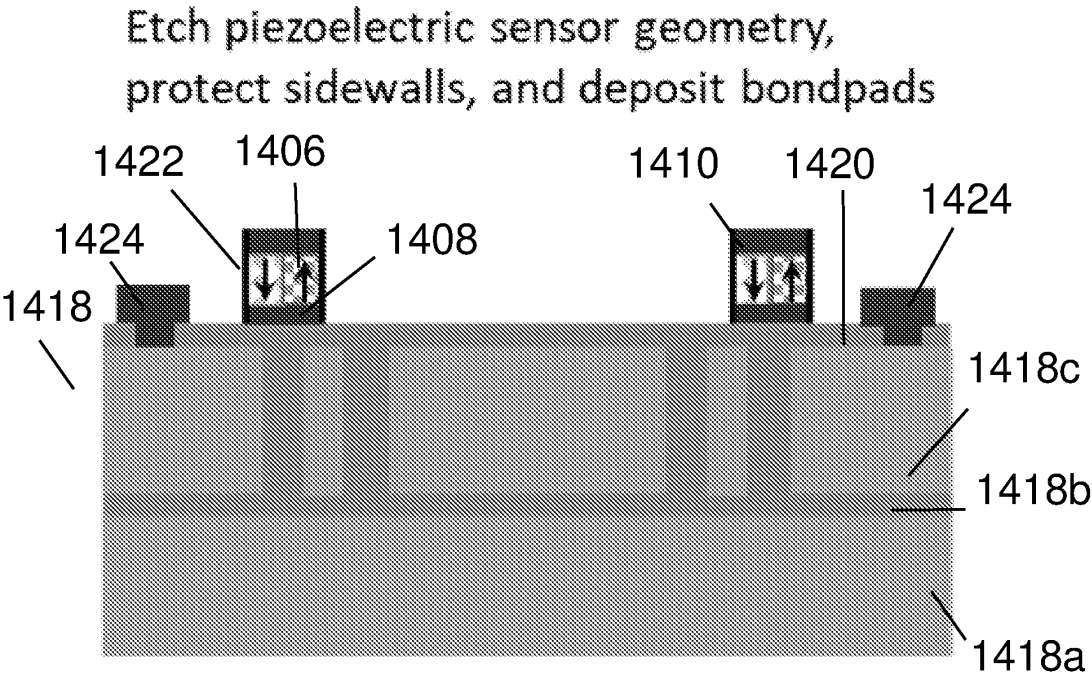


FIG. 14F

